## More Top Quark Physics and the Trigger Program

Ken Johns 07 November 2006



- Designed to reduce the L1 trigger rate for electrons and taus at high luminosity by exploiting the L1CAL and L1CTT Run IIb trigger upgrades
- L1CTK trigger algorithms match φ position of EM/jet objects from L1CAL with φ position of tracks from L1CTT
  - Matching in  $E_T/P_T$  is also used
  - Isolation and CPS/FPS information is also used
- Based on the successful L1MU trigger architecture developed by Arizona for Run II

11/6/2006



- Arizona holds sole responsibility for the L1CTK trigger hardware and software
  - Hardware
    - Day-to-day operations, monitoring, and maintenance
    - Trouble-shooting
    - Documentation for shifters
  - Software
    - Online control and monitoring ("Examine" and REGMON GUI's)
    - Offline "reconstruction" of L1CTK data
    - L1CTK trigger simulator and certification
    - Data analysis (e.g. efficiency, purity, optimization)
- These tasks are fundamentally important ones for DØ and require a substantial time and intellectual commitment
- Obviously we draw heavily on L1MU hardware and software accomplishments

11/6/2006



### Hardware status All trigger hardware installed and integrated by early 2006 16 trigger cards, 16 flavor boards, 6 crate managers, 12 splitter cards Tested with upgraded L1CAL and L1CTT triggers during 2006 shutdown Still\* waiting for latency shift to occur at DØ In the meantime we are focusing on software and offline analysis 11/6/2006 K. Johns

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AIR/WATER HEAT EXCHANGE

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### L1CTK trigger crate

### L1CTK manager crate

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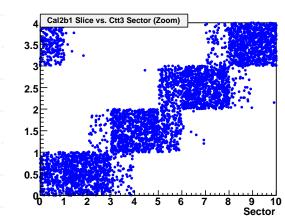
Sof 🔷	tware status	
	<ul> <li>reviously</li> <li>Developed suite of online GUI's</li> <li>Developed class structure for evaluating L1 trigger algorithms</li> </ul>	СТК
	<ul> <li>1ore recently</li> <li>Completed offline analysis package (unpacket) etc.)</li> </ul>	king,
	<ul> <li>Developed L1CTK trigger simulator (can be inside or outside DØ framework)</li> <li>Completed L1CTK monitoring in "Examine"</li> </ul>	run
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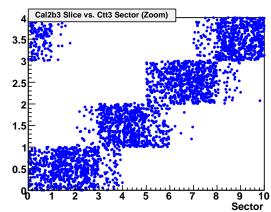


### $\phi \phi$ matching algorithms

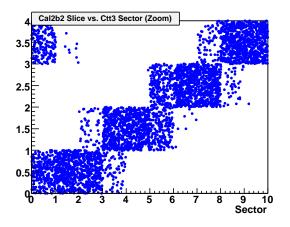
sliceVsector\_Z\_pt3

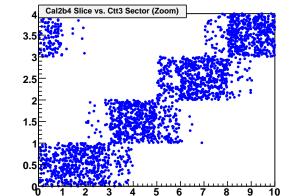
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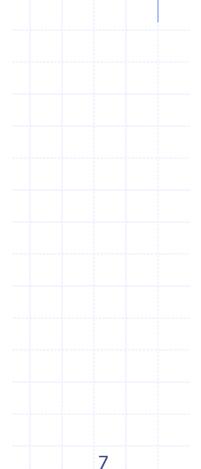




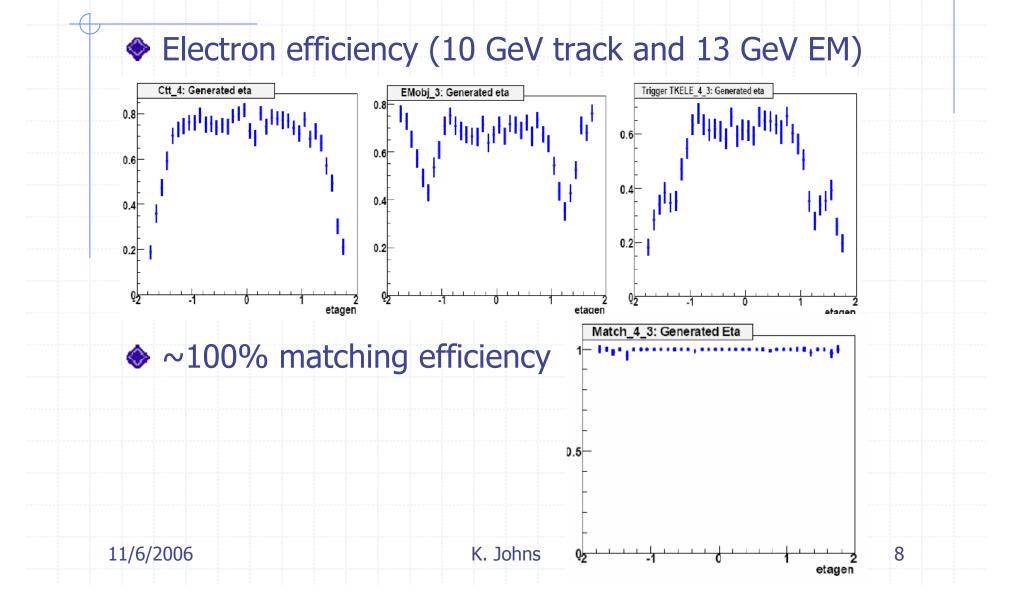




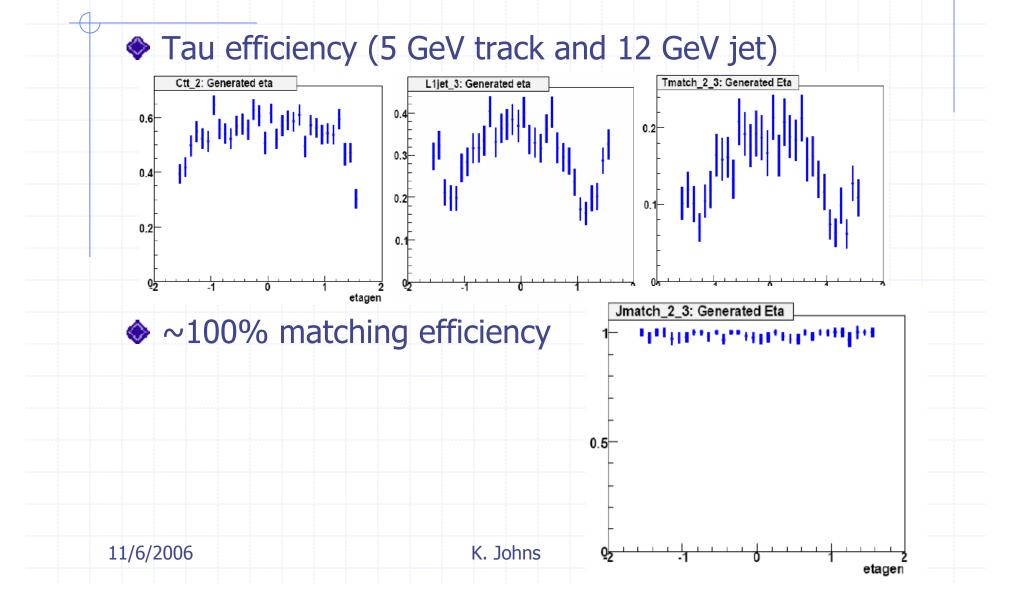
Sector











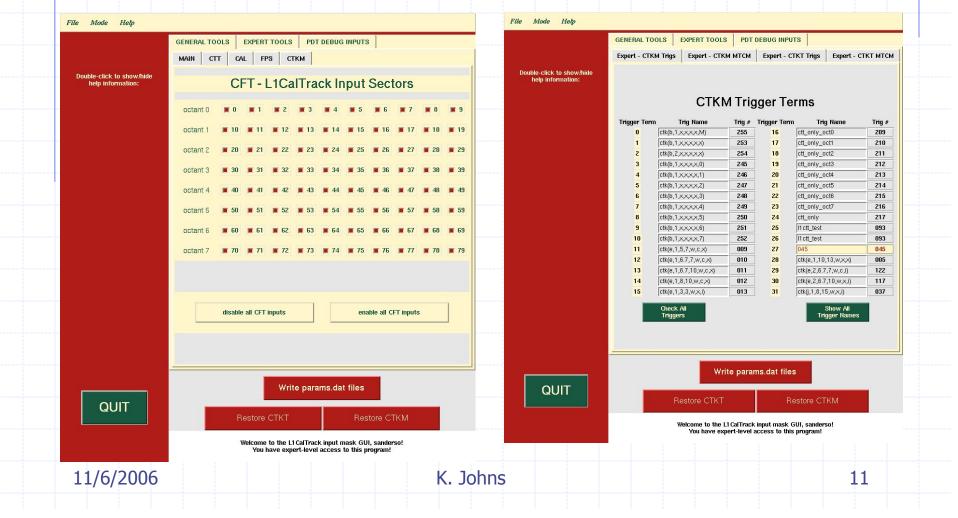


L1CTK power supply control and monitoring

СТКТ	СТКМ	L1CTK Su	pply									
Device	U0 (+5V) Voltage Current	U1 (+12V) Voltage Current	U2 ( -12  V) Voltage Current	U3 (+3.3V) Voltage Current	U4 (+5V) Voltage Current	U5 (+12V) Voltage Current	U6 ( -12  V) Voltage Current	U7 (+3.3V) Voltage Current	SUPPLY STATUS			
					L1CTK Su in MCH	ipply Located 1 Rack 119						
L1CTK Voltage (V)	4.98	12.00	11.96	3.31	4.97	11.91	11.84	3.31	Normal	On	Off	Reset
L1CTK Current (A)	24.01	5.41	0.48	56.68	8.54	0.91	0.48	7.97				
Status:	Clear P	Parity										Exit
	Clear P	Parity										Exit
	Clear P	arity										Exit
	Clear P	'arity										Exit
	Clear P	'arity										Exit
	Clear P	'arity										Exit
	Clear P	'arity										Exit
	Clear P	'arity										Exit



### L1CTK online control





### REGMON monitoring

#### Error registers are also monitored by alarm system

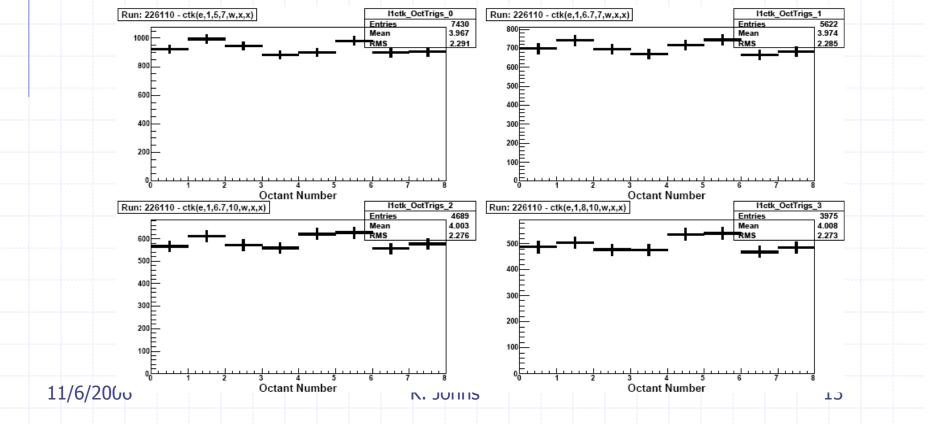
СТКТ	СТКМ										
Device	MaskA	MaskB	LockA	LockB	FF FullA	FF FullB	ParityA	ParityB	D-AvailA	D-AvailB	
					L1 Cal Tra	ck Trigger Cra	ate				·
CTKT-S1	0x1c00	Oxf	0xc00	0x0	Oxfff	0x0	0x0	0x0	0xf3ff	0xf3ff	Clear Pari
CTKT-S3	0x1c00	Oxf	0xc00	0x0	Oxfff	0x0	0x0	0x0	0xf3ff	0xf3ff	Clear Pari
CTKT-S5	0x1c00	Oxf	0xc00	0x0	Oxffff	0x0	0x0	0x0	0xf3ff	0xf3ff	Clear Pari
CTKT-S7	0x1c00	Oxf	0xc00	0x0	Oxfff	0x0	0x0	0x0	0xf3ff	0xf3ff	Clear Pari
CTKT-S9	0x1c00	Oxf	0xc00	0x0	Oxffff	0x0	0x0	0x0	0xf3ff	0xf3ff	Clear Pari
CTKT-S11	0x1c00	Oxf	0xc00	0x0	Oxffff	0x0	0x0	0x0	0xf3ff	0xf3ff	Clear Pari
CTKT-S13	0x1c00	Oxf	0xc00	0x0	Oxffff	0x0	0x0	0x0	0xf3ff	0xf3ff	Clear Pari
CTKT-S15	0x1c00	Oxf	0xc00	0x0	Oxfcff	0x0	0x0	0x0	0xf3ff	0xf3ff	Clear Par
Status:	ct Clea	r Parity									Exit
Reconne											



### Online "Examine" plots

Φ distribution of electron triggers for different

 $(P_T, E_T)$  thresholds

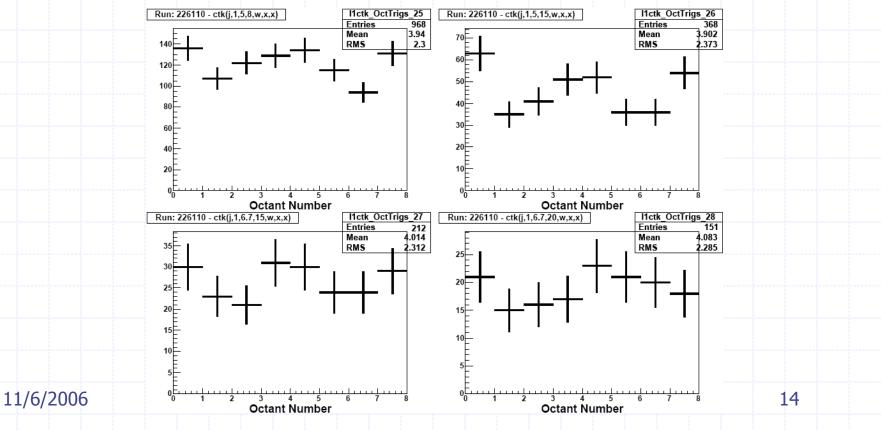




### Online "Examine" plots

•  $\Phi$  distribution of tau triggers for different ( $P_T, E_T$ )

thresholds



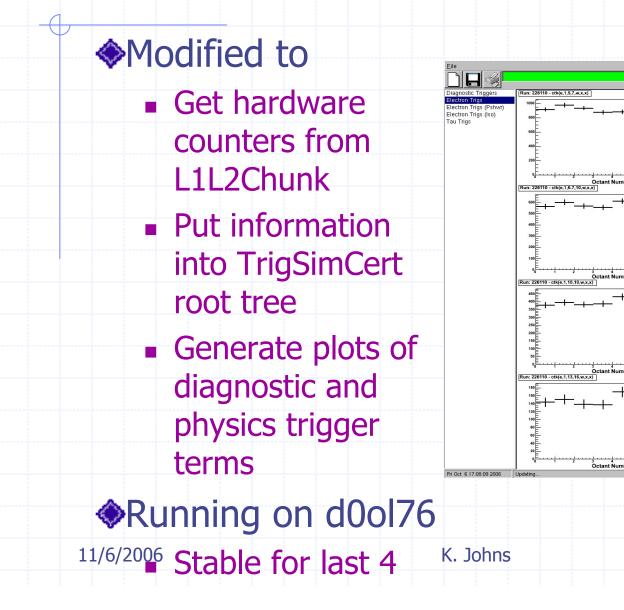


### Software: Trigger Examine

Plot Info Prev Config

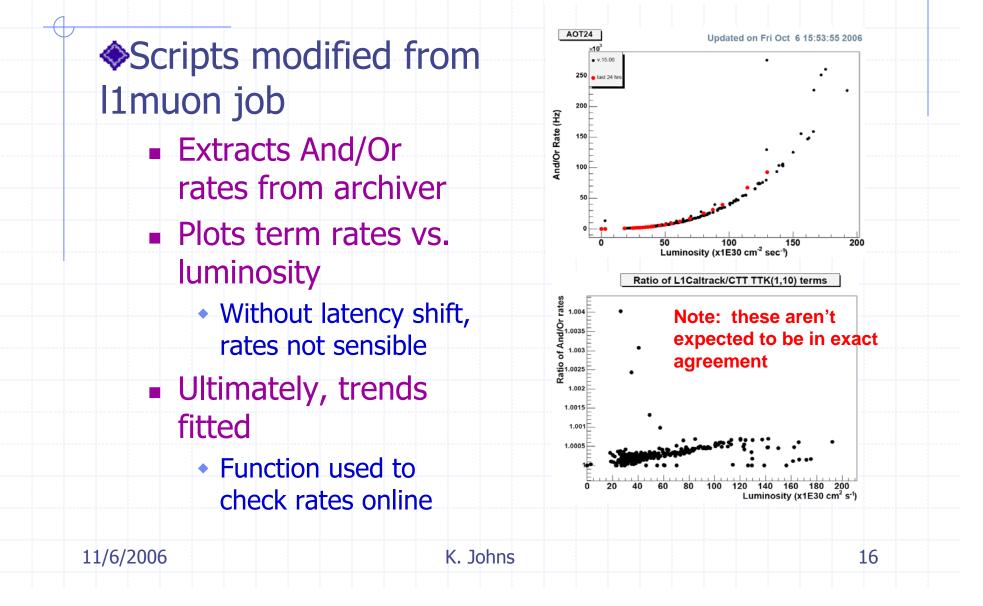
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n: 226110 - ctk(e,1,10,13,w.x,x)





## Software: Rate Montoring





Arizona (Anderson, Burke, Johns, Steinberg, and Temple) is solely responsible for all aspects of the L1CTK trigger

This (2006) is the last year Arizona will likely be able to provide substantial hardware and software support services to DØ

11/6/2006

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Arizona continues to hold primary responsibility for the L1MU trigger hardware and software

Hardware

- Day-to-day operations, monitoring, and maintenance
- Trouble-shooting (sometimes the entire muon system)
- Instructions for shifters
- Support for L1CTT and FPD trigger managers
- Software
  - Online control and monitoring ("Examine" and REGMON GUI's)
  - Offline "reconstruction" of L1MU data
  - L1MU trigger simulator and certification
  - Data analysis (e.g. efficiency, purity, optimization)

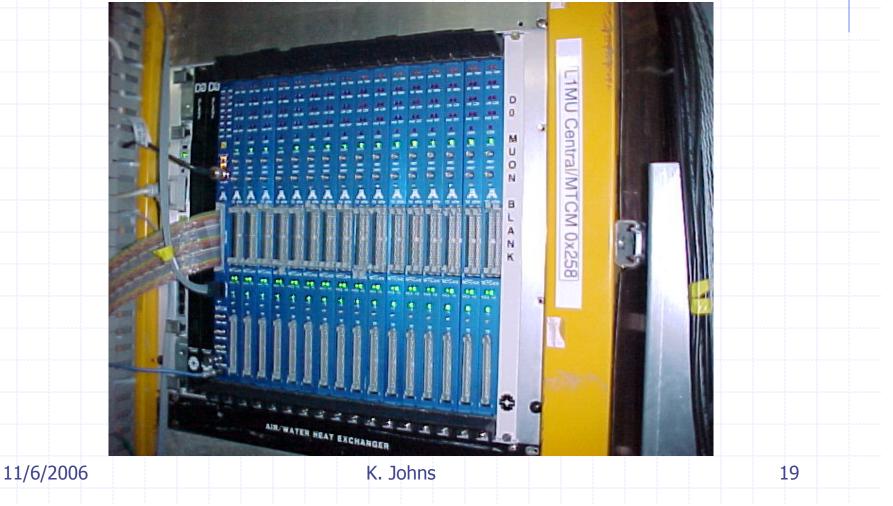
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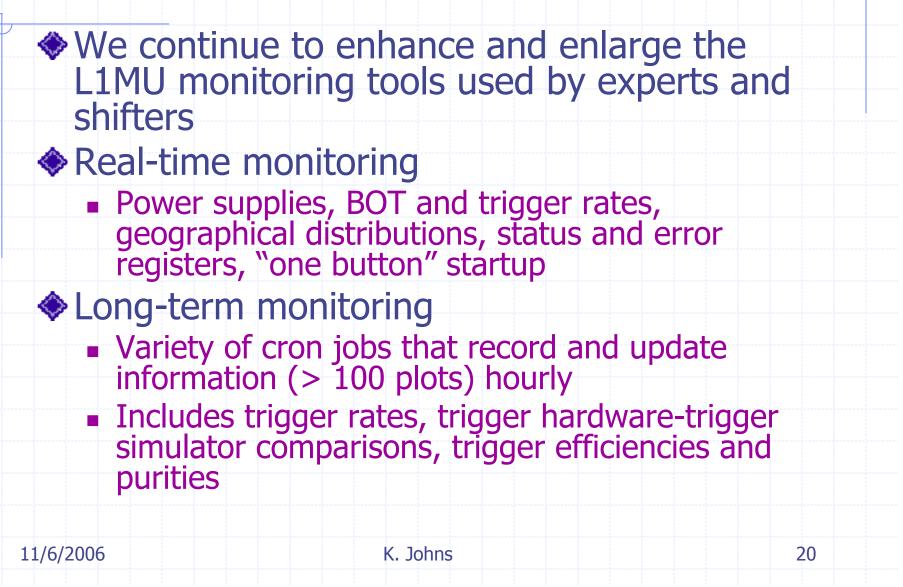
K. Johns

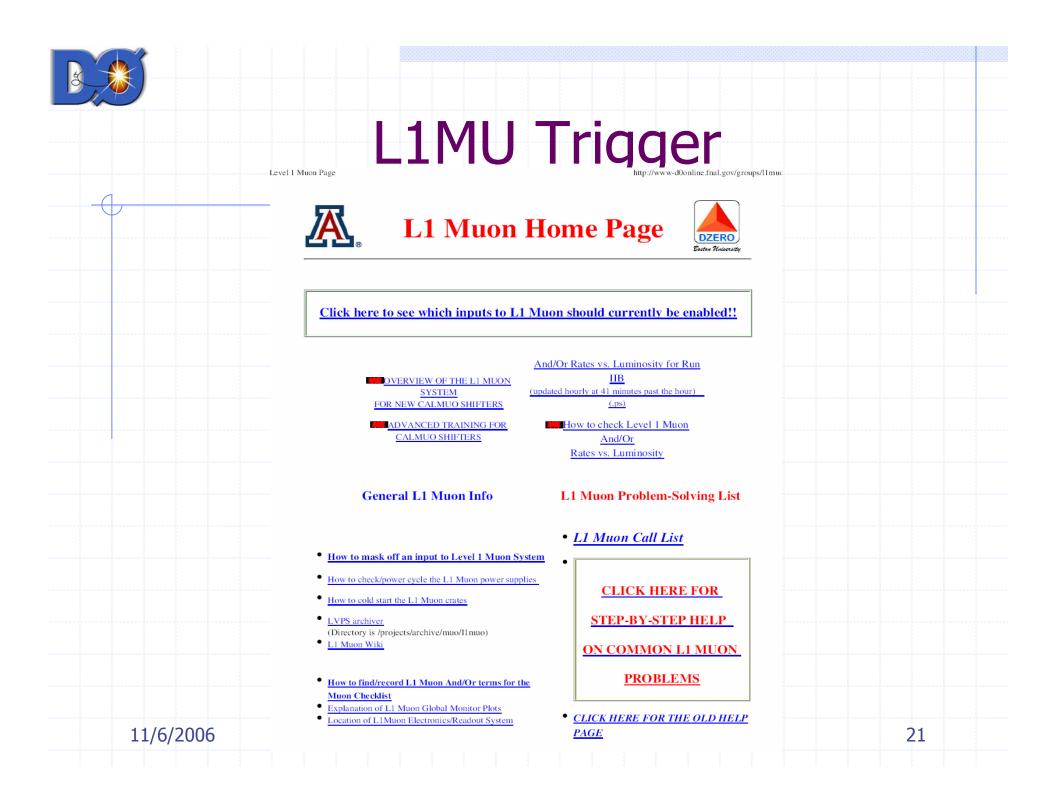


### In the collision hall











Tabs for individual crates

	<u>F</u> ile <u>V</u> iew								<u>H</u> e
	L1MU Supp	lies MTCC	MTCN	MTCS	мтм	1			
	Device	Mask	Lock	FF Full	Parity	Latch Error			
				]	L1 Muon Cent	tral Trigger Crate			
	MTCC_XX0	0x4000	0x4000	0x0	0x4000	0x0	Clear Parity	Clear Latch Error	
	MTCC_XX1	0x0	0x0	0x0	0x0	0x0	Clear Parity	Clear Latch Error	
Expand to	MTCC_XX2	0x4000	0x4000	0x0	0x4000	0x0	Clear Parity	Clear Latch Error	
	MTCC_XX3	0x0	0x0	0x0	0x0	0x0	Clear Parity	Clear Latch Error	
	MTCC_XX4	0x4000	0x4000	0x0	0x0	0x0	Clear Parity	Clear Latch Error	
see	MTCC_XX5	0x0	0x0	0x0	0x0	0x0	Clear Parity	Clear Latch Error	
-	MTCC_XX6	0x4000	0x4000	0x0	0x0	PDT016 Good	ear Parity	Clear Latch Error	
individual	MTCC_XX7	0x0	0x0	0x0	0x0	PDT026 Good	ear Parity	Clear Latch Error	
individual	MTCC_XX8	0x4000	0x4000	0x0	0x40	PDT036 Good PDT106 Good	ear Parity	Clear Latch Error	
errors	MTCC_XX9	0x0	0x0	0x0	0x0	PDT116 Good	ear Parity	Clear Latch Error	
CHUIS	MTCC_XXA	0x0	0x0	9x0	0x0	PDT136 Good	ear Parity	Clear Latch Error	
	MTCC_XXB	0x1000	0x1000	0x0	0x10	PDT146 Good	ear Parity	Clear Latch Error	
	MTCC_XXC	0x0	0x0	0x0	0x0	Bphi Oct6 #0 Good	ear Parity	Clear Latch Error	
	MTCC_XXD	0x1000	0x1000	0x0	0x80	PDT206 Good PDT216 Good	ear Parity	Clear Latch Error	
	MTCC_XXE	0x4000	0x4000	0x0	0x0	PDT236 Good	ear Parity	Clear Latch Error	
	MTCC_XXF	0x0	0x0	0x0	0x0	PDT246 BAD!	ear Parity	Clear Latch Error	
	Status: Clear In	tched error finish	and .			No Connect			
	status, joiear la	iterieu en or ninsi	ieu	$\lambda$		Aphi Oct6 Good	_ /		
	Reconnect	Clear Parit	y Clear L	Error		Bphi Oct6 #1 Good CMSC Oct6 (Conc) Goo	od		Exit
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Help

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### ♦ L1MU REGMON GUI

✓ L1 Muon PS Monitor and Error Register Display.

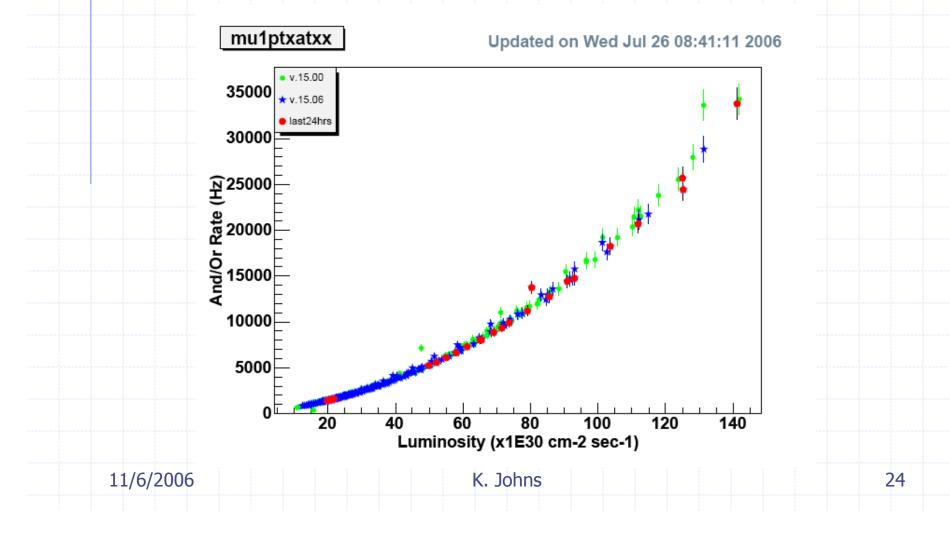
File View

LIMU Suppli	es MTCC	MTCN	MTCS	MTM	LICTITest	LIPDTTest	
Device	Mask	Lock	FF Full	Parity	Latch Error		
				L1 Muon South	Trigger Crate		
TCS_XX0	0x0	0x0	0x0	0x0	0x0	Clear Parity	Clear Latch Error
TCS_XX1	0xcf00	0xf00	0x0	0x800	0x0	Clear Parity	Clear Latch Error
TCS_XX2	0x0	0x0	0x0	0x0	0x0	Clear Parity	Clear Latch Error
CS_XX3	0xcf00	0xf00	0x0	0x800	0x0	Clear Parity	Clear Latch Error
TCS_XX4	0x0	0x0	0x0	0x0	0x0	Clear Parity	Clear Latch Error
TCS_XX5	0xcf00	0xf00	0x0	0x4	0x0	Clear Parity	Clear Latch Error
TCS_XX6	0x0	0x0	0x0	0x0	0x0	Clear Parity	Clear Latch Error
TCS_XX7	0xcf00	0xf00	0x0	0x0	0x0	Clear Parity	Clear Latch Error
TCS_XX8	0x0	0x0	0x0	0x0	0x0	Clear Parity	Clear Latch Error
rcs_xx9	0xcf00	0xb00	0x400	0x400	0x0	Clear Parity	Clear Latch Error
CS_XXA	0x0	0x0	0x0	0x0	0x0	Clear Parity	Clear Latch Error
TCS_XX8	0xcf00	0xf00	0x0	0x800	0x0	Clear Parity	Clear Latch Error
TCS_XXC	0x0	0x0	0x0	0x0	0x0	Clear Parity	Clear Latch Error
TCS_XXD	0xcf00	0xf00	0x0	0x0	0x0	Clear Parity	Clear Latch Error
TCS_XXE	0x0	0x0	0x0	0x0	0x0	Clear Parity	Clear Latch Error
TCS_XXF	0xcf00	0xf00	0x0	0x0	0x0	Clear Parity	Clear Latch Error

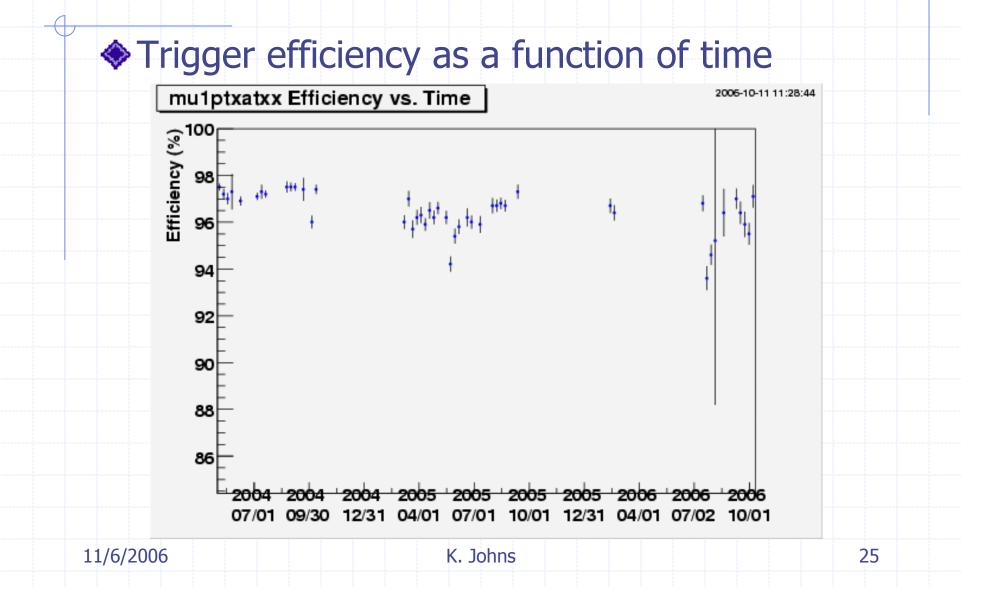
K. Johns

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### Trigger rate as a function of luminosity







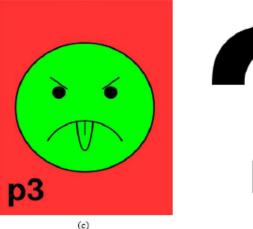


### Results when cursor placed over plot



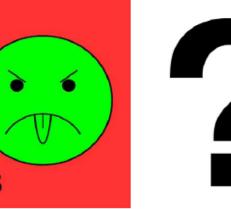
(a)







(d)

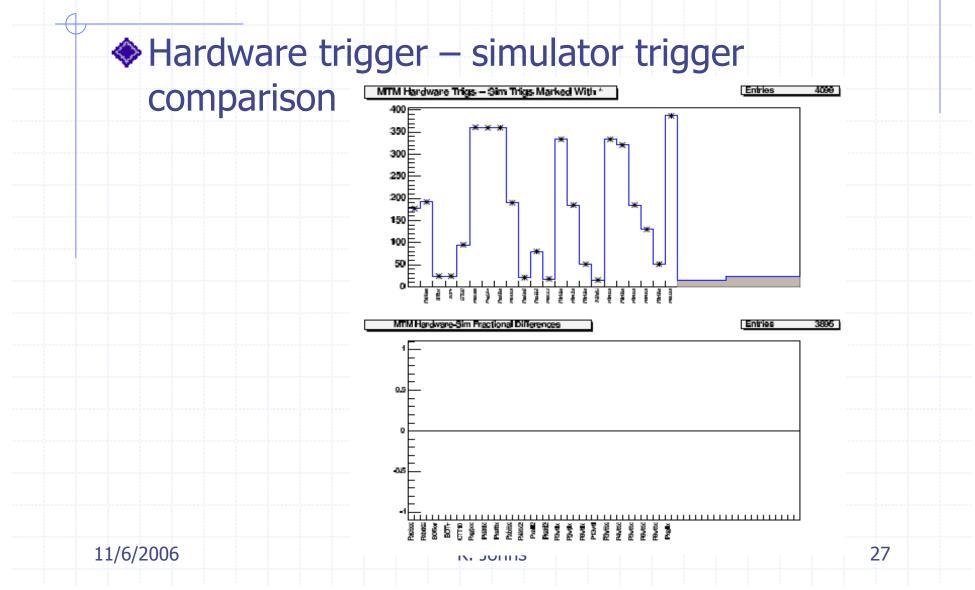






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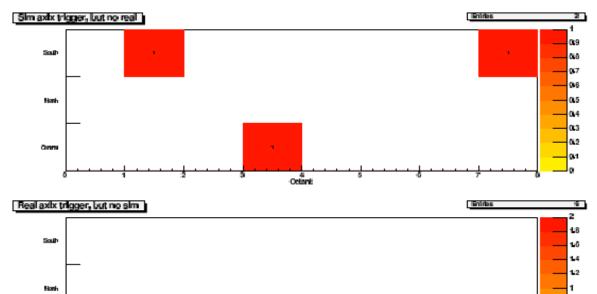


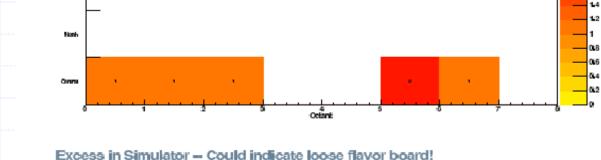


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## L1MU Trigger

# Hardware trigger – simulator trigger comparison





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The stellar performance of the L1MU trigger is due to the personal responsibility assumed by Anderson, Burke, Johns, Steinberg, and Temple

 Aside, it was the only L1 trigger system that did not need to be upgraded for higher luminosity running

This (2006) is the last year Arizona will likely be able to provide critical operation services to DØ

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