ANNECY lapp

ABBA Electronics

ymca_card_v0

MODIFIE: Fri Jan 30 09:52:36 2015

ETUDE: N.Dumont Dayot | PAGE: 1 / 27

DESSIN: N.Dumont Dayot | SHEET: 1 / 27

MENU

VCC=P3V3_IPMI
(GND:53,22,63,65;VCC:21,52)

p3v3_ipmi
C382 100N
GND

atmga128 U31

2B5 IN ATMEGA_RESET → 20 RESET*

24 XTAL1
23 XTAL2

4B6 IN POWER_SEQ_FAULT_N → 51 PA0
4B6 IN POWER_SEQ_DONE_N → 50 PA1
3B1 IN MMC_TEMP_ALARM_N → 49 PA2
48 PA3
47 PA4
46 PA5
45 PA6
44 PA7

R110 33K R111 33K R112 33K

23B7 IN
23B7 IN
23B7 IN
AMC_GA0 → 10 PB0
AMC_GA1 → 11 PB1
AMC_GA2 → 12 PB2
13 PB3
14 PB4

3D7 OUT MMC_LED_RED_N → 15 PB5
3D7 OUT MMC_LED_GREEN_N → 16 PB6
3D7 OUT MMC_LED_BLUE_N → 17 PB7

25E8 OUT MMC_FPGA_RESETN → 37 PC2
25D4 OUT MMC_FPGA_RELOADN → 38 PC3
2A8 25C4 IN MMC_FPGA_INIT_DONE → 39 PC4
40 PC5
41 PC6
4D8 OUT MMC_DC_DC_EN → 42 PC7

35 PC0
36 PC1

1 PEN*

AVCC 64
AREF 62

MMC:ATMEGA128

R186 33
R187 33
AMC_SCL_L
AMC_SDA_L
MMC_MICROSWITCH_N
MMC_SCL
MMC_SDA

PD0 25
PD1 26
PD2 27
PD3 28
PD4 29
PD5 30
PD6 31
PD7 32

MMC:ATMEGA128

PE0 2
PE1 3
PE2 4
PE3 5
PE4 6 MMC_FPGA_USER_IO0 BI 25D4
PE5 7 MMC_FPGA_USER_IO1 BI 25D4
PE6 8
PE7 9

PF0 61
PF1 60 A10_G1_VCC_POK IN 5B6 4C2
PF2 59 A10_G2_POWER_POK IN 7D3 4C2
PF3 58 A10_G3_POWER_POK IN 8C1 8D4 4C2
PF4 57 CON_ATMEGA_JTAG_TCK IN 24C6 24B4
PF5 56 CON_ATMEGA_JTAG_TMS IN 24B6 24B4
PF6 55 CON_ATMEGA_JTAG_MISO OUT 24A3 24B6
PF7 54 CON_ATMEGA_JTAG_MOSI IN 24B6 24A4

PG0 33
PG1 34
PG2 43
PG3 18
PG4 19

p3v3_ipmi
R116 33K R117 33K R118 4.7K

AMC_SCL_L IN 23A7
AMC_SDA_L BI 23A7
MMC_MICROSWITCH_N IN 3B6
MMC_SCL OUT 3A6 3B1 3D1
MMC_SDA BI 3A6 3B1 3D2

R121 AMC_PS1_N IN 23B5 2A5
AMC_PS0_N IN 23B5 2A3
R120 150K
R119 330
390K

GND

VP12
R122 150K
R123 49.9K
GND

p3v3_ipmi
C381 1.0N
GND

VCC : 21,52
GND : 53,22,63
THERMAL_PAD : 65,66,67,68

GND=GND
VCC=P3V3_IPMI

p3v3_ipmi
R113 4.7K R114 4.7K

SN74LVC2G06DCKR
U30
24B6 23B4 IN AMC_ENABLE_N → 1 1A 1Y 6 → ATMEGA_RESET OUT 2D6

SN74LVC2G06DCKR
U30
2C6 25C4 IN MMC_FPGA_INIT_DONE → 3 2A 2Y 4 → FPGA_INIT_DONE_LED_N OUT 3D7

GND=GND
VCC=P3V3_IPMI

VP12 test_pin 1 TEST T4
p3v3_ipmi test_pin 1 TEST T5

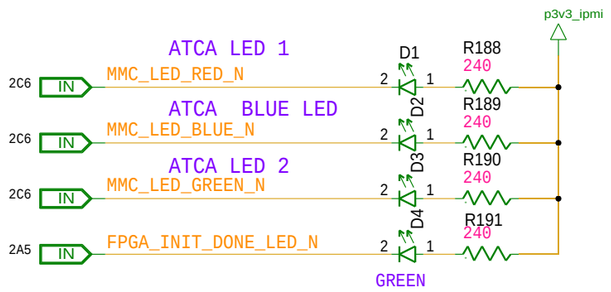
2D2 23B5 IN AMC_PS1_N → R115 0 → D8 A C BAT165 → AMC_PS0_N IN 23B5 2C2

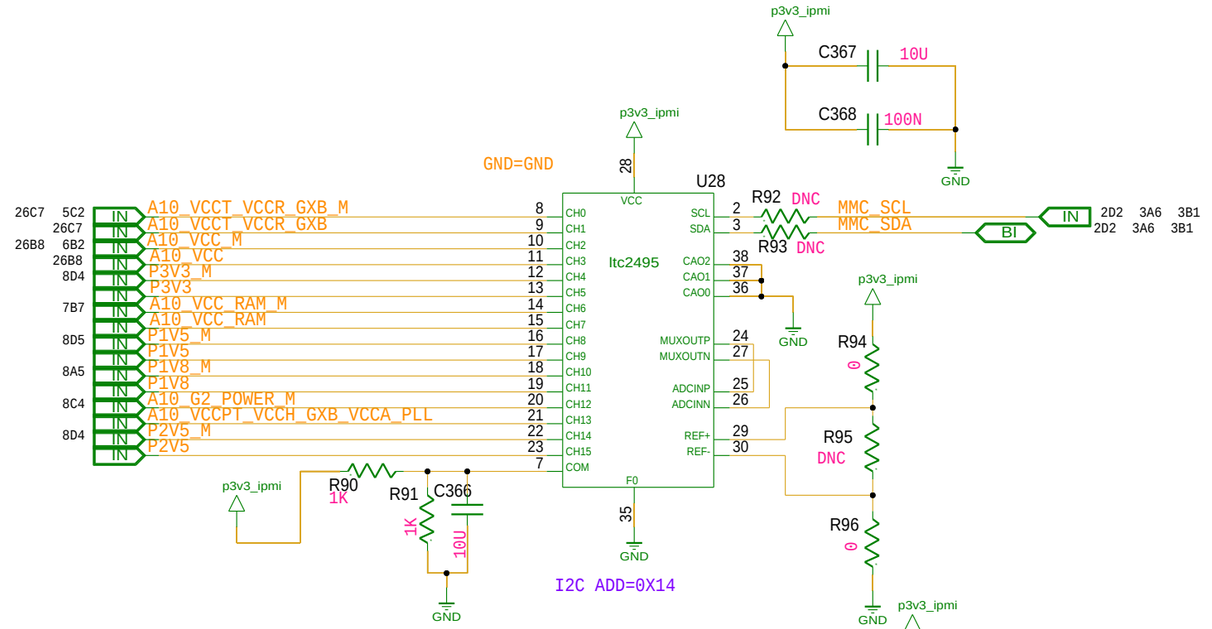
PS1/PS0 SCHOTTKY DIODE : 0.6V MAX WHEN 2MA

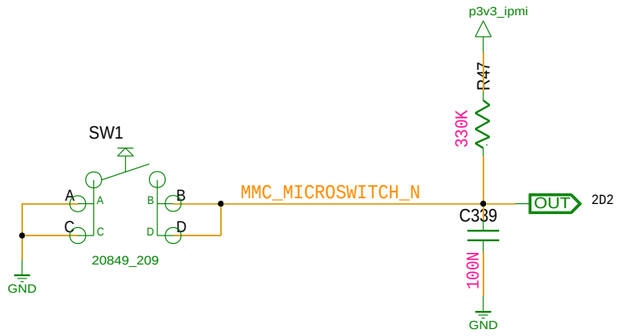
ANNECY lapp
ABBA Electronics

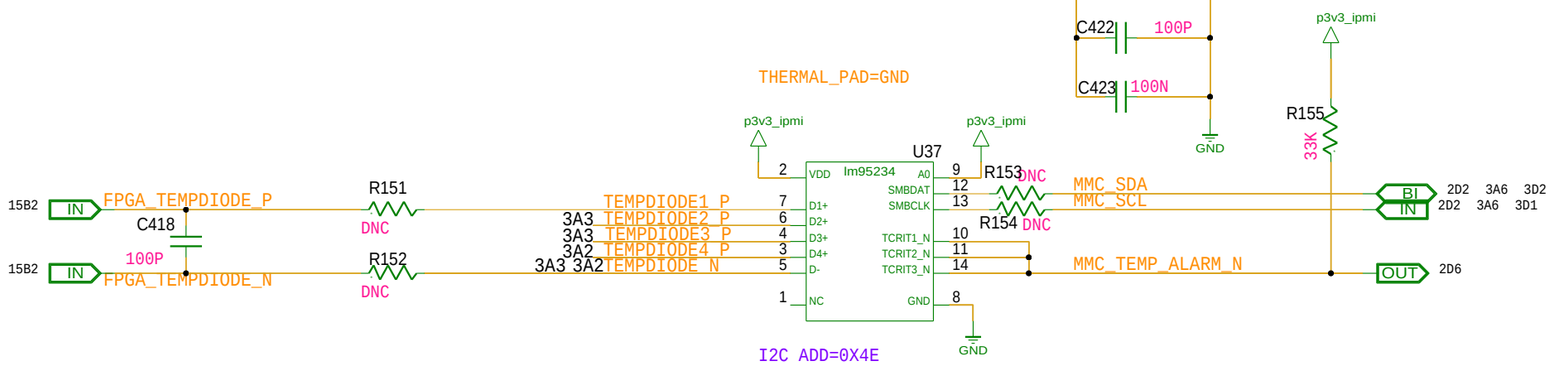
ymca_card_v0

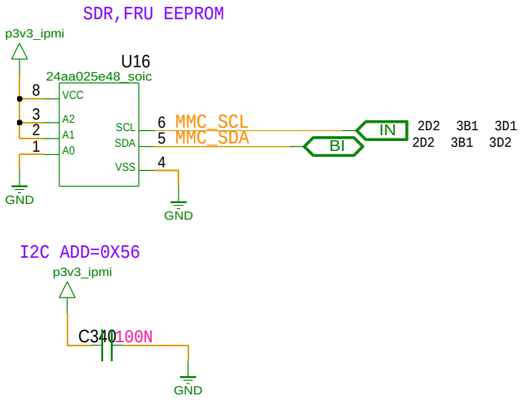
MODIFIE: Mon Mar 23 09:50:36 2015
ETUDE: N.Dumont Dayot | PAGE: 2 / 27
DESSIN: N.Dumont Dayot | SHEET: 2 / 27
MMC:ATMEGA128

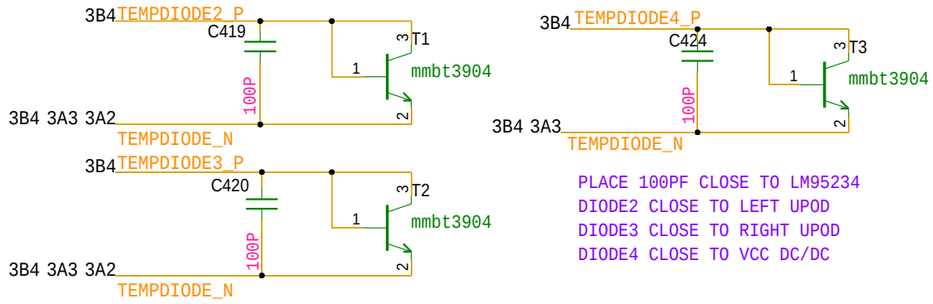












ANNECY lapp ABBA Electronics

ymca_card_v0

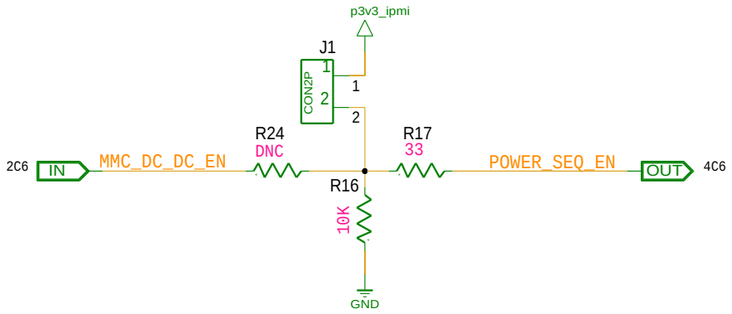
MODIFIE: Mon Mar 23 09:50:36 2015

ETUDE: N.Dumont Dayot | PAGE: 3 / 27

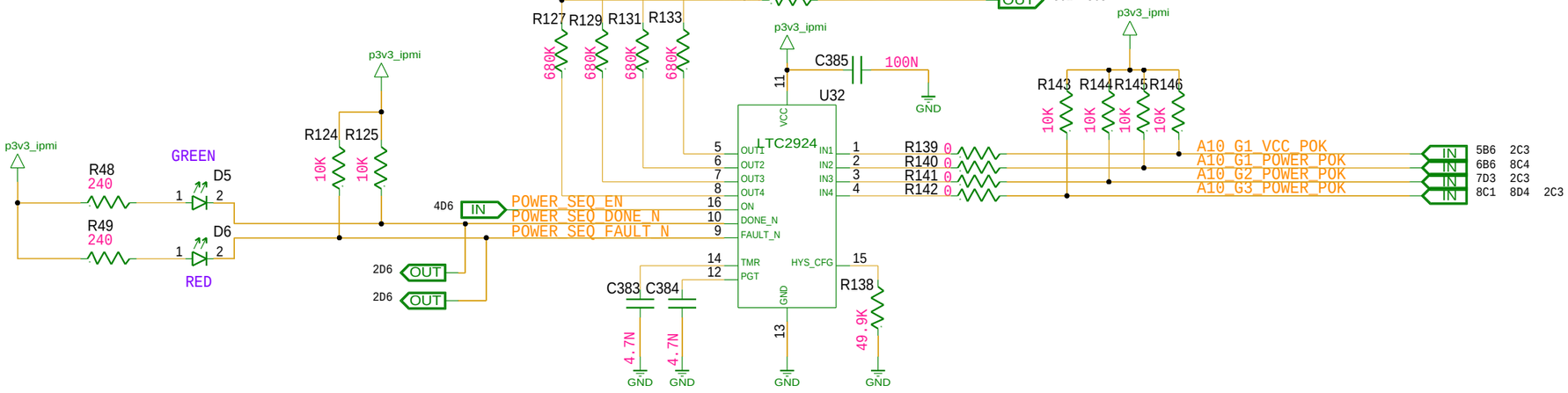
DESSIN: N.Dumont Dayot | SHEET: 3 / 27

MMC:EEPROM, SENSORS, OTHERS

DC/DC ENABLE BY MMC OR EXTERNAL SWITCH
FIRST : MMC NOT CONNECTED ('DNC'ON MMC_DC_DC_EN)



REGROUP RES 'DNC' MMC_DC_DC_EN WITH RES 'DNC' FPGA_N_CONFIG (P25)



POWER SEQUENCING : DELAY~1MS FOR IN TO OUT;1MS OUT TURNED ON
DETECTION ON DC/DC POWER GOOD SIGNALS : VON>=3V AND VOFF<2.7V
OUT~8V=>VOUT ENABLE ~2V

ANNECY lapp ABBA Electronics

ymca_card_v0

MODIFIE: Mon Mar 23 09:50:37 2015
ETUDE: N.Dumont Dayot | PAGE: 4 / 27
DESSIN: N.Dumont Dayot | SHEET: 4 / 27
ARRIA10 : VOLTAGE SEQUENCER

LOW LEAKAGE MOSFET <300NA

p3v3_ipmi

GND=GND
VCC=P3V3_IPMI

R51
4.7K

SN74LVC2G06DCKR
U17

4D4 IN A10_G1_VCC_EN 1 1A 1Y 6

SN74LVC2G06DCKR
U17
3 2A 2Y 4

p3v3_ipmi
C341
10N
GND

GND=GND
VCC=P3V3_IPMI

VP12
C342 C343
47U 47U
GND

6B6 LMZ31530_VCC_INH

INH MAX=7 V ; INTERNAL PULL UP

R52
825
GND

R53
160

4C2 2C3 OUT A10_G1_VCC_POK

SOFT START TIME ~2.8MS

p3v3_ipmi

GROUP1:VCC=0.95V@30A

PH_VCC
11 22 23 24 25 26 27 28 71
PH_0 PH_1 PH_2 PH_3 PH_4 PH_5 PH_6 PH_7 PH_8

U18

42 PVIN_0
43 PVIN_1
44 PVIN_2
66 PVIN_3
69 PVIN_4
2 VIN_0
15 VIN_1
16 INH
6 ILIM
7 FREQ_SEL
3 SS_SEL
19 PWRGD
18 PWRGD_PU

lmz31530

V5V 61
SENSE+ 14
VOUT_0 10
VOUT_1 52
VOUT_2 53
VOUT_3 54
VOUT_4 55
VOUT_5 56
VOUT_6 57
VOUT_7 58
VOUT_8 59
VOUT_9 60
VOUT_10 68
VADJ 13
AGND 9

A10_VCC_M

C344 C345 C346 C347
100U 100U 100U 100U
GND

R54
511
R55
2.00K

a10_vcc
R56
0.001
OUT 3D5 26C7

a10_vcc
test_pin
1 TEST T6

PGND_0 PGND_1 PGND_2 PGND_3 PGND_4 PGND_5 PGND_6 PGND_7 PGND_8 PGND_9 PGND_10 PGND_11 PGND_12 PGND_13 PGND_14 PGND_15 PGND_16 PGND_17 PGND_18 PGND_19 PGND_20 PGND_21 PGND_22
1 5 17 33 34 37 38 39 40 41 46 47 48 49 50 51 62 63 64 65 67 70 72
GND

ANNECY lapp ABBA Electronics

ymca_card_v0

MODIFIE: Mon Mar 23 09:50:37 2015
ETUDE: N.Dumont Dayot | PAGE: 5 / 27
DESSIN: N.Dumont Dayot | SHEET: 5 / 27
DC/DC ARRIA10 : GROUP1->VCC

LOW LEAKAGE MOSFET <300NA

p3v3_ipmi

GND=GND
VCC=P3V3_IPMI

R180
4.7K

SN74LVC2G06DCKR
U45

8D8 4D4 IN A10_G1_POWER_EN 1 1A 1Y 6

p3v3_ipmi
C516
100P
GND

SN74LVC2G06DCKR
U45
3 2A 2Y 4

GND=GND
VCC=P3V3_IPMI

GROUP1:VCCT_GXB=1.0V AND VCCR_GXB=1.0V (AT LEAST) FOR 11.3GBPS<DATA RATE<12.5GBPS

VCCT_GXB AND VCCR_GXB MERGED : 1.0V@30A

VP12
C517 C518
47U 47U
GND

PH_PWR
11 22 23 24 25 26 27 28 71
PH_0 PH_1 PH_2 PH_3 PH_4 PH_5 PH_6 PH_7 PH_8

U46
lmz31530

42 PVIN_0
43 PVIN_1
44 PVIN_2
66 PVIN_3
69 PVIN_4
2 VIN_0
15 VIN_1
16 INH
6 ILIM
7 FREQ_SEL
3 SS_SEL
19 PWRGD
18 PWRGD_PU

5C6 LMZ31530_PWR_INH

INH MAX=7 V ; INTERNAL PULL UP

R181
825
GND

R182
160

4C2 8C4 OUT A10_G1_POWER_POK

SOFT START TIME ~2.8MS

p3v3_ipmi

PGND_0 PGND_1 PGND_2 PGND_3 PGND_4 PGND_5 PGND_6 PGND_7 PGND_8 PGND_9 PGND_10 PGND_11 PGND_12 PGND_13 PGND_14 PGND_15 PGND_16 PGND_17 PGND_18 PGND_19 PGND_20 PGND_21 PGND_22
1 5 17 33 34 37 38 39 40 41 46 47 48 49 50 51 62 63 64 65 67 70 72
GND

V5V 61
SENSE+ 14
VOUT_0 10
VOUT_1 52
VOUT_2 53
VOUT_3 54
VOUT_4 55
VOUT_5 56
VOUT_6 57
VOUT_7 58
VOUT_8 59
VOUT_9 60
VOUT_10 68
VADJ 13
AGND 9

A10_VCCT_VCCR_GXB_M

R185
0.001

a10_vcct_vccr_gxb
OUT 3D5 26B8

C519 C520 C521 C522
100U 100U 100U 100U
GND

R183
196

R184
2.00K

T7
a10_vcct_vccr_gxb
test_pin
1 TEST

a10_vcct_vccr_gxb

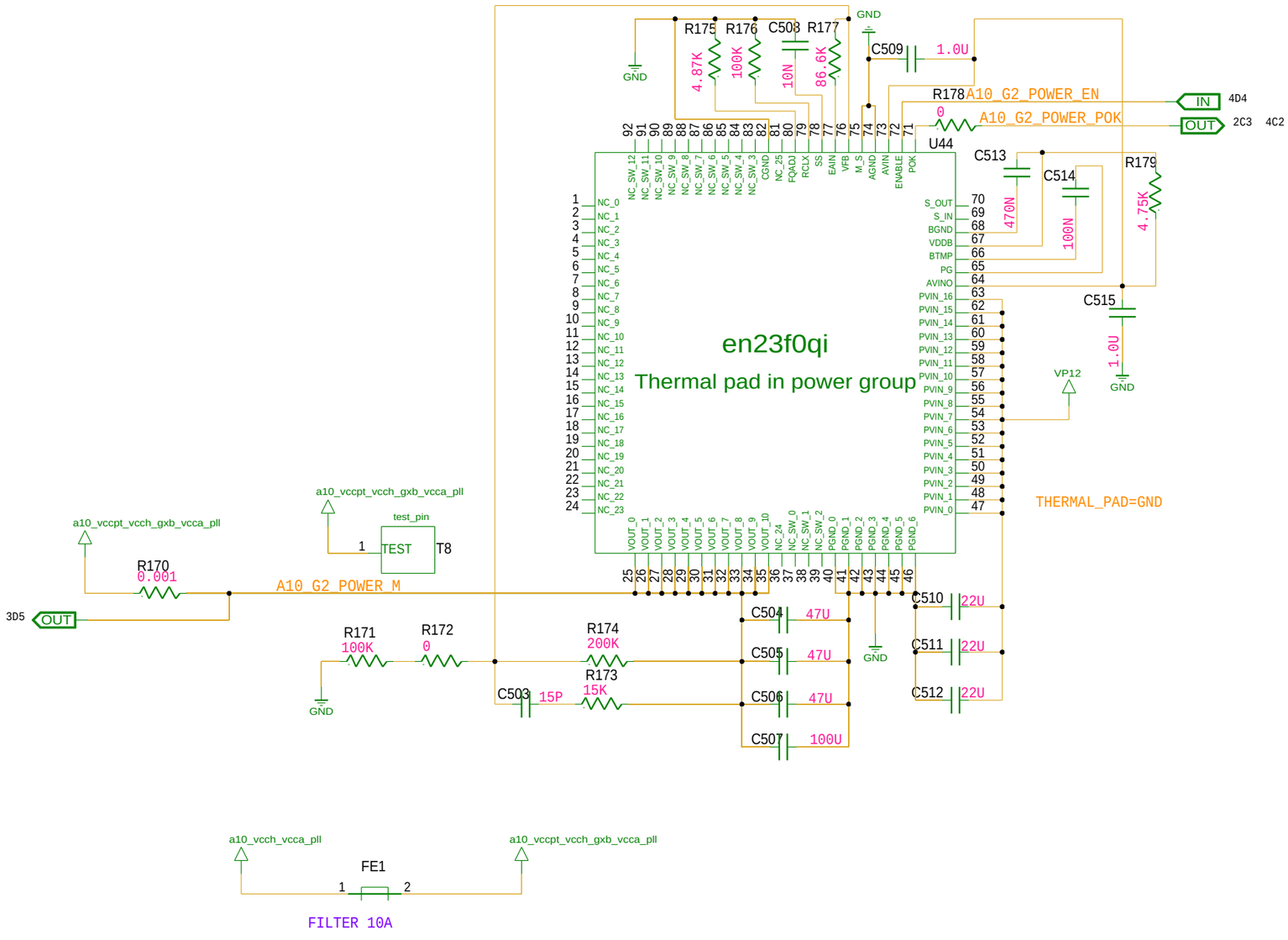
ANNECY lapp ABBA Electronics

ymca_card_v0

MODIFIE: Mon Mar 23 09:50:37 2015
ETUDE: N.Dumont Dayot | PAGE: 6 / 27
DESSIN: N.Dumont Dayot | SHEET: 6 / 27
DC/DC ARRIA10-GROUP1->VCCR,VCCT_GXB

EN2360QI & EN23F0QI : ENABLE CANNO'T BE ASSERTED BEFORE PVIN

GROUP2 : VCCPT,VCCH_GXB,VCCA_PLL=1.8V@15A



	ymca_card_v0	MODIFIE: Mon Mar 23 09:50:38 2015	
		ETUDE: N.Dumont Dayot	PAGE: 7 / 27
		DESSIN: N.Dumont Dayot	SHEET: 7 / 27
		DC/DC ARRIA10->GROUP2	

GROUP 1:VCC_RAM=0.95V
GROUP 3:VCCPGM=1.8V ; VCCIO [1.8V-1.5V]
OTHERS POWER SUPPLY : 3.3V [NB:UPOD~1.6A]

EN2360QI & EN23F0QI : ENABLE CANNO'T BE ASSERTED BEFORE PVIN

U29 LTM4644
GND in power group
C7 J3 F3 F7
C369 22U
C370 10U
C371 22U
C372 10U
C373 47U
C374 47U
C375 47U
C376 47U
C377 2.2N
C378 2.2N
C379 2.2N
C380 2.2N
R97 0
R98 13.3K
R99 0
R100 40.2K
R101 0
R102 100K
R103 0
R104 30.1K
R105 3.57K
R106 0.001
R107 0.001
R108 0.001
R109 0.001
P1V8_M
P1V5_M
A10_VCC_RAM_M
P3V3_M
A10_G3_POWER_POK
A10_G1_POWER_POK
A10_G1_POWER_EN
A10_G3_POWER_EN
P1V8
P1V5
P3V3
a10_vcc_ram
P2V5
VP12
GND
IN
OUT
6C7 4D4
8C1 4C4
3D5
8C1 4C2 2C3
6B6 4C2
T13 test_pin TEST
T9 T10 T11 T12

OTHER POWER SUPPLY : 2.5V@6A [NB:UPOD~3.6A]

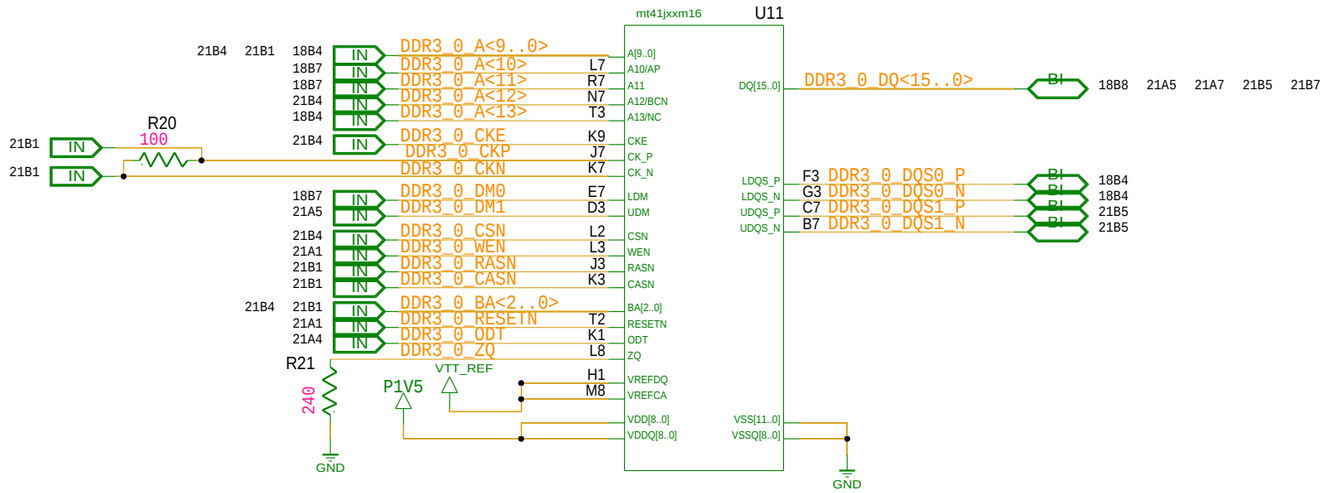
U13 en2360qi
Thermal pad in power group
THERMAL_PAD=GND
R30 10K
R31 100K
C182 10N
R32 56K
C186 1.0U
R33 0
R34 560
R35 4.75K
C188 220N
C189 47N
C190 1.0U
C187 22U
C183 47U
C184 47U
C185 100U
R25 0.001
R26 63.4K
R27 0
R28 200K
R29 12K
C181 12P
P2V5_M
8D4 4C2 2C3
4C4 8C8

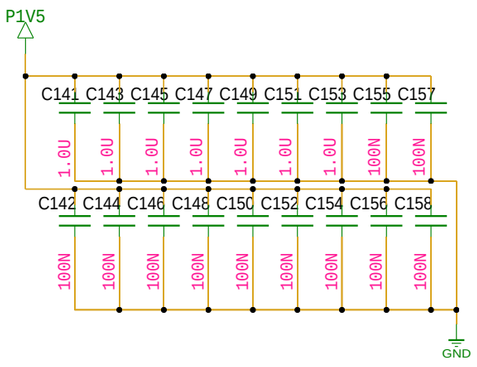
ymca_card_v0

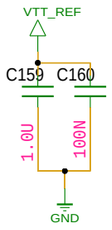
MODIFIE: Mon Mar 23 09:50:38 2015
ETUDE: N.Dumont Dayot
DESSIN: N.Dumont Dayot
PAGE: 8 / 27
SHEET: 8 / 27
DC/DC ARRIA10 GROUP3 AND VCCRAM
DC/DC FOR OTHER POWER SUPPLIES

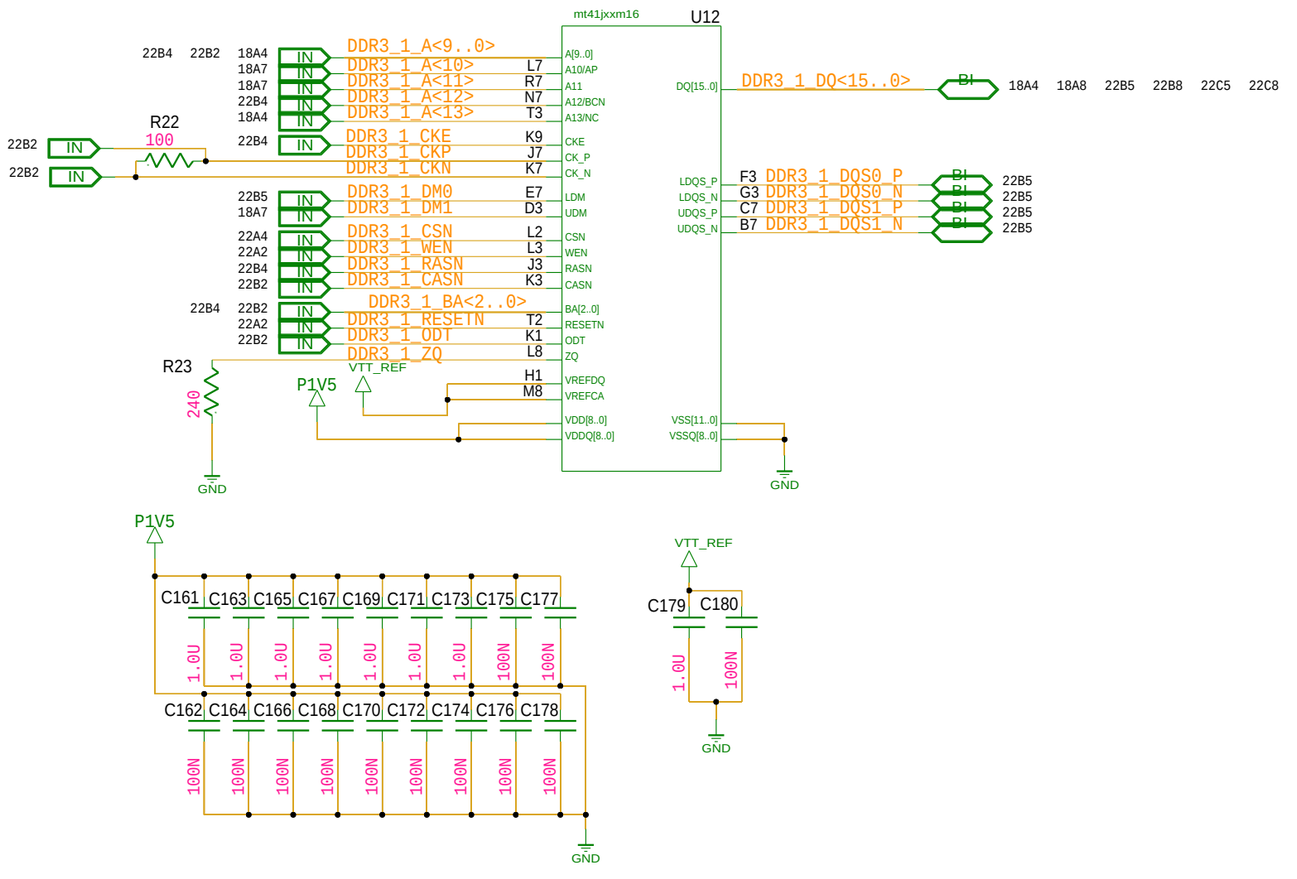
DDR3 1GBITS : A13 NOT CONNECTED
DDR3 2GBITS : A13 CONNECTED

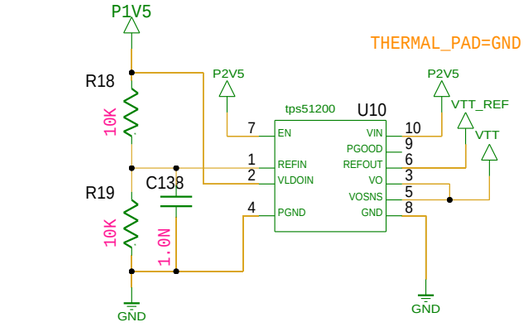
ARRIA10 CONNECTIONS : BANK ON TOP [3G,3H,2L,2K]

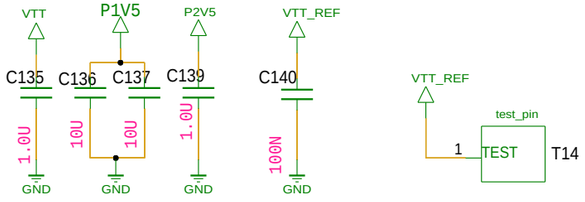












ANNECY lapp — ABBA Electronics

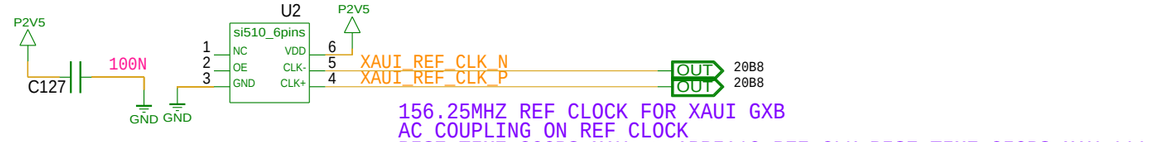
ymca_card_v0

MODIFIE: Mon Mar 23 09:50:39 2015

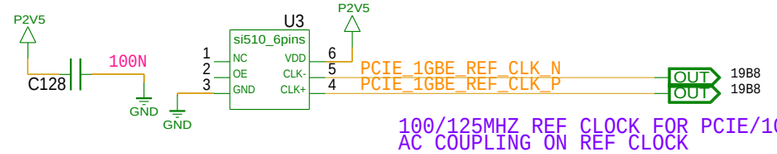
ETUDE: N.Dumont Dayot | PAGE: 9 / 27

DESSIN: N.Dumont Dayot | SHEET: 9 / 27

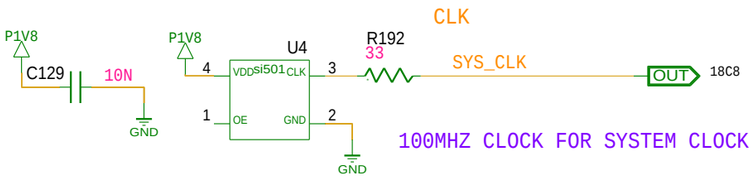
MEMORIES : DDR3



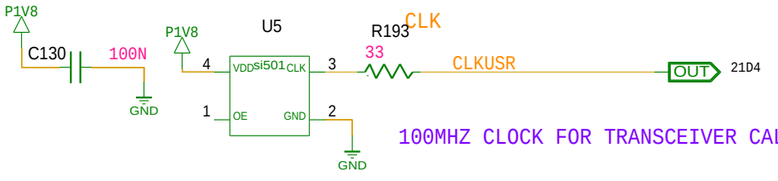
156.25MHZ REF CLOCK FOR XAUI GXB
AC COUPLING ON REF CLOCK
RISE TIME=800PS MAX => ARRIA10 REF CLK RISE TIME=250PS MAX !!!



100/125MHZ REF CLOCK FOR PCIE/1GBE GXB
AC COUPLING ON REF CLOCK

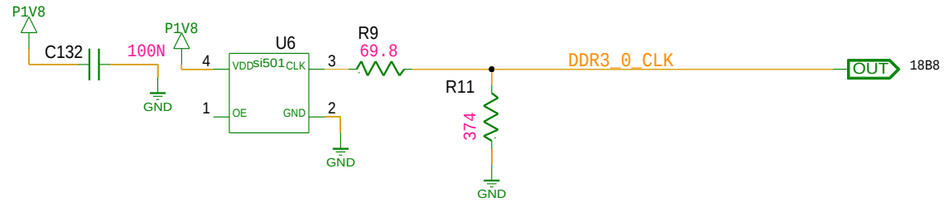


100MHZ CLOCK FOR SYSTEM CLOCK



100MHZ CLOCK FOR TRANSCEIVER CALIBRATION

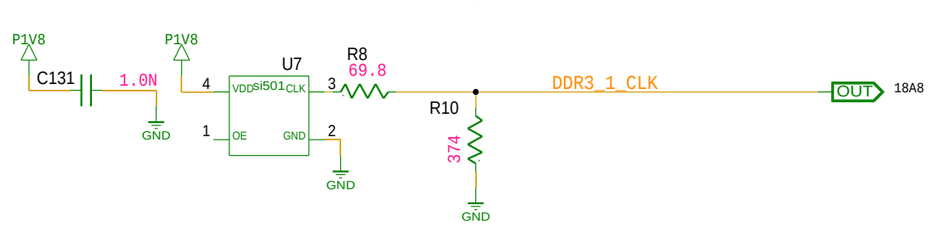
100MHZ CLOCK FOR DDR3_0



VOLTAGE DIVIDER FOR 1.5V APPLICATION
1/(2XPIXRC)~500MHZ
R=PARALLEL EQUIVALENT RESISTANCE
C=ARRIA10 INPUT CAPACITANCE (5PF FOR CALCUL)

IF 1.5V OSCILLATOR FOUND
CHANGE 69.8 BY 33 AND REMOVE 374

100MHZ CLOCK FOR DDR3_1

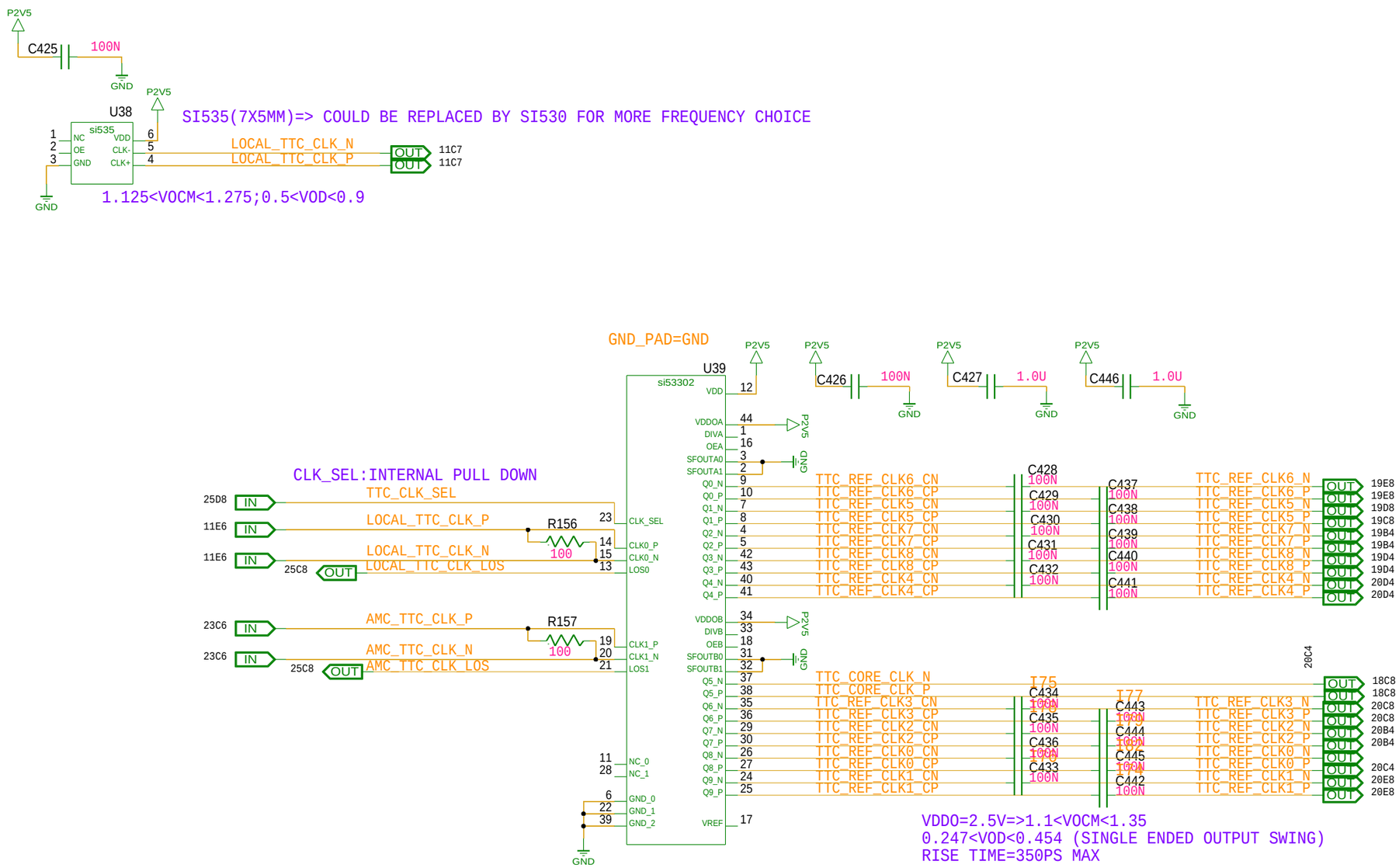


VOLTAGE DIVIDER FOR 1.5V APPLICATION
1/(2XPIXRC)~500MHZ
R=PARALLEL EQUIVALENT RESISTANCE
C=ARRIA10 INPUT CAPACITANCE (5PF FOR CALCUL)

IF 1.5V OSCILLATOR FOUND
CHANGE 69.8 BY 33 AND REMOVE 374

ymca_card_v0

MODIFIE: Mon Mar 23 09:50:39 2015
ETUDE: N.Dumont Dayot | PAGE: 10 / 27
DESSIN: N.Dumont Dayot | SHEET: 10 / 27
STANDARD CLOCKS



ymca_card_v0	MODIFIE: Mon Mar 23 09:50:44 2015
	ETUDE: N.Dumont Dayot — PAGE: 11 / 27
	DESSIN: N.Dumont Dayot — SHEET: 11 / 27
	TTC CLOCKS

UPOD_TX_L0

RESETN:INTERNAL PULL UP

I2C ADD=0X28

U40

afbr_77d2sz

TX_UPOD_RESETN F4 RESETL

TX_UPOD_SDA D4 SDA_0

TX_UPOD_SCL E4 SCL_0

TX_UPOD_SDA D6 SDA_1

TX_UPOD_SCL E6 SCL_1

G3 ADDR0

E3 ADDR1

C3 ADDR2

TX_UPOD_L0_P<0> D1 DIN0+

TX_UPOD_L0_N<0> D2 DIN0-

TX_UPOD_L0_P<1> F1 DIN1+

TX_UPOD_L0_N<1> F2 DIN1-

TX_UPOD_L0_P<2> A2 DIN2+

TX_UPOD_L0_N<2> B2 DIN2-

TX_UPOD_L0_P<3> J2 DIN3+

TX_UPOD_L0_N<3> H2 DIN3-

TX_UPOD_L0_P<4> A4 DIN4+

TX_UPOD_L0_N<4> B4 DIN4-

TX_UPOD_L0_P<5> J4 DIN5+

TX_UPOD_L0_N<5> H4 DIN5-

TX_UPOD_L0_P<6> A6 DIN6+

TX_UPOD_L0_N<6> B6 DIN6-

TX_UPOD_L0_P<7> J6 DIN7+

TX_UPOD_L0_N<7> H6 DIN7-

TX_UPOD_L0_P<8> A8 DIN8+

TX_UPOD_L0_N<8> B8 DIN8-

TX_UPOD_L0_P<9> J8 DIN9+

TX_UPOD_L0_N<9> H8 DIN9-

TX_UPOD_L0_P<10> D9 DIN10+

TX_UPOD_L0_N<10> D8 DIN10-

TX_UPOD_L0_P<11> F9 DIN11+

TX_UPOD_L0_N<11> F8 DIN11-

VCC25[3..0] VCC33[3..0] NC[6..0] GND[31..0] INTL_0 INTL_1

TX_UPOD_L0_INTN F5 D5

R158 4.7K

p3v3_left_tx0 p2v5_left_tx0

UPOD_TX_L1

U41

I2C ADD=0X29

TX_UPOD_RESETN F4 RESETL

TX_UPOD_SDA D4 SDA_0

TX_UPOD_SCL E4 SCL_0

TX_UPOD_SDA D6 SDA_1

TX_UPOD_SCL E6 SCL_1

G3 ADDR0

E3 ADDR1

C3 ADDR2

TX_UPOD_L1_P<0> D1 DIN0+

TX_UPOD_L1_N<0> D2 DIN0-

TX_UPOD_L1_P<1> F1 DIN1+

TX_UPOD_L1_N<1> F2 DIN1-

TX_UPOD_L1_P<2> A2 DIN2+

TX_UPOD_L1_N<2> B2 DIN2-

TX_UPOD_L1_P<3> J2 DIN3+

TX_UPOD_L1_N<3> H2 DIN3-

TX_UPOD_L1_P<4> A4 DIN4+

TX_UPOD_L1_N<4> B4 DIN4-

TX_UPOD_L1_P<5> J4 DIN5+

TX_UPOD_L1_N<5> H4 DIN5-

TX_UPOD_L1_P<6> A6 DIN6+

TX_UPOD_L1_N<6> B6 DIN6-

TX_UPOD_L1_P<7> J6 DIN7+

TX_UPOD_L1_N<7> H6 DIN7-

TX_UPOD_L1_P<8> A8 DIN8+

TX_UPOD_L1_N<8> B8 DIN8-

TX_UPOD_L1_P<9> J8 DIN9+

TX_UPOD_L1_N<9> H8 DIN9-

TX_UPOD_L1_P<10> D9 DIN10+

TX_UPOD_L1_N<10> D8 DIN10-

TX_UPOD_L1_P<11> F9 DIN11+

TX_UPOD_L1_N<11> F8 DIN11-

VCC25[3..0] VCC33[3..0] NC[6..0] GND[31..0] INTL_0 INTL_1

TX_UPOD_L1_INTN F5 D5

R159 4.7K

p3v3_left_tx1 p2v5_left_tx1

P3V3 L1 4.7U C479 C481 C483 100N 22U 100N R162 0.5

P2V5 L2 4.7U C480 C482 C484 100N 22U 100N R163 0.5

P3V3 L3 4.7U C485 C487 C489 100N 22U 100N R164 0.5

P2V5 L4 4.7U C486 C488 C490 100N 22U 100N R165 0.5

C447 C448 C449 C450 C451 C452 C453 C454 100N 1.0U

C455 C456 C457 C458 C459 C460 C461 C462 100N 1.0U

UPOD_RX_L0

U33

I2C_ADD=0X34

afbr_78d2sz

RX_UPOD_RESETN F4 RESETL

RX_UPOD_SDA D4 SDA_0

RX_UPOD_SCL E4 SCL_0

RX_UPOD_SDA D6 SDA_1

RX_UPOD_SCL E6 SCL_1

G3 ADDR0

E3 ADDR1

C3 ADDR2

RX_UPOD_L0_P<0> D1 DOUT0+

RX_UPOD_L0_N<0> D2 DOUT0-

RX_UPOD_L0_P<1> F1 DOUT1+

RX_UPOD_L0_N<1> F2 DOUT1-

RX_UPOD_L0_P<2> A2 DOUT2+

RX_UPOD_L0_N<2> B2 DOUT2-

RX_UPOD_L0_P<3> J2 DOUT3+

RX_UPOD_L0_N<3> H2 DOUT3-

RX_UPOD_L0_P<4> A4 DOUT4+

RX_UPOD_L0_N<4> B4 DOUT4-

RX_UPOD_L0_P<5> J4 DOUT5+

RX_UPOD_L0_N<5> H4 DOUT5-

RX_UPOD_L0_P<6> A6 DOUT6+

RX_UPOD_L0_N<6> B6 DOUT6-

RX_UPOD_L0_P<7> J6 DOUT7+

RX_UPOD_L0_N<7> H6 DOUT7-

RX_UPOD_L0_P<8> A8 DOUT8+

RX_UPOD_L0_N<8> B8 DOUT8-

RX_UPOD_L0_P<9> J8 DOUT9+

RX_UPOD_L0_N<9> H8 DOUT9-

RX_UPOD_L0_P<10> D9 DOUT10+

RX_UPOD_L0_N<10> D8 DOUT10-

RX_UPOD_L0_P<11> F9 DOUT11+

RX_UPOD_L0_N<11> F8 DOUT11-

VCC33[3..0] VCC25[3..0] NC[6..0] GND[31..0] INTL_0 INTL_1

RX_UPOD_L0_INTN D5 F5

R147 4.7K

p3v3_left_rx0 p2v5_left_rx0

P3V3 L9 4.7U C106 C108 C121 100N 22U 100N R207 0.5

P2V5 L10 4.7U C107 C109 C122 100N 22U 100N R208 0.5

C386 C387 C388 C389 C390 C391 C392 C393 100N 1.0U

UPOD_RX_L1

U34

I2C_ADD=0X35

afbr_78d2sz

RX_UPOD_RESETN F4 RESETL

RX_UPOD_SDA D4 SDA_0

RX_UPOD_SCL E4 SCL_0

RX_UPOD_SDA D6 SDA_1

RX_UPOD_SCL E6 SCL_1

G3 ADDR0

E3 ADDR1

C3 ADDR2

RX_UPOD_L1_P<0> D1 DOUT0+

RX_UPOD_L1_N<0> D2 DOUT0-

RX_UPOD_L1_P<1> F1 DOUT1+

RX_UPOD_L1_N<1> F2 DOUT1-

RX_UPOD_L1_P<2> A2 DOUT2+

RX_UPOD_L1_N<2> B2 DOUT2-

RX_UPOD_L1_P<3> J2 DOUT3+

RX_UPOD_L1_N<3> H2 DOUT3-

RX_UPOD_L1_P<4> A4 DOUT4+

RX_UPOD_L1_N<4> B4 DOUT4-

RX_UPOD_L1_P<5> J4 DOUT5+

RX_UPOD_L1_N<5> H4 DOUT5-

RX_UPOD_L1_P<6> A6 DOUT6+

RX_UPOD_L1_N<6> B6 DOUT6-

RX_UPOD_L1_P<7> J6 DOUT7+

RX_UPOD_L1_N<7> H6 DOUT7-

RX_UPOD_L1_P<8> A8 DOUT8+

RX_UPOD_L1_N<8> B8 DOUT8-

RX_UPOD_L1_P<9> J8 DOUT9+

RX_UPOD_L1_N<9> H8 DOUT9-

RX_UPOD_L1_P<10> D9 DOUT10+

RX_UPOD_L1_N<10> D8 DOUT10-

RX_UPOD_L1_P<11> F9 DOUT11+

RX_UPOD_L1_N<11> F8 DOUT11-

VCC33[3..0] VCC25[3..0] NC[6..0] GND[31..0] INTL_0 INTL_1

RX_UPOD_L1_INTN D5 F5

R148 4.7K

p3v3_left_rx1 p2v5_left_rx1

P3V3 L11 4.7U C123 C541 C543 100N 22U 100N R209 0.5

P2V5 L12 4.7U C124 C542 C544 100N 22U 100N R210 0.5

C394 C395 C396 C397 C398 C399 C400 C401 100N 1.0U

ymca_card_v0

MODIFIE: Mon Mar 23 09:50:40 2015

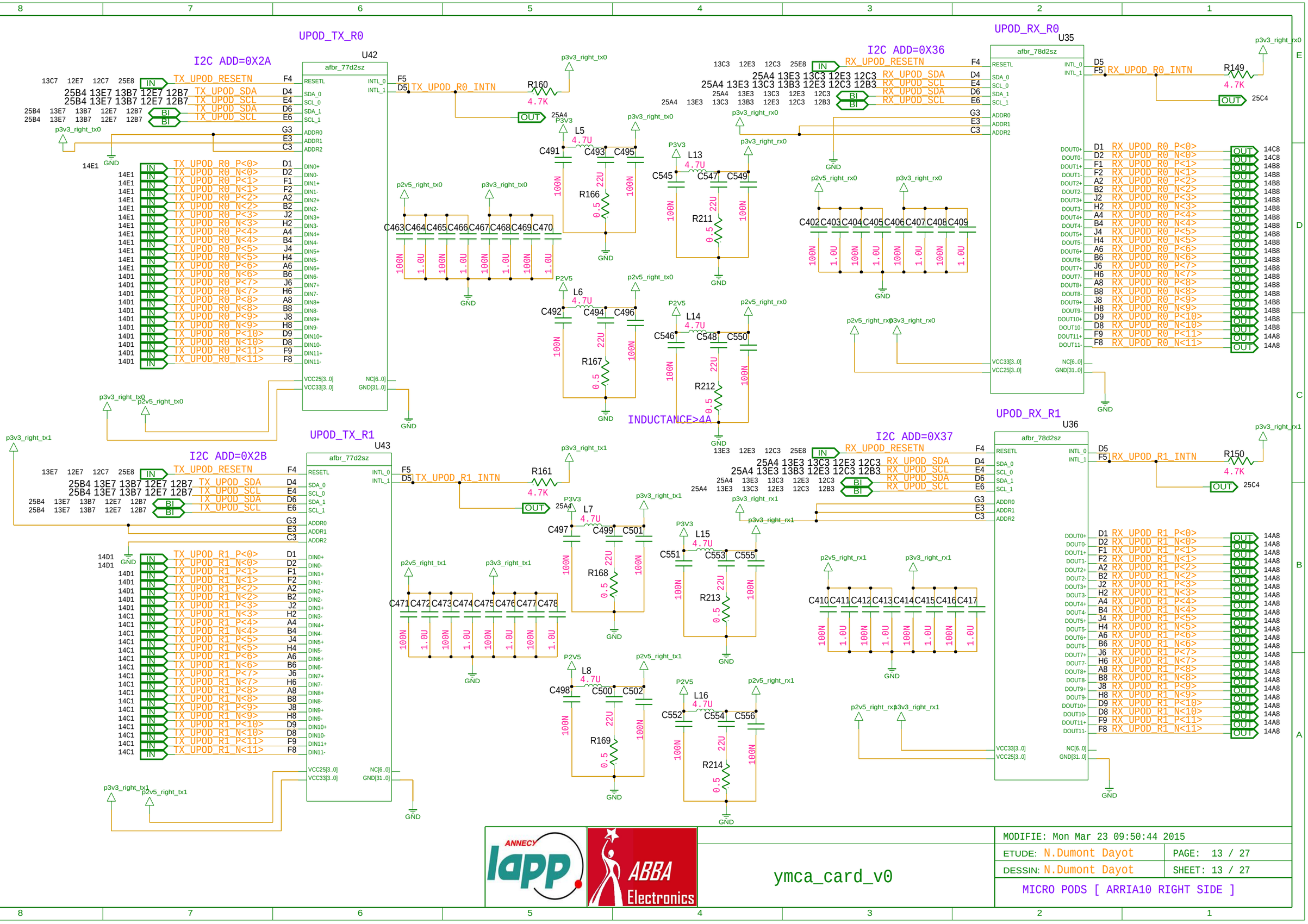
ETUDE: N.Dumont Dayot

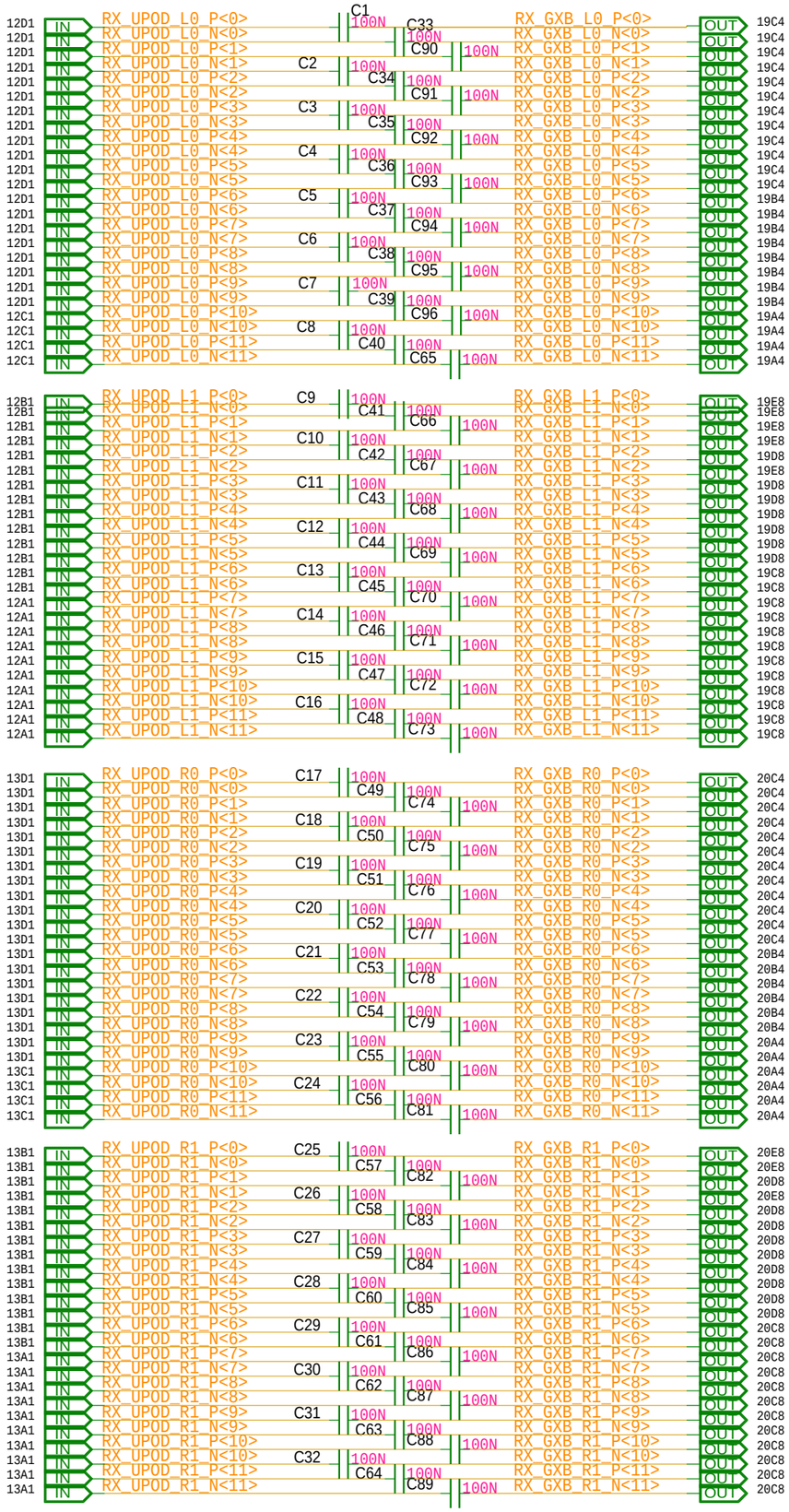
PAGE: 12 / 27

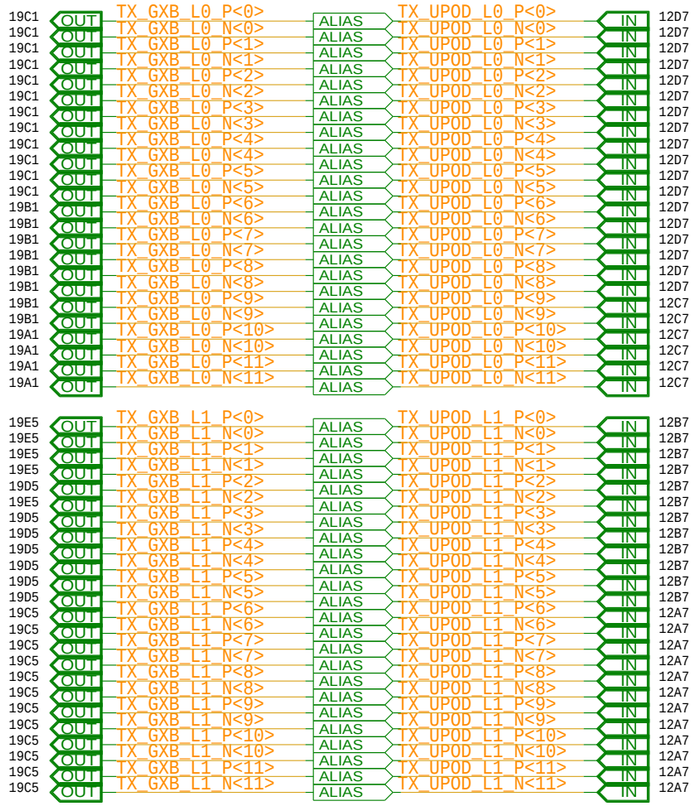
DESSIN: N.Dumont Dayot

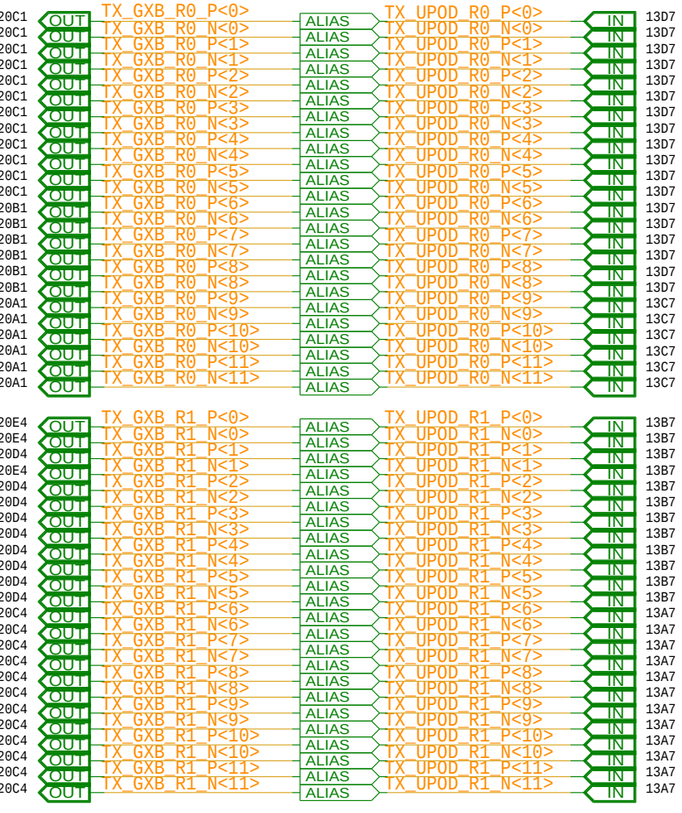
SHEET: 12 / 27

MICRO PODS [ARRIA10 LEFT SIDE]


UPOD_TX_R0
I2C ADD=0X2A
U42
afbr_77d2sz
TX_UPOD_RESETN
TX_UPOD_SDA
TX_UPOD_SCL
TX_UPOD_R0_P<0>
TX_UPOD_R0_N<0>
TX_UPOD_R0_P<1>
TX_UPOD_R0_N<1>
TX_UPOD_R0_P<2>
TX_UPOD_R0_N<2>
TX_UPOD_R0_P<3>
TX_UPOD_R0_N<3>
TX_UPOD_R0_P<4>
TX_UPOD_R0_N<4>
TX_UPOD_R0_P<5>
TX_UPOD_R0_N<5>
TX_UPOD_R0_P<6>
TX_UPOD_R0_N<6>
TX_UPOD_R0_P<7>
TX_UPOD_R0_N<7>
TX_UPOD_R0_P<8>
TX_UPOD_R0_N<8>
TX_UPOD_R0_P<9>
TX_UPOD_R0_N<9>
TX_UPOD_R0_P<10>
TX_UPOD_R0_N<10>
TX_UPOD_R0_P<11>
TX_UPOD_R0_N<11>
TX_UPOD_R0_INTN
R160
4.7K
L5
4.7U
L6
4.7U
R166
R167
INDUCTANCE>4A
UPOD_RX_R0
U35
I2C ADD=0X36
RX_UPOD_RESETN
RX_UPOD_SDA
RX_UPOD_SCL
RX_UPOD_R0_INTN
R149
4.7K
L13
4.7U
L14
4.7U
R211
R212
UPOD_TX_R1
U43
I2C ADD=0X2B
TX_UPOD_R1_INTN
R161
4.7K
L7
4.7U
L8
4.7U
R168
R169
UPOD_RX_R1
U36
I2C ADD=0X37
RX_UPOD_R1_INTN
R150
4.7K
L15
4.7U
L16
4.7U
R213
R214
GND
P3V3
P2V5
ANNECY
IAPP
ABBA Electronics
ymca_card_v0
MODIFIE: Mon Mar 23 09:50:44 2015
ETUDE: N.Dumont Dayot
PAGE: 13 / 27
DESSIN: N.Dumont Dayot
SHEET: 13 / 27
MICRO PODS [ARRIA10 RIGHT SIDE]







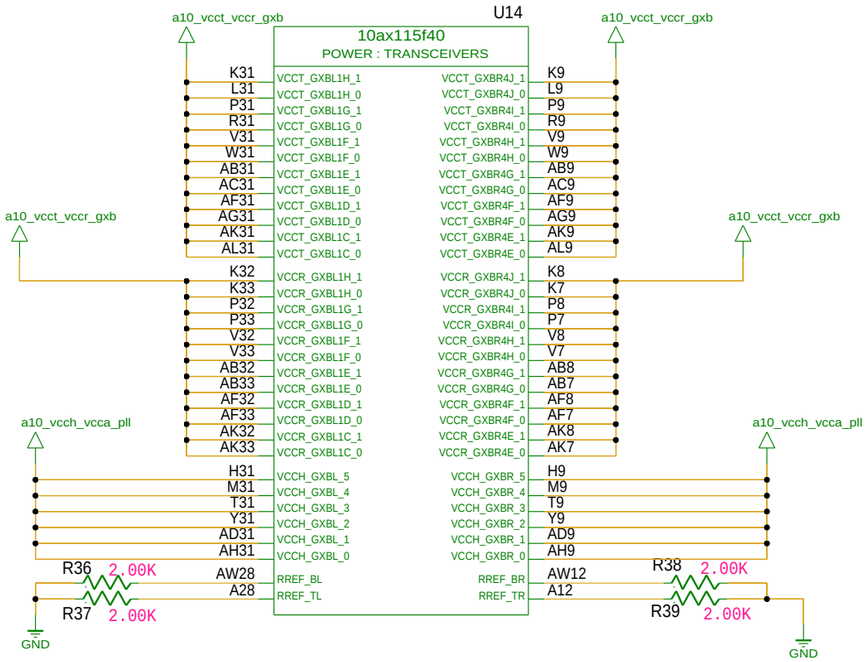
ymca_card_v0

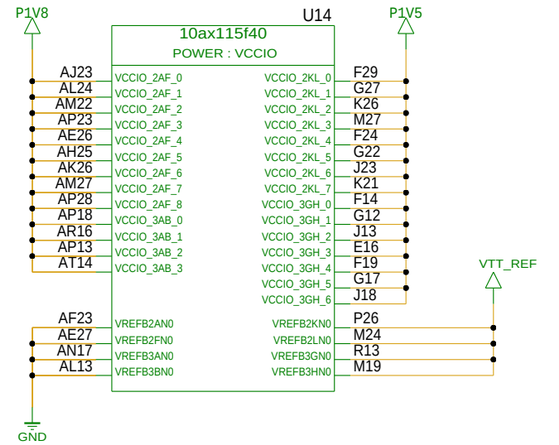
MODIFIE: Mon Mar 23 09:50:45 2015

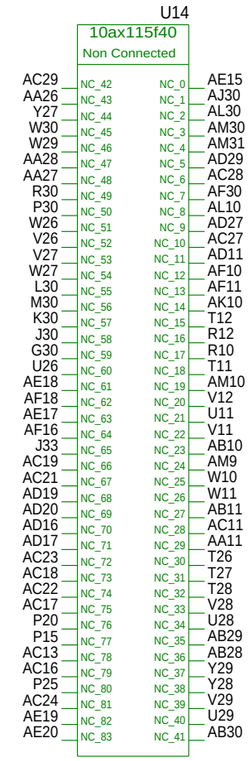
ETUDE: N.Dumont Dayot | PAGE: 14 / 27

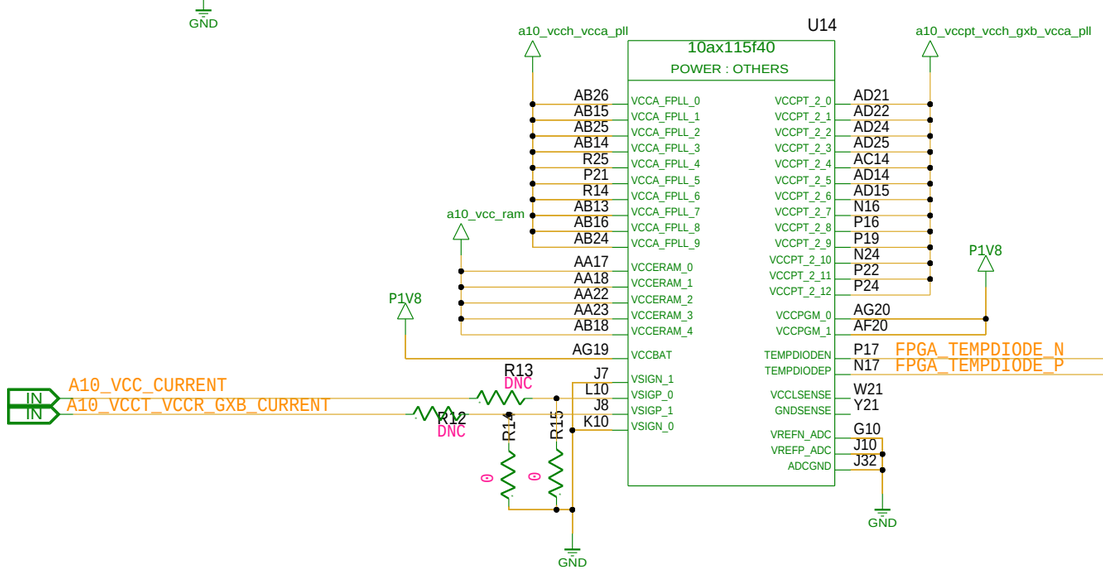
DESSIN: N.Dumont Dayot | SHEET: 14 / 27

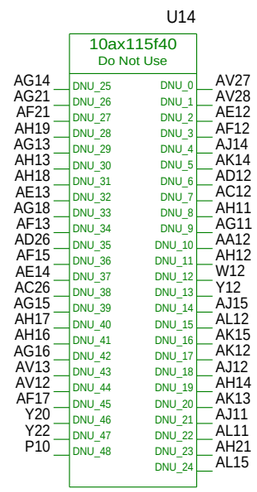
UPOD TO ARRIA10 CONNECTIONS











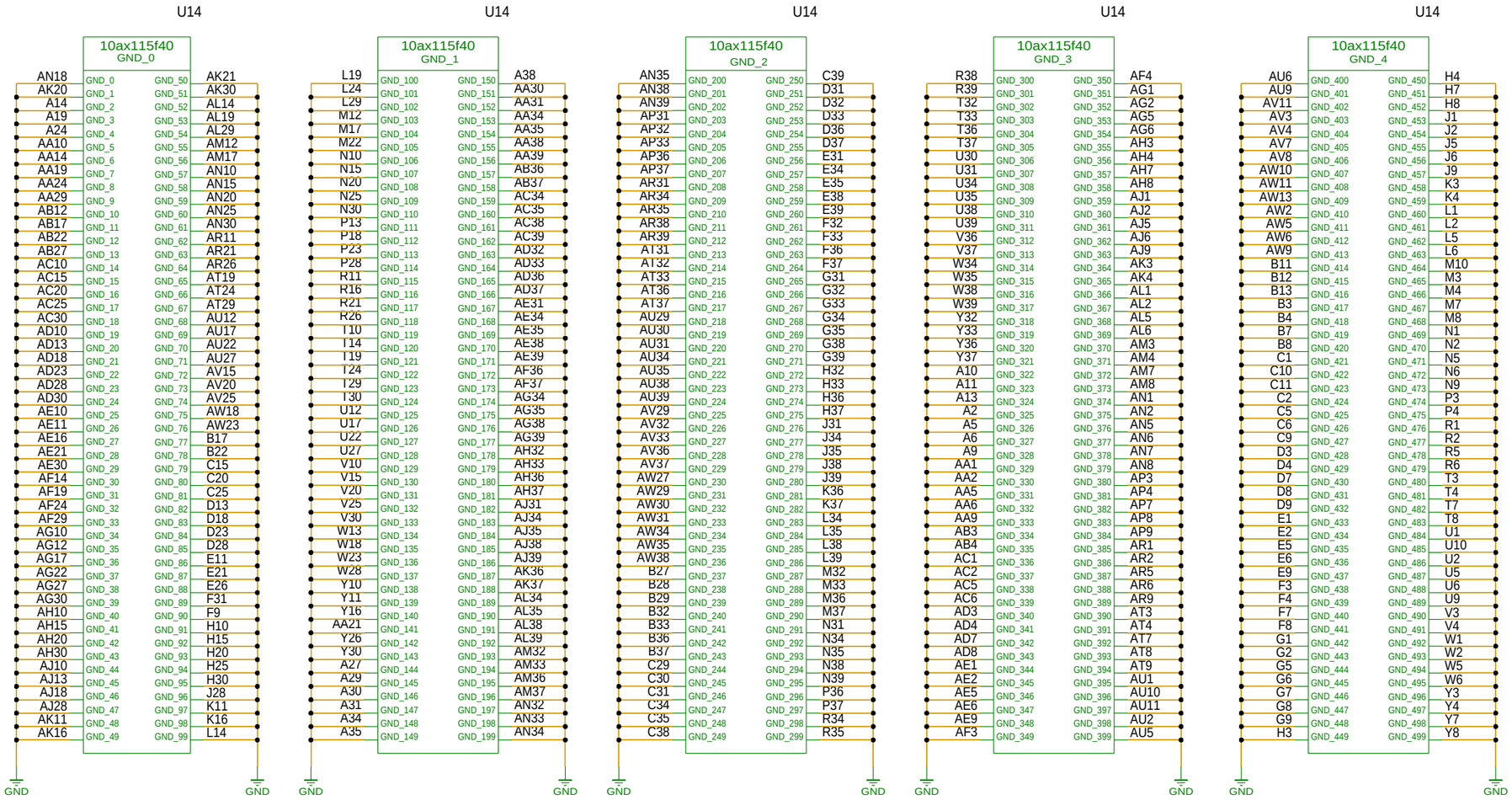
ASSUMPTION : BANK 2KL[1.5V]=DDR3_0
ASSUMPTION : BANK 3GH[1.5V]=DDR3_1
ASSUMPTION : BANK 3AB[1.8V]=OUTPUT TEST PINS,AMC_ID
ASSUMPTION : BANK 2AF[1.8V]=IO

VSIG : EXTERNAL VOLTAGE SENSOR IF NEEDED
DO NOT DRIVE UNTIL VCCA_PLL HAS REACHED 1.62V
TIED TO GND IF NOT USED=DEFAULT CONFIG

VREFNADC:INTERNAL REF WHEN TIED TO GND

ymca_card_v0

MODIFIE: Mon Mar 23 09:50:40 2015
ETUDE: N.Dumont Dayot
PAGE: 15 / 27
DESSIN: N.Dumont Dayot
SHEET: 15 / 27
ARRIA10 : POWER AND NC



ymca_card_v0

MODIFIE: Mon Mar 23 09:50:46 2015

ETUDE: N.Dumont Dayot | PAGE: 16 / 27

DESSIN: N.Dumont Dayot | SHEET: 16 / 27

ARRIA10:GROUND

A10 VCC DECOUPLING

a10_vcc

C191 C196 C201 C206 C211 C216 C221 C226 C231 C236 C239 C242 C245 C248 C250 C252 C254 C256
100U 100U 100U 100U 100U 100U 10U 10U 10U 10U 10U 10U 1.0U 1.0U 1.0U 1.0U 1.0U 1.0U

C192 C197 C202 C207 C212 C217 C222 C227 C232 C237 C240 C243 C246 C249 C251 C253 C255 C257
100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N

FPGA POWER DECOUPLING

C523 C524 C525 C526 C527 C528 C529 C530 C531 C532 C533 C534 C535 C536 C537 C538 C539 C540
10N 10N 10N 10N 10N 10N 10N 10N 10N 1.0N 1.0N 1.0N 1.0N 1.0N 1.0N 1.0N 1.0N 1.0N

GND

A10 VCCT_GXB AND VCCR_GXB DECOUPLING

a10_vcct_vccr_gxb

C260 C265 C270 C275 C280 C285 C290 C295 C300 C305 C308 C311 C314 C317 C320 C323 C326 C329
100U 100U 100U 100U 100U 100U 10U 10U 10U 10U 10U 10U 1.0U 1.0U 1.0U 1.0U 1.0U 1.0U

C261 C266 C271 C276 C281 C286 C291 C296 C301 C306 C309 C312 C315 C318 C321 C324 C327 C330
100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N

C262 C267 C272 C277 C282 C287 C292 C297 C302 C307 C310 C313 C316 C319 C322 C325 C328 C331
10N 10N 10N 10N 10N 10N 10N 10N 10N 1.0N 1.0N 1.0N 1.0N 1.0N 1.0N 1.0N 1.0N 1.0N

GND

A10 VCCRAM DECOUPLING

a10_vcc_ram

C332 C333 C334 C335 C336 C337
100N 100N 100N 100N 100N 100N

GND

A10 VCCPT VCCH_GXB VCCA_PLL DECOUPLING

a10_vcch_vcca_pll

a10_vccpt_vcch_gxb_vcca_pll

C193 C198 C203 C208 C213 C218 C223 C228 C233
100U 100U 100U 100U 10U 10U 10U 10U 10U

C194 C199 C204 C209 C214 C219 C224 C229 C234 C238 C241 C244 C247
100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N

C195 C200 C205 C210 C215 C220 C225 C230 C235
10N 10N 10N 10N 10N 10N 10N 10N 10N

GND

A10 P1V8 DECOUPLING

P1V8

C258 C263 C268 C273 C278 C283 C288 C293 C298 C303
100N 100N 100N 100N 100N 100N 100N 100N 100N 100N

GND

A10 P1V5 DECOUPLING

P1V5

C259 C264 C269 C274 C279 C284 C289 C294 C299 C304
100N 100N 100N 100N 100N 100N 100N 100N 100N 100N

GND

ANNECY lapp ABBA Electronics

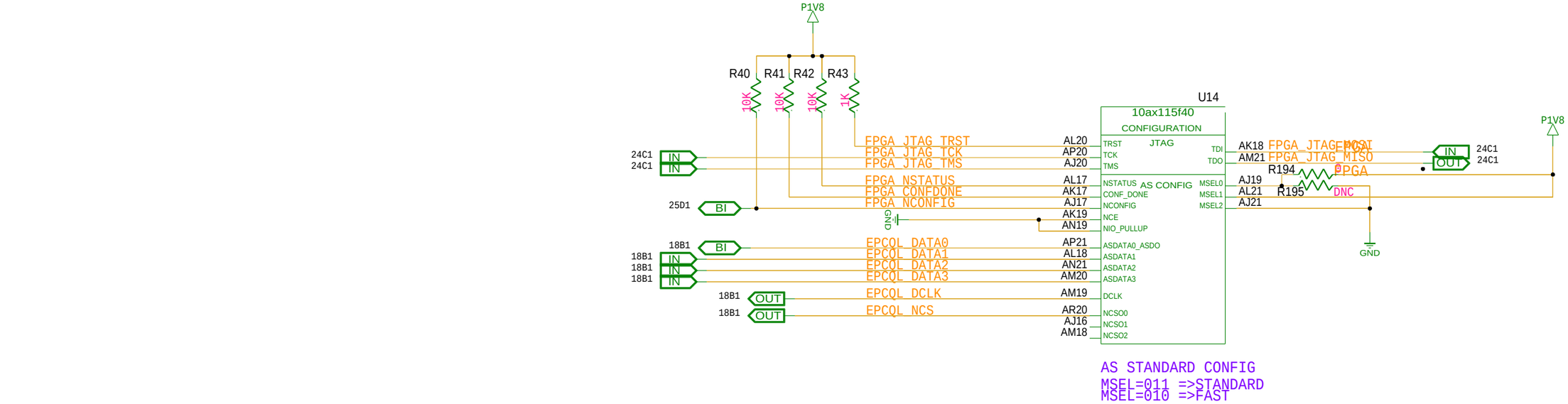
ymca_card_v0

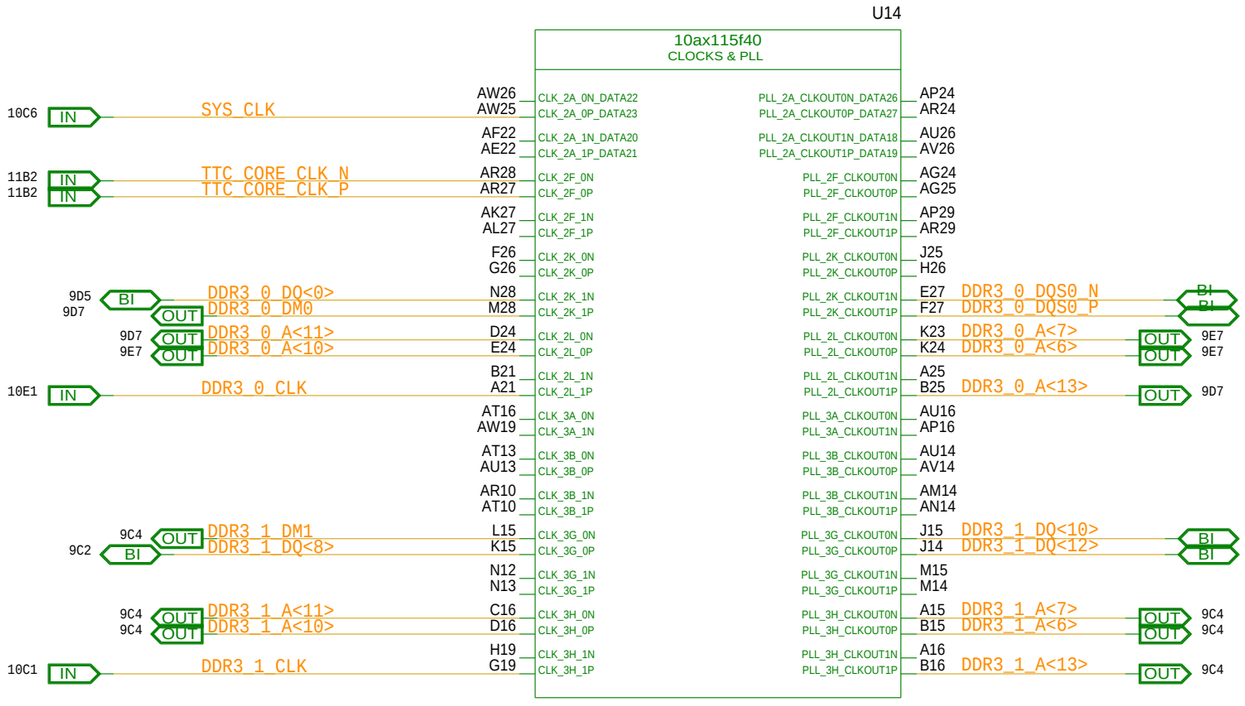
MODIFIE: Mon Mar 23 09:50:46 2015

ETUDE: N.Dumont Dayot | PAGE: 17 / 27

DESSIN: N.Dumont Dayot | SHEET: 17 / 27

ARRIA10 DECOUPLING





DDR3 REF CLOCKS SHOULD HAVE THE FREQUENCY GIVEN BYMGWZ
DDR3 REF CLOCKS COME FROM INTERNAL FPGA PLL (IO 1.5V)

LVDS IO : 0.247<VOD<0.6 1.125<VOCM<1.375 VOCM=1.25 TYPICAL

ANNECY lapp — ABBA Electronics

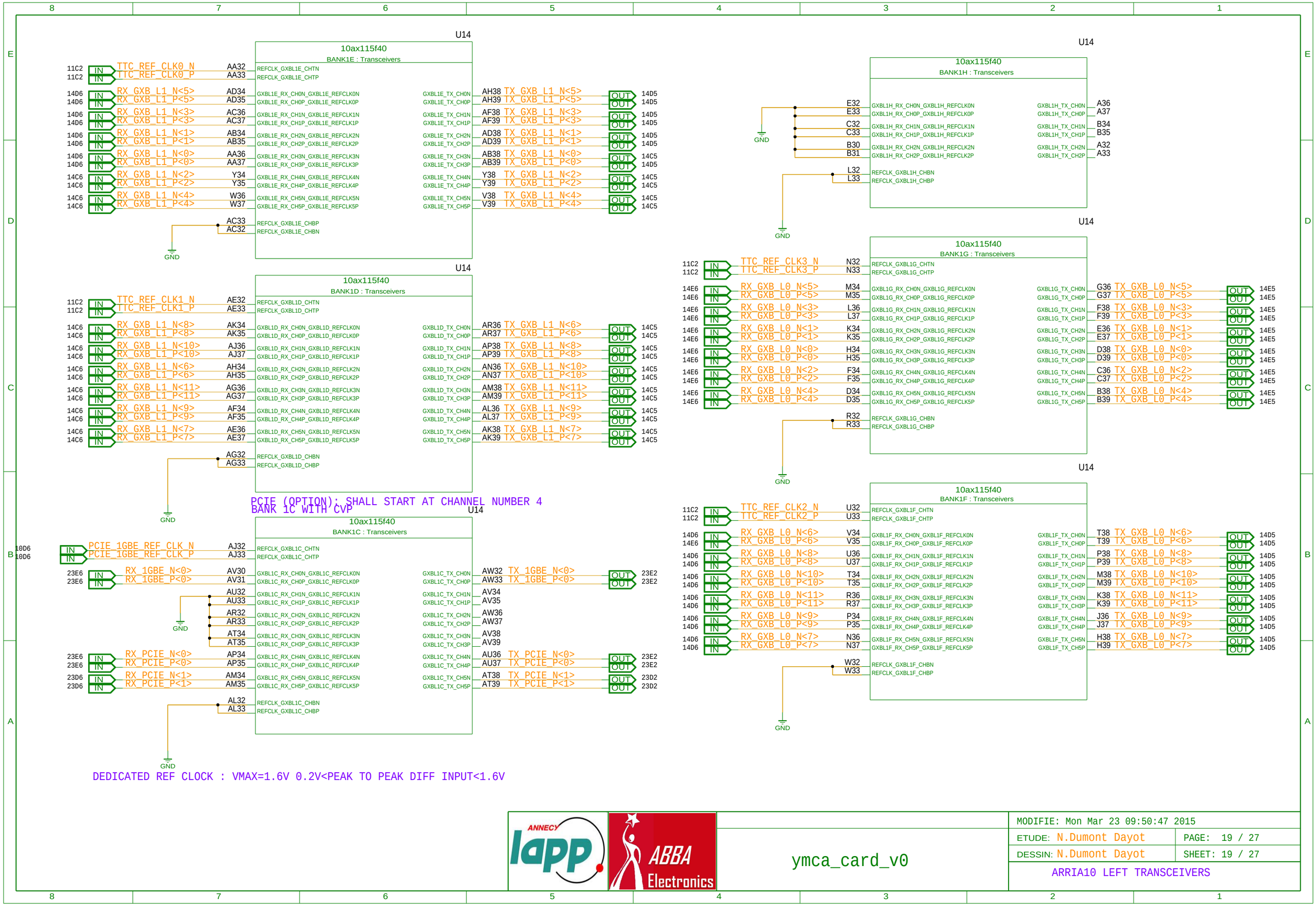
ymca_card_v0

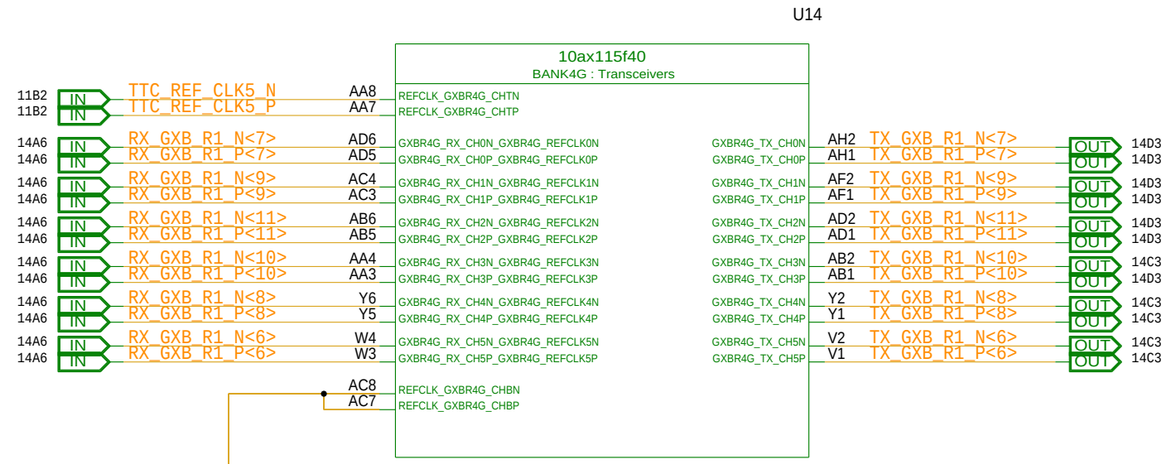
MODIFIE: Mon Mar 23 09:50:41 2015

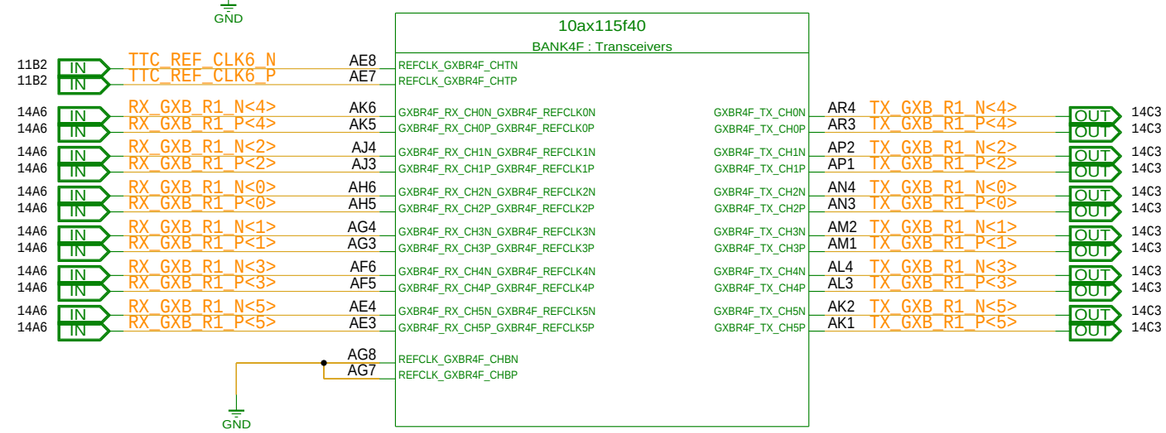
ETUDE: N.Dumont Dayot | PAGE: 18 / 27

DESSIN: N.Dumont Dayot | SHEET: 18 / 27

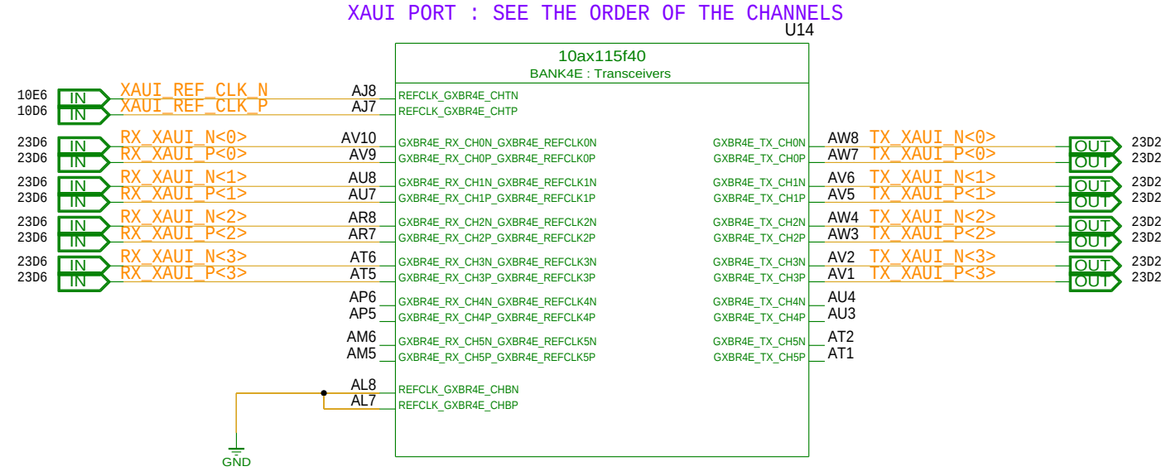
ARRIA10 CLOCKS AND CONFIGURATION

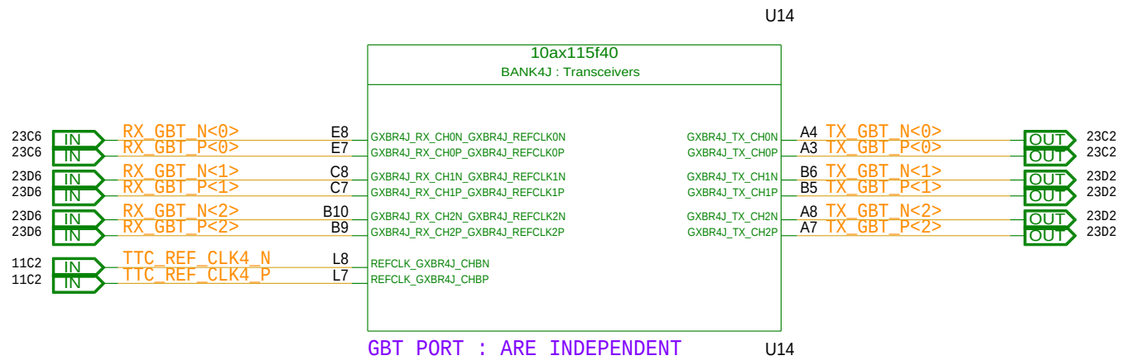

U14
10ax115f40
BANK1E : Transceivers
TTC_REF_CLK0_N
TTC_REF_CLK0_P
RX_GXB_L1_N<5>
RX_GXB_L1_P<5>
RX_GXB_L1_N<3>
RX_GXB_L1_P<3>
RX_GXB_L1_N<1>
RX_GXB_L1_P<1>
RX_GXB_L1_N<0>
RX_GXB_L1_P<0>
RX_GXB_L1_N<2>
RX_GXB_L1_P<2>
RX_GXB_L1_N<4>
RX_GXB_L1_P<4>
TX_GXB_L1_N<5>
TX_GXB_L1_P<5>
TX_GXB_L1_N<3>
TX_GXB_L1_P<3>
TX_GXB_L1_N<1>
TX_GXB_L1_P<1>
TX_GXB_L1_N<0>
TX_GXB_L1_P<0>
TX_GXB_L1_N<2>
TX_GXB_L1_P<2>
TX_GXB_L1_N<4>
TX_GXB_L1_P<4>
GND
U14
10ax115f40
BANK1H : Transceivers
GND
U14
10ax115f40
BANK1G : Transceivers
TTC_REF_CLK3_N
TTC_REF_CLK3_P
RX_GXB_L0_N<5>
RX_GXB_L0_P<5>
RX_GXB_L0_N<3>
RX_GXB_L0_P<3>
RX_GXB_L0_N<1>
RX_GXB_L0_P<1>
RX_GXB_L0_N<0>
RX_GXB_L0_P<0>
RX_GXB_L0_N<2>
RX_GXB_L0_P<2>
RX_GXB_L0_N<4>
RX_GXB_L0_P<4>
TX_GXB_L0_N<5>
TX_GXB_L0_P<5>
TX_GXB_L0_N<3>
TX_GXB_L0_P<3>
TX_GXB_L0_N<1>
TX_GXB_L0_P<1>
TX_GXB_L0_N<0>
TX_GXB_L0_P<0>
TX_GXB_L0_N<2>
TX_GXB_L0_P<2>
TX_GXB_L0_N<4>
TX_GXB_L0_P<4>
GND
U14
10ax115f40
BANK1D : Transceivers
TTC_REF_CLK1_N
TTC_REF_CLK1_P
RX_GXB_L1_N<8>
RX_GXB_L1_P<8>
RX_GXB_L1_N<10>
RX_GXB_L1_P<10>
RX_GXB_L1_N<6>
RX_GXB_L1_P<6>
RX_GXB_L1_N<11>
RX_GXB_L1_P<11>
RX_GXB_L1_N<9>
RX_GXB_L1_P<9>
RX_GXB_L1_N<7>
RX_GXB_L1_P<7>
TX_GXB_L1_N<6>
TX_GXB_L1_P<6>
TX_GXB_L1_N<8>
TX_GXB_L1_P<8>
TX_GXB_L1_N<10>
TX_GXB_L1_P<10>
TX_GXB_L1_N<11>
TX_GXB_L1_P<11>
TX_GXB_L1_N<9>
TX_GXB_L1_P<9>
TX_GXB_L1_N<7>
TX_GXB_L1_P<7>
GND
U14
10ax115f40
BANK1F : Transceivers
TTC_REF_CLK2_N
TTC_REF_CLK2_P
RX_GXB_L0_N<6>
RX_GXB_L0_P<6>
RX_GXB_L0_N<8>
RX_GXB_L0_P<8>
RX_GXB_L0_N<10>
RX_GXB_L0_P<10>
RX_GXB_L0_N<11>
RX_GXB_L0_P<11>
RX_GXB_L0_N<9>
RX_GXB_L0_P<9>
RX_GXB_L0_N<7>
RX_GXB_L0_P<7>
TX_GXB_L0_N<6>
TX_GXB_L0_P<6>
TX_GXB_L0_N<8>
TX_GXB_L0_P<8>
TX_GXB_L0_N<10>
TX_GXB_L0_P<10>
TX_GXB_L0_N<11>
TX_GXB_L0_P<11>
TX_GXB_L0_N<9>
TX_GXB_L0_P<9>
TX_GXB_L0_N<7>
TX_GXB_L0_P<7>
GND
PCIE (OPTION): SHALL START AT CHANNEL NUMBER 4
BANK 1C WITH CVP
U14
10ax115f40
BANK1C : Transceivers
PCIE_1GBE_REF_CLK_N
PCIE_1GBE_REF_CLK_P
RX_1GBE_N<0>
RX_1GBE_P<0>
TX_1GBE_N<0>
TX_1GBE_P<0>
RX_PCIE_N<0>
RX_PCIE_P<0>
RX_PCIE_N<1>
RX_PCIE_P<1>
TX_PCIE_N<0>
TX_PCIE_P<0>
TX_PCIE_N<1>
TX_PCIE_P<1>
GND
DEDICATED REF CLOCK : VMAX=1.6V 0.2V<PEAK TO PEAK DIFF INPUT<1.6V
ANNECY
lapp
ABBA
Electronics
ymca_card_v0
MODIFIE: Mon Mar 23 09:50:47 2015
ETUDE: N.Dumont Dayot
PAGE: 19 / 27
DESSIN: N.Dumont Dayot
SHEET: 19 / 27
ARRIA10 LEFT TRANSCEIVERS



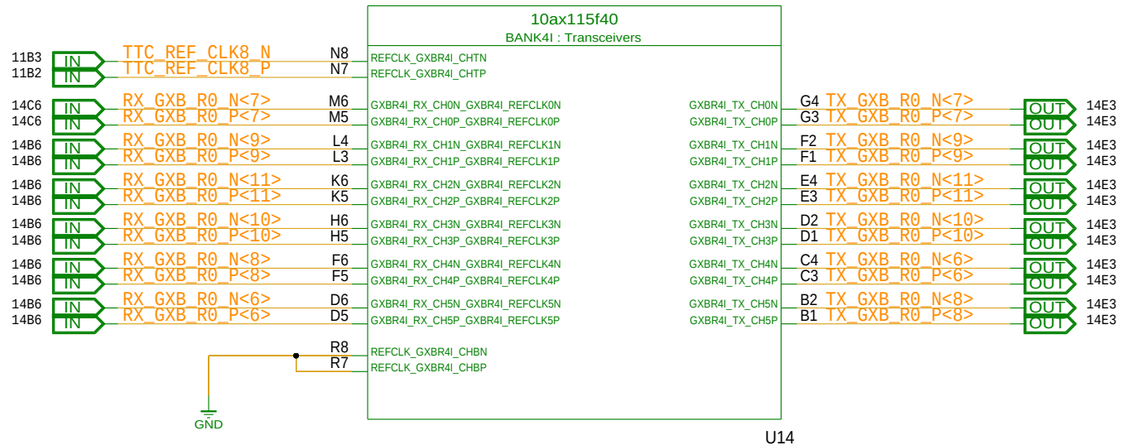


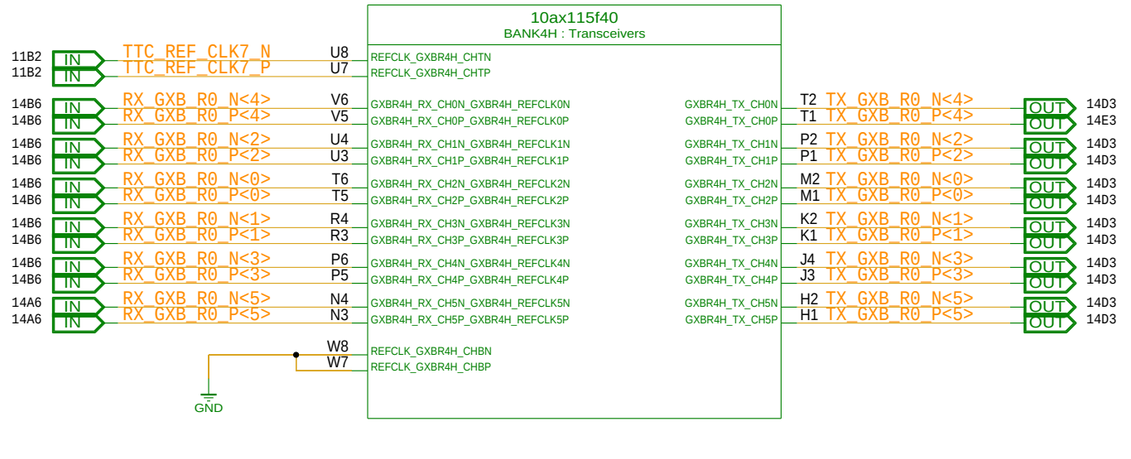
XAUI PORT : SEE THE ORDER OF THE CHANNELS





GBT PORT : ARE INDEPENDENT





ymca_card_v0

MODIFIE: Mon Mar 23 09:50:47 2015

ETUDE: N.Dumont Dayot | PAGE: 20 / 27

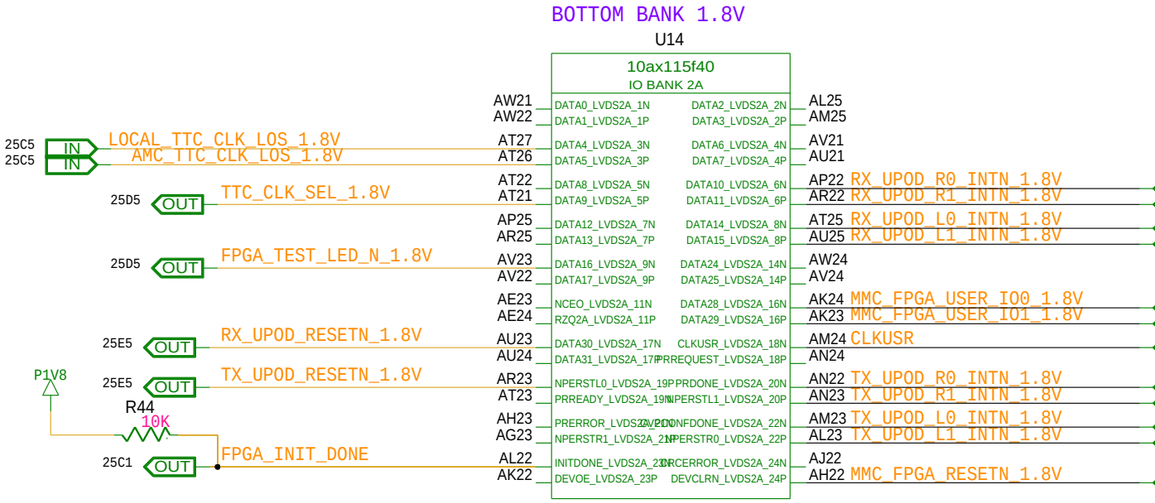
DESSIN: N.Dumont Dayot | SHEET: 20 / 27

ARRIA10 RIGHT TRANSCEIVERS

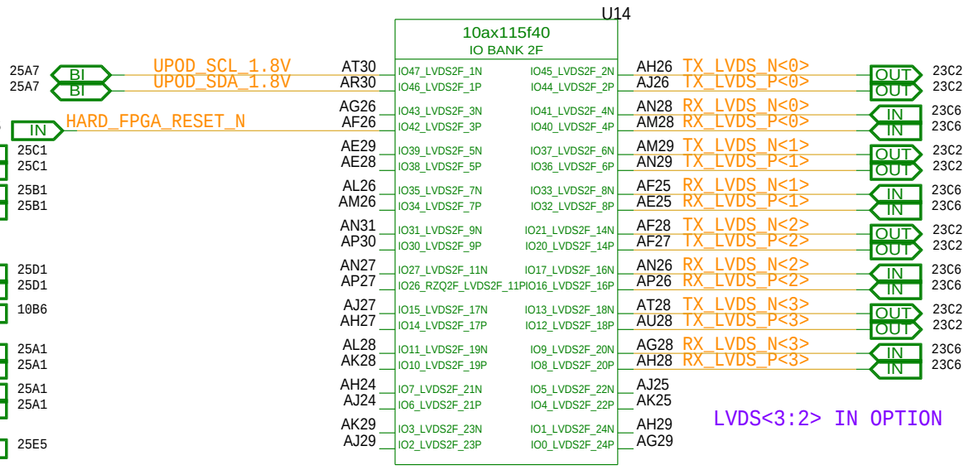
PUT PRREQUEST AT 0 IF NOT USED

SOFT CDR ON RX LVDS ONLY ON PINS WITH EVEN NUMBER

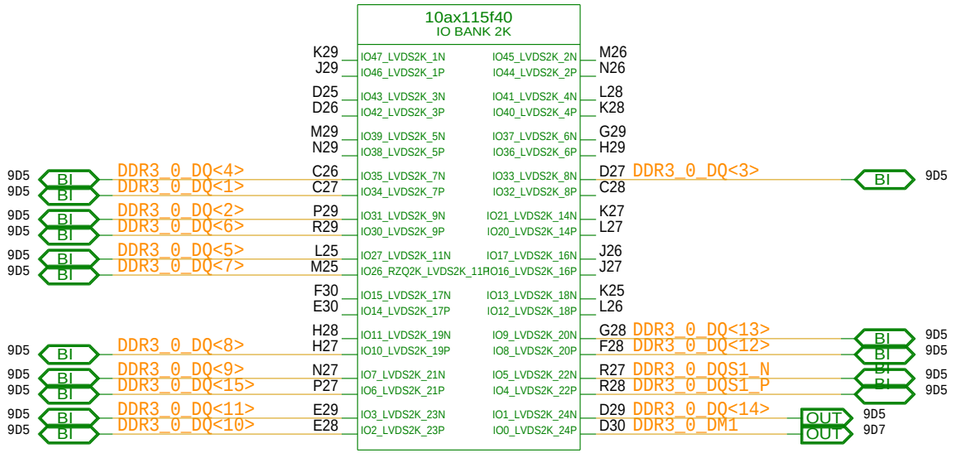
BOTTOM BANK 1.8V



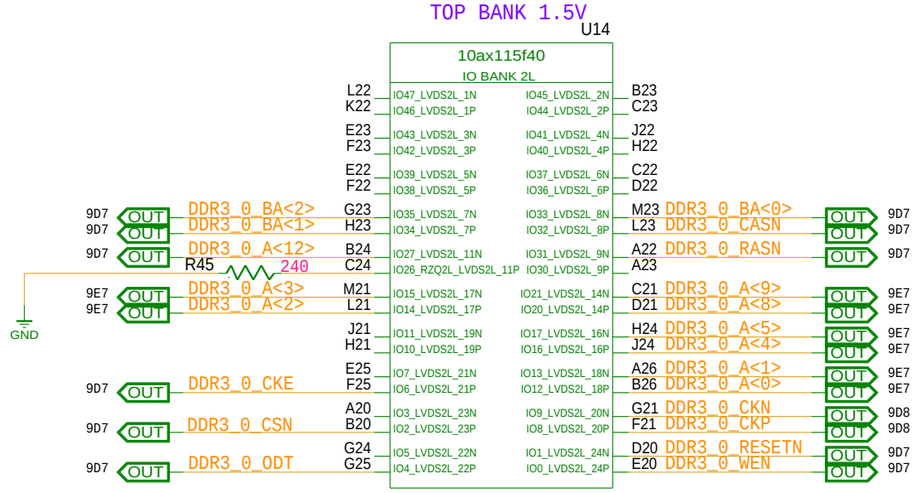
BOTTOM BANK 1.8V



TOP BANK 1.5V



TOP BANK 1.5V



BANK 2K : DDR3_0 DATA PINS
DQS AND DQ IN SAME IO LANE : COULD BE CHANGED

BANK 2L : DDR3_0 ADRESS/COMMAND PINS
A/C PIN PLACEMENT IS FIXED

SEE ARRIA 10EMIF GUIDELINES FOR PLACEMENT RULES
DDR3 PLACEMENT CONFIRMED WITH QUARTUS (PCB CONSTRAINTS PG.74....)

ymca_card_v0

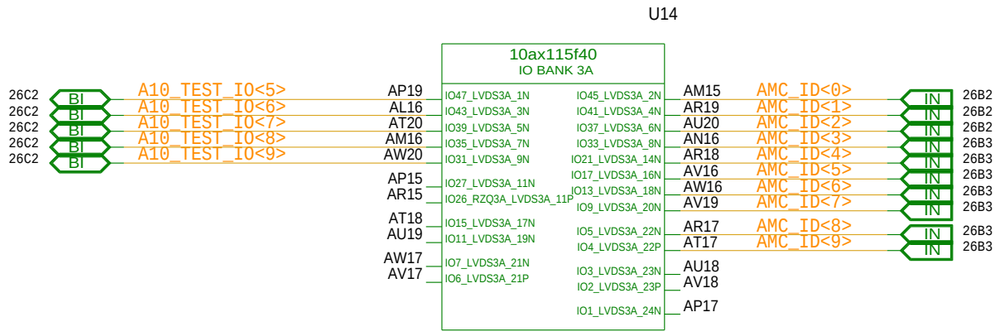
MODIFIE: Mon Mar 23 09:50:41 2015

ETUDE: N.Dumont Dayot | PAGE: 21 / 27

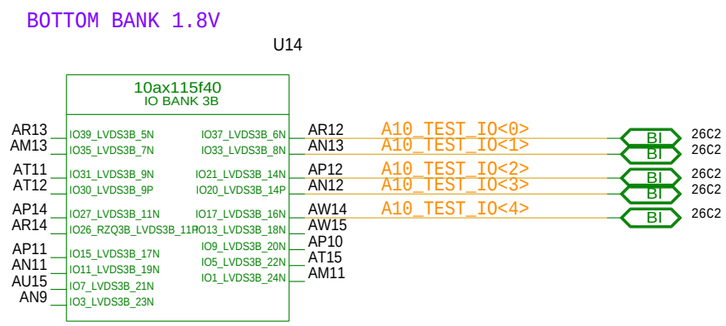
DESSIN: N.Dumont Dayot | SHEET: 21 / 27

ARRIA10 : BANK 2A,2F,2K,2L

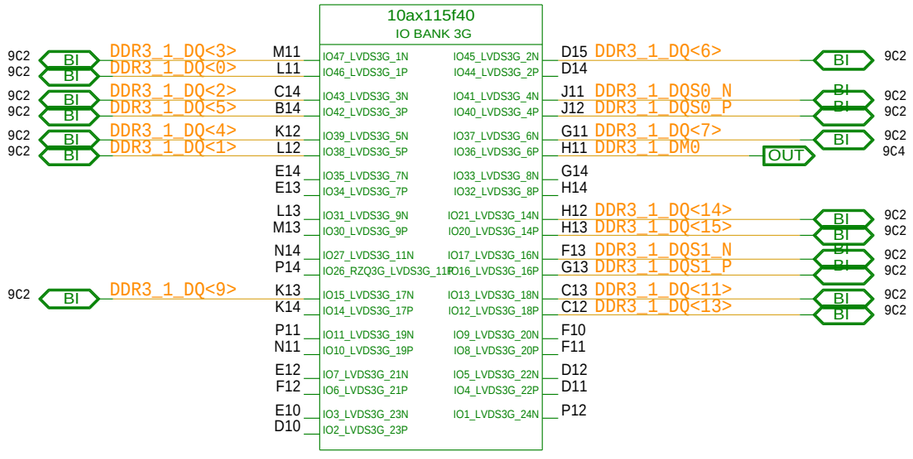
BOTTOM BANK 1.8V



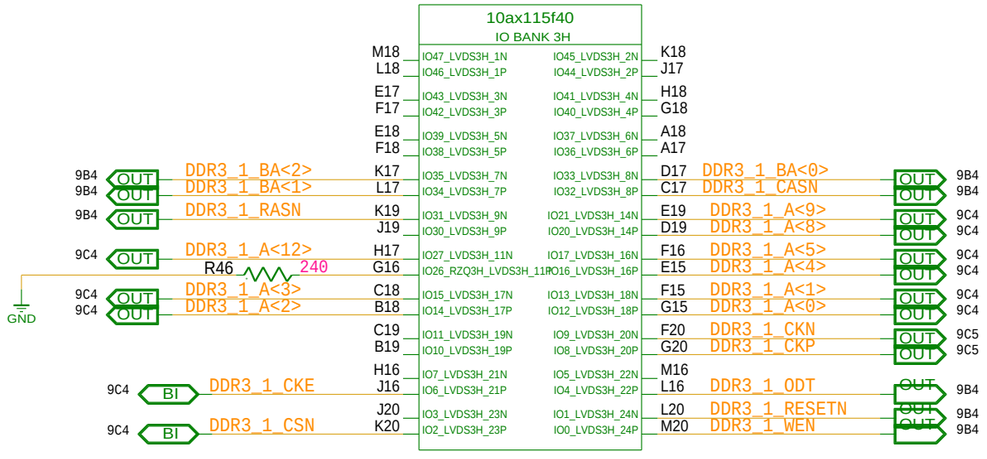
BOTTOM BANK 1.8V



TOP BANK 1.5V



TOP BANK 1.5V



BANK 3G : DDR3_0 DATA PINS
DQS AND DQ IN SAME IO LANE : COULD BE CHANGED

BANK 3H : DDR3_0 ADRESS/COMMAND PINS
A/C PIN PLACEMENT IS FIXED

SEE ARRIA 10EMIF GUIDELINES FOR PLACEMENT RULES

DDR3 PLACEMENT CONFIRMED WITH QUARTUS (PCB CONSTRAINTS PG.74....)

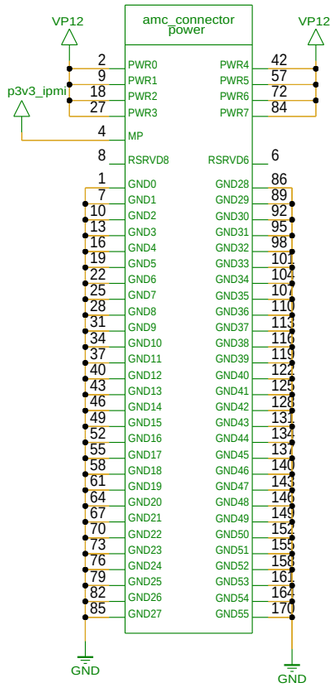
ymca_card_v0

MODIFIE: Mon Mar 23 09:50:42 2015

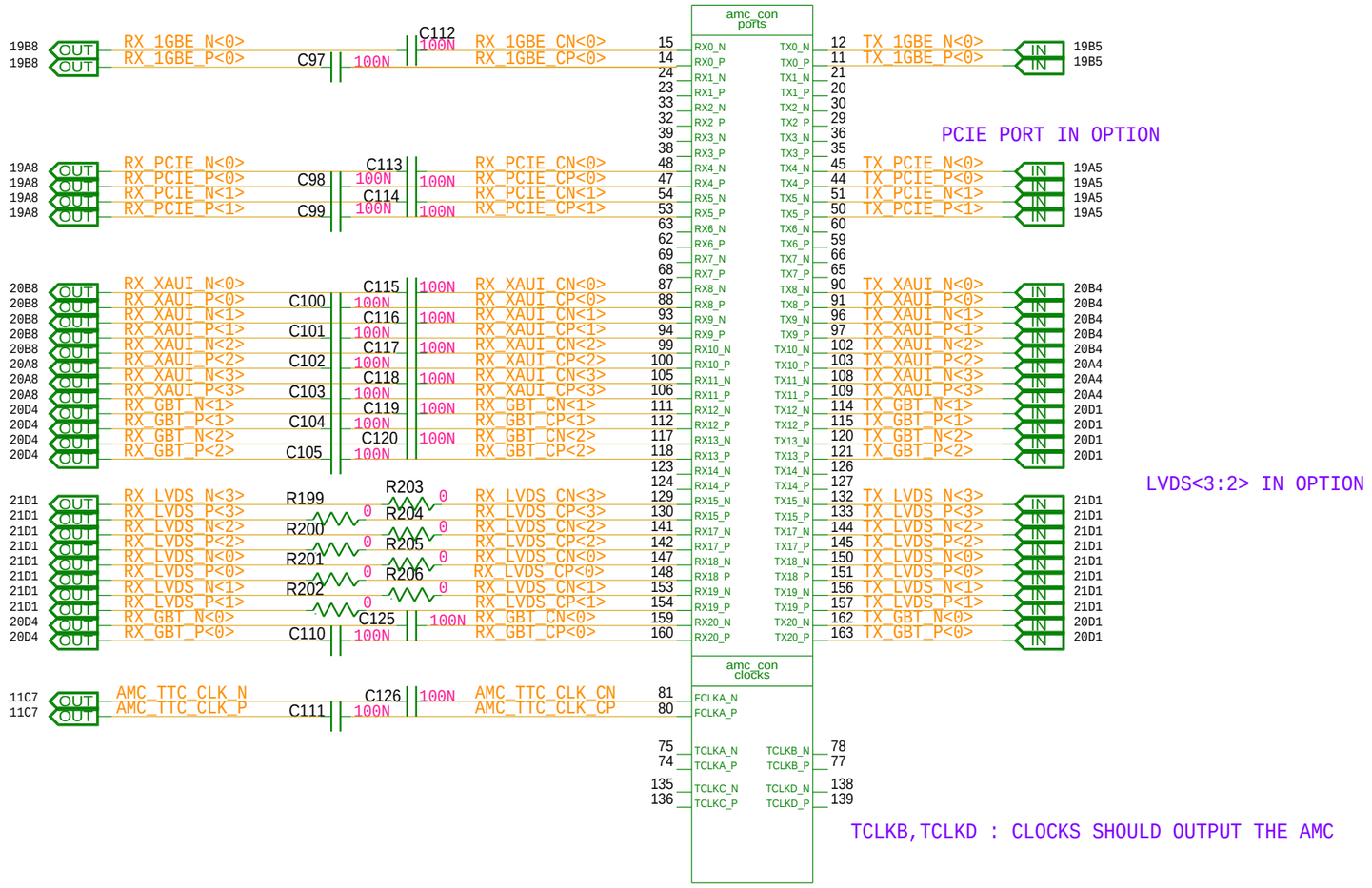
ETUDE: N.Dumont Dayot | PAGE: 22 / 27

DESSIN: N.Dumont Dayot | SHEET: 22 / 27

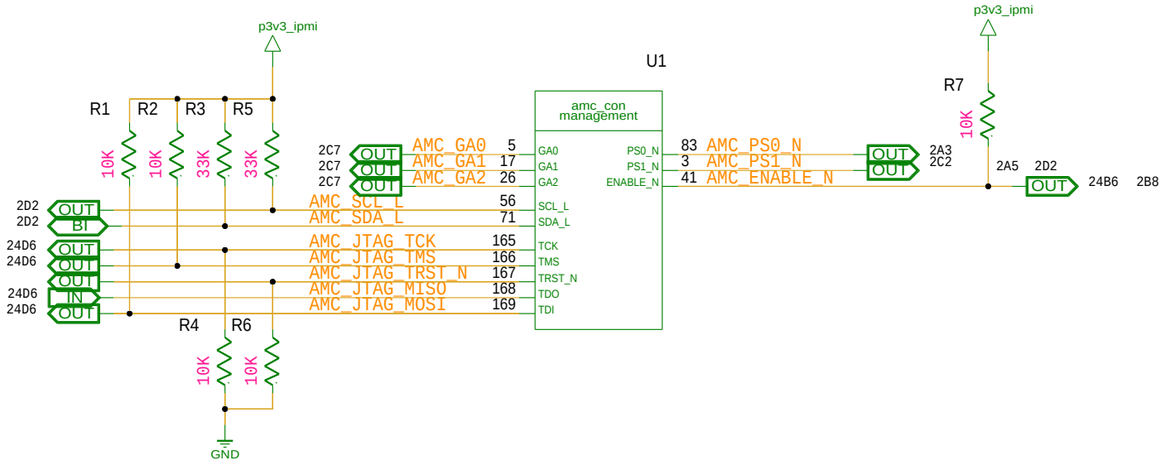
U1



U1

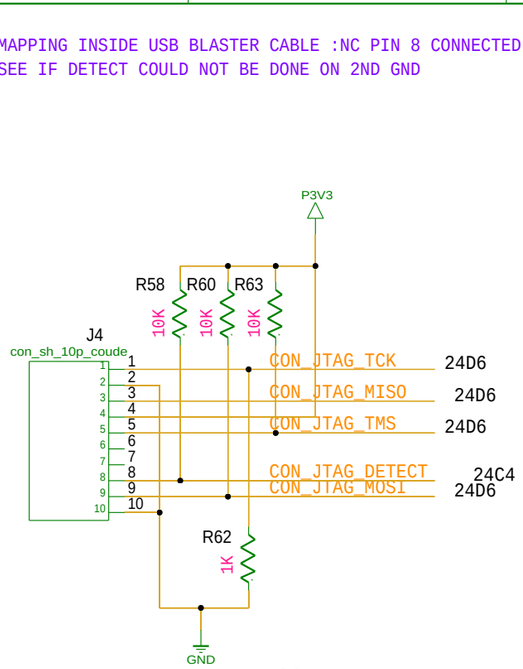


COMMON OPTION REGION : PORTS 0-3
FAT PIPES REGION : PORTS 4-11
EXTENDED OPTION REGION : PORTS 12-15,17-20

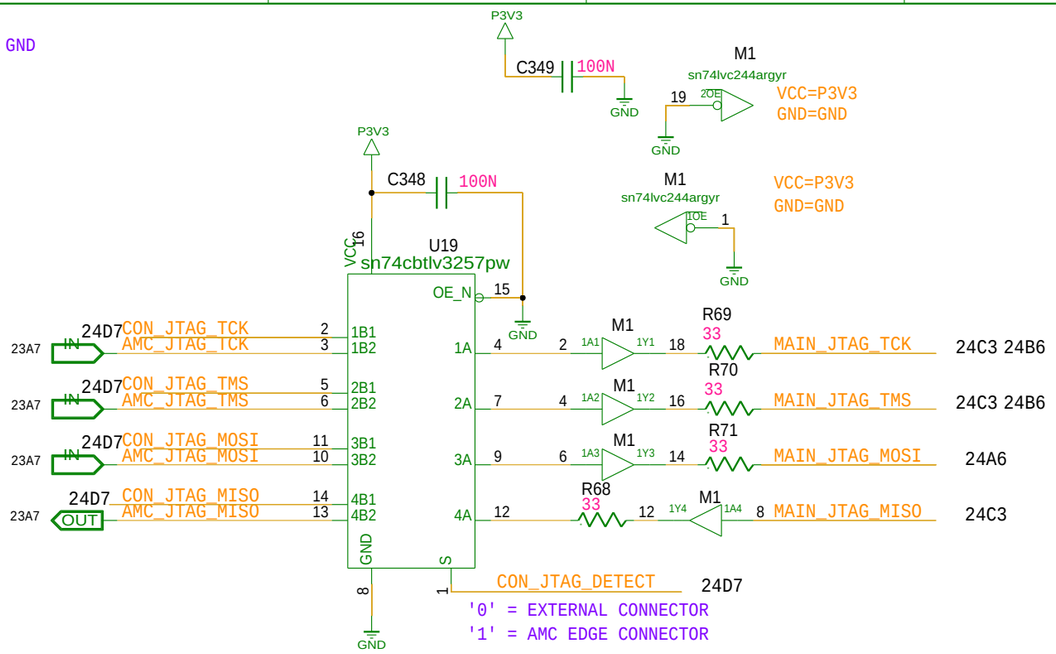


	ymca_card_v0	MODIFIE: Mon Mar 23 09:50:48 2015	
		ETUDE: N.Dumont Dayot	PAGE: 23 / 27
		DESSIN: N.Dumont Dayot	SHEET: 23 / 27
		AMC CONNECTOR	

MAPPING INSIDE USB BLASTER CABLE :NC PIN 8 CONNECTED TO GND
SEE IF DETECT COULD NOT BE DONE ON 2ND GND

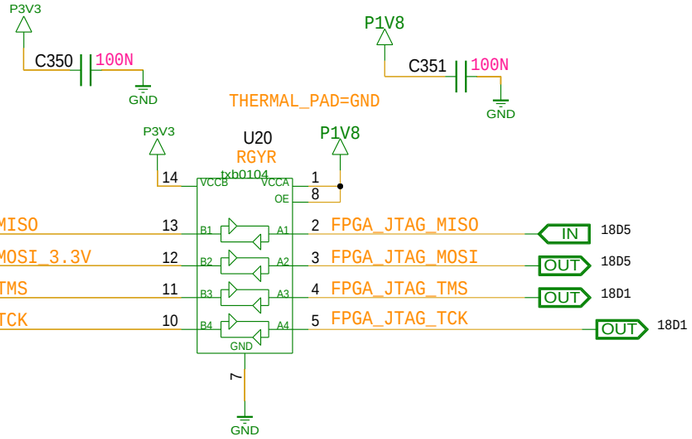


24D6
24D6
24D6
24C4
24D6

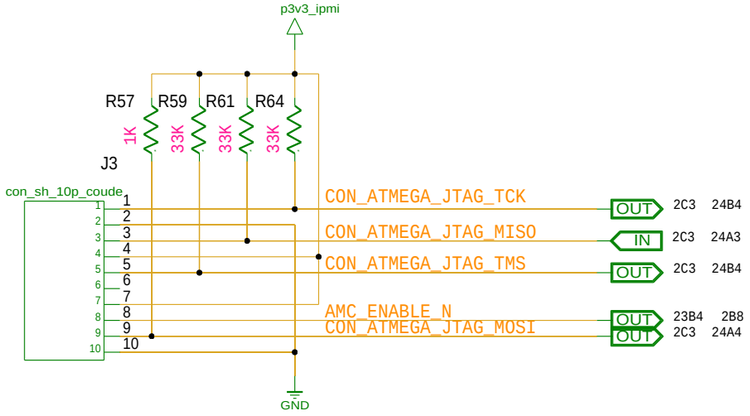


24C3 24B6
24C3 24B6
24A6
24C3

GND=GND VCC=P3V3
GND=GND VCC=P3V3
GND=GND VCC=P3V3
GND=GND VCC=P3V3



18D5
18D5
18D1
18D1



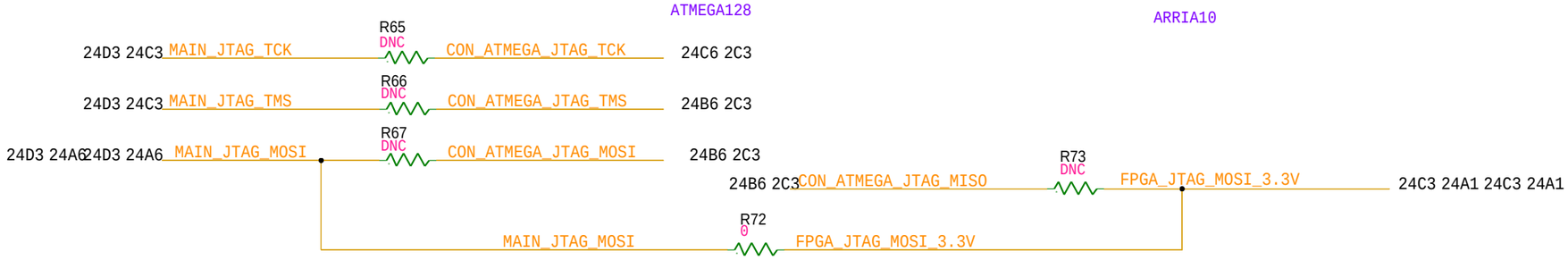
OUT 2C3 24B4
IN 2C3 24A3
OUT 2C3 24B4
OUT 23B4 2B8
OUT 2C3 24A4

MAIN JTAG

ATMEGA128

ARRIA10

3.3V<->1.8V TRANSLATION FOR ARRIA10 JTAG

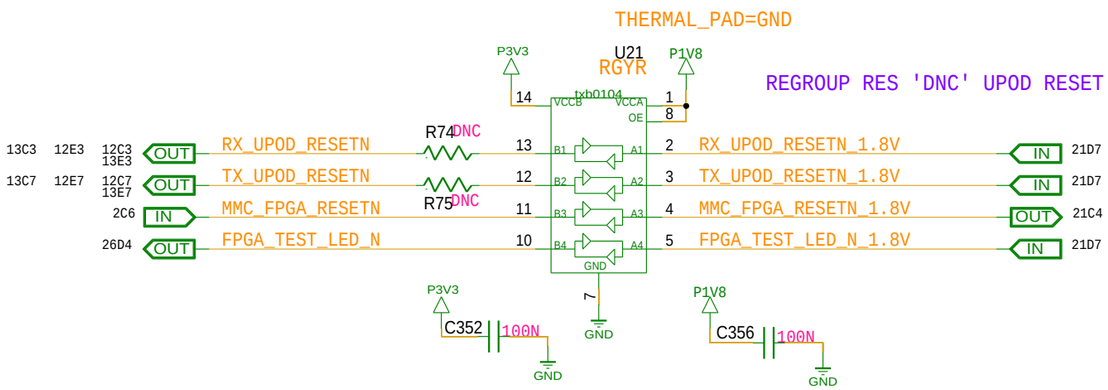


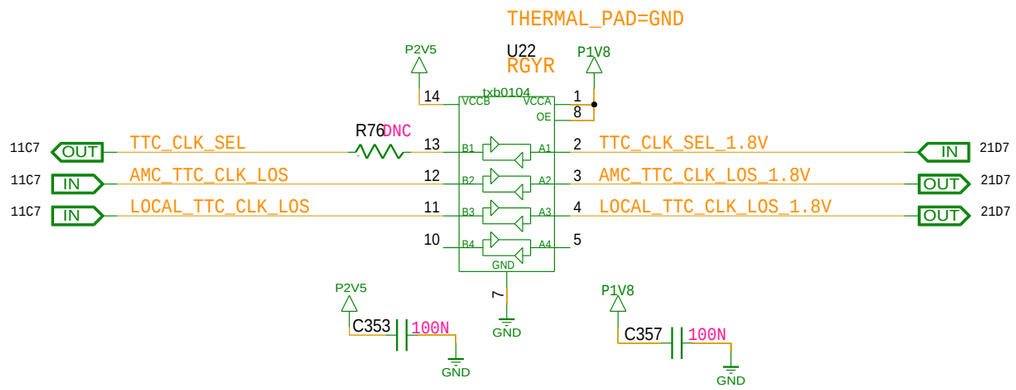
CONNECTION TO BE CLARIFIED AND VERIFIED

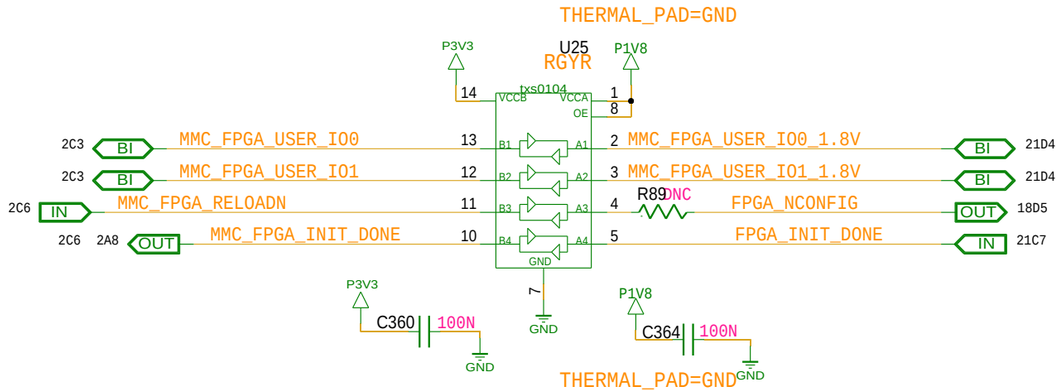
DEFAULT CONFIG : ATMEGA128 DISCONNECTED AND SHORTENED FROM MAIN JTAG CHAIN
REPLACE X RESISTANCE BY 0 AND 0 BY X TO PUT ATMEGA128 IN MAIN JTAG CHAIN

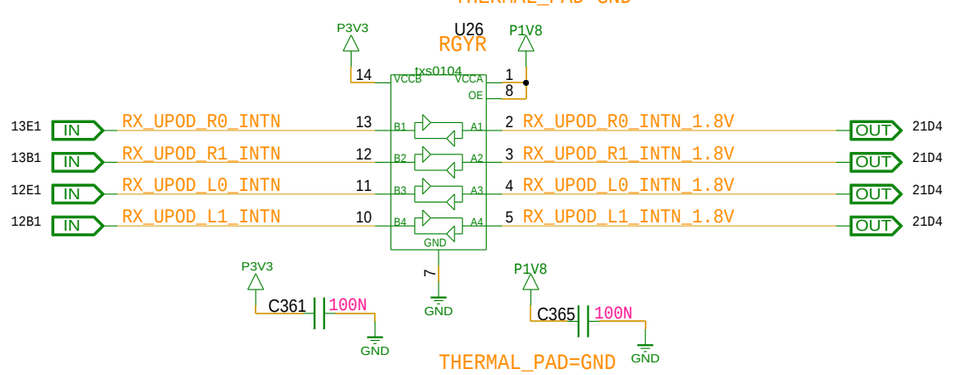
ymca_card_v0

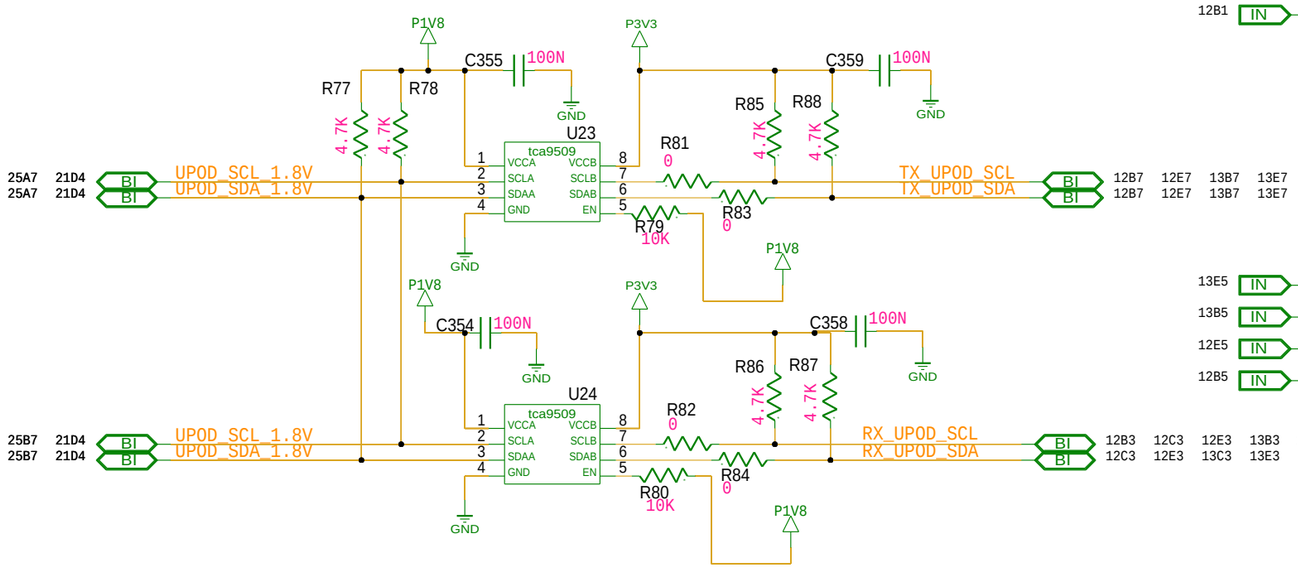
MODIFIE: Mon Mar 23 09:50:42 2015
ETUDE: N.Dumont Dayot | PAGE: 24 / 27
DESSIN: N.Dumont Dayot | SHEET: 24 / 27
JTAG CHAINS

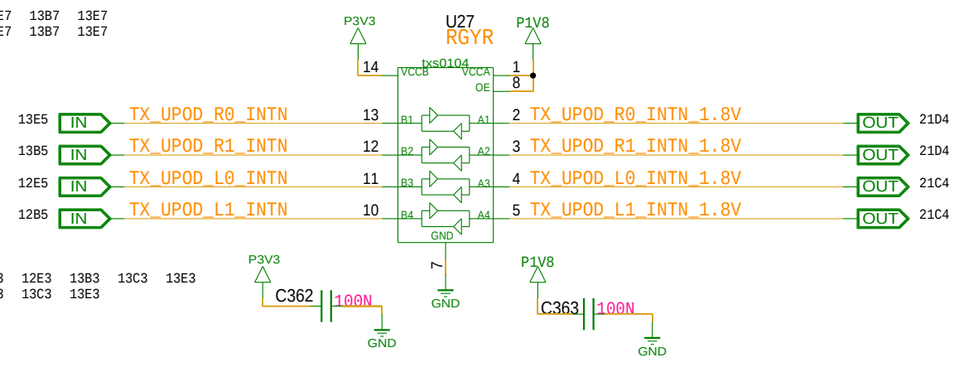












REGROUP RES 'DNC' UPOD RESET AND RES 'DNC' TTC_CLK_SEL

TXS0104 FOR OPEN DRAIN

I2C LEVEL SHIFTER BETWEEN FPGA AND UPOD

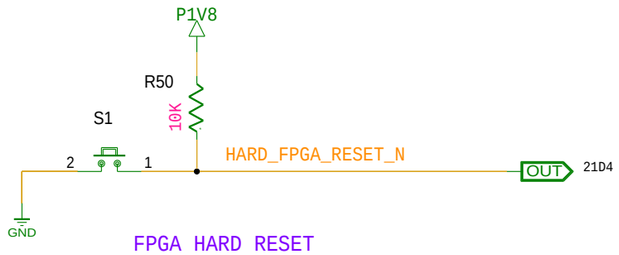
ymca_card_v0

MODIFIE: Mon Mar 23 09:50:42 2015

ETUDE: N.Dumont Dayot | PAGE: 25 / 27

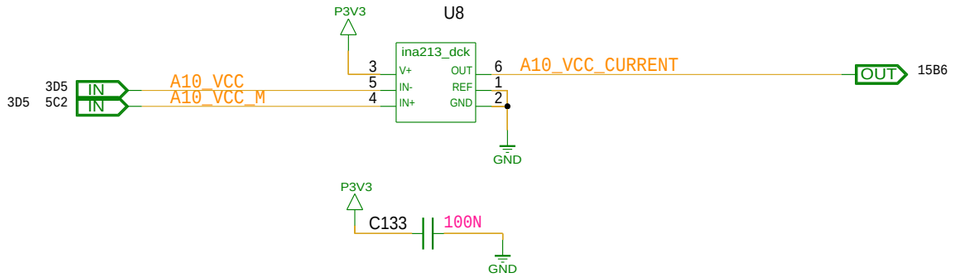
DESSIN: N.Dumont Dayot | SHEET: 25 / 27

LEVEL TRANSLATION

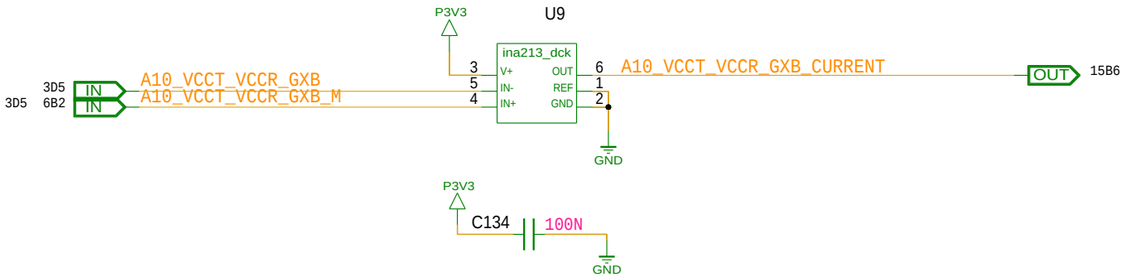


FPGA HARD RESET
SEE IF POSSIBLE TO PUT ON FRONT PANEL

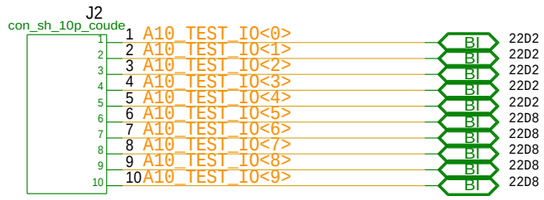
TEST LED FROM FPGA
SEE IF POSSIBLE TO PUT ON FRONT PANEL



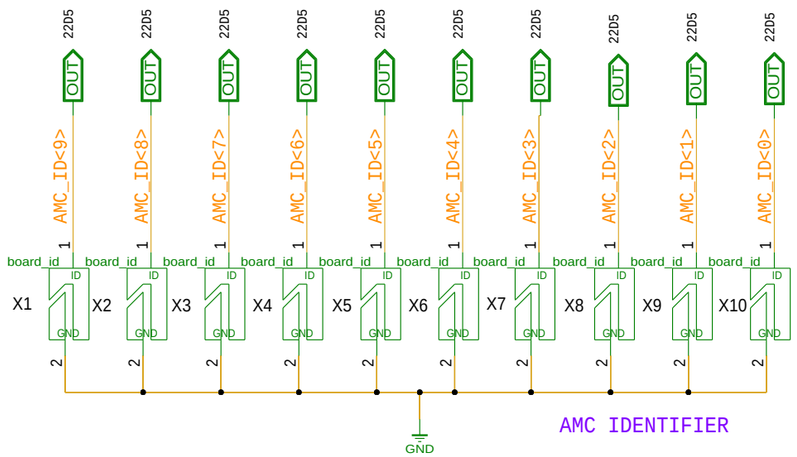
A10 VCC CURRENT MONITORING



A10 TRANSMITTER/RECEIVER GXB CURRENT MONITORING



TEST PADS FROM FPGA
SEE IF POSSIBLE TO PUT ON FRONT PANEL

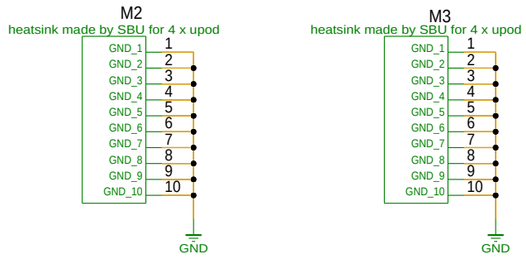


AMC IDENTIFIER

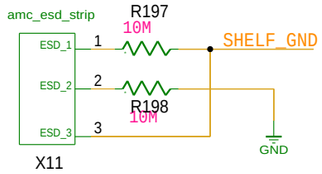
ymca_card_v0

MODIFIE: Mon Mar 23 09:50:43 2015
ETUDE: N.Dumont Dayot
PAGE: 26 / 27
DESSIN: N.Dumont Dayot
SHEET: 26 / 27
FPGA CONNECTIONS

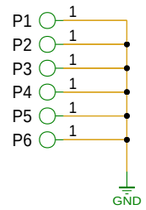
HEATSINK UPOD



SHELF GND = CONNECTED TO FRONT PLATE



GND LOOPS



	ymca_card_v0	MODIFIE: Mon Mar 23 09:50:43 2015
		ETUDE: N.Dumont Dayot — PAGE: 27 / 27
		DESSIN: N.Dumont Dayot — SHEET: 27 / 27
		OTHERS