The ATLAS Phase-I Upgrade LAr System ATCA Carrier Board

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1. Introduction

The Phase-I upgrade LAr trigger system includes components which receive digitized cell-level charges recorded in the EM calorimeter for each beam crossing, perform energy and time reconstruction from these inputs and transmit the results to L1Calo. For triggered events, results are also sent to the detector read out data stream, and dedicated monitoring information can be provided. These components, collectively called the LDPB, consist of processor mezzanine cards inserted in carrier cards. The input optical fibers used to receive data from the LAr front end system and output optical fibers used to transmit data to L1Calo are connected through the front panel of the mezzanine cards, and all associated processing occurs on the mezzanines. Data sent to the TDAQ system for triggered events as well as monitoring data are read out through the carrier, either via dedicated optical connections implementing the GBT protocol (TDAQ data) or via backplane connections implementing the 10 gigabit XAUI protocol (monitoring). The mezzanine and carrier cards are designed to the AMC and ATCA specifications respectively. The carrier provides four, full width AMC bays using the standard cut out form factor. It also includes a rear transition module (RTM) to provide external connectivity augmenting that available through the ATCA shelf backplane and AMC front panels. On board data routing and processing is provided via a Xilinx FPGA.

The bandwidth requirement[(1)] for trigger data flowing through the carrier is based on the expected number of bytes per L1 accept times the L1 accept rate. This gives 2 Gbps/carrier to the TDAQ system during running following the Phase-I upgrade and 10 Gbps/carrier following the Phase-II upgrade. The bandwidth for monitoring data is driven by two scenarios: (1) recording (prescaled) cluster input and reconstructed data for clusters with energy above a given threshold to allow online checks of the reconstruction and (2) an “oscilloscope” mode in which the digitized raw data for a selected set of channels is continuously sent to a LAr system for diagnostics and monitoring. The bandwidth required for these depends on the thresholds and number of channels to be viewed. A 10 Gbps/carrier rate was chosen as a compromise between the amount of information available and the design complexity.[1] The I/O for the raw front end data and the reconstructed energy and time data sent to L1Calo is performed through the AMC front panel and does not impact the bandwidth requirements for the carrier.

This note describes the design and features of the ATCA carrier and the RTM. Sections 2 and 3 describe the carrier data connectivity and processing capability respectively. Section 4 discusses the implementation of the ATCA mandated power, management and monitoring infrastructure as well as the additional power distribution on the board. The clocks provided on the carrier are described in section 5. Section 6 describes the JTAG and I2C functionality, and section 7 documents the jumpers present on the carrier. Section 8 provides RTM information. In addition, two appendices provide

[1] There are 31 carriers in the full system, so this 10 Gbps/carrier corresponds to 310 Gbps for the LAr system which is also a significant load to the LAr monitoring system(s).

detailed documentation of the connections used on the AMC interface and the ATCA/RTM interface[2]. A fourth appendix provides some information regarding the carrier layout.

2. Carrier Data transfer connectivity: Backplane, AMC sites and RTM

The carrier card's primary purpose is sending and receiving data. Data are received and/or transmitted using four methods: (1) serial transceiver connections between the carrier and AMC cards, (2) LVDS connections between the carrier and AMC cards, (3) serial transceiver connections to optical fibers which are connected to the carrier via SFP+ cages on the RTM and (4) serial transceiver connections between the carrier and other ATCA boards connected through the ATCA shelf backplane. In addition to the data sending and receiving, processing can be implemented in the onboard FPGA through which all data passes.

A block diagram of the carrier data and clock connectivity is shown in Figure 1, and the data connections are shown in Table 1 grouped by destination and reference clock domain (Sec. 5). The transceiver and LVDS connections are general purpose and do not have a fixed protocol requirement. However, three protocols are expected to be used: (1) gigabit Ethernet (GbE) links between the carrier, AMC sites and ATCA shelf for configuration and control, (2) 10 gigabit XAUI links between the carrier, AMC sites and shelf for private monitoring and (3) GBT links between the carrier, AMC sites and RTM for communication with the ATLAS TDAQ system. In addition LVDS signals are provided between the carrier and each AMC site in case dedicated communication (e.g. decoded trigger information from the GBT) is needed. This is not expected, but provided in case there are resource limitations on the AMCs. The types of data to be sent using the different connections are shown in Table 2. The table also includes the Xilinx GTH transceiver mapping to signals. As required by the AMC and ATCA specifications, the data and clock lines are AC coupled on the receiving end of each differential pair and the traces will each have 50Ω impedance, matching the pair termination of 100Ω.

Though not formally required by the specifications, most AMCs and ATCA cards expect a GbE link on a specific channel. For AMCs this is expected to be port 0, and for ATCA cards it is expected to be on the zone 2 base channels 1 and 2. These ports are provided on the LAr carrier and its AMC sites. In addition, the carrier has a GbE connection to the RTM and a 100 Mbps Ethernet connection to the IPMC.[3]

[2] The FPGA pin information is at http://sbhepnt.physics.sunysb.edu/LArUpgrade/ATCA_FPGA_PINOUT-REV-A.pdf

[3] In the first test version of the carrier, the GbE connections will all be routed through the FPGA with minimal switching firmware, and the 100 Mbps IPMC will be connected to an RJ45 socket on the RTM . In addition, the two ATCA base connections will not be implemented, and an SFP connection will be provided on the RTM for Ethernet access. An evaluation of possible standalone GbE switches is ongoing. For the second version of the carrier the final configuration, either GbE through the FPGA or GbE through a dedicated switch will be used. This will be decided based on the evaluation of firmware versus hardware switches. The baseline choice is use of an Intel FM2112/4112 switch, but a simpler unmanaged switch like the Broadcom BCM5389 may be used instead. An FPGA firmware solution is unlikely to be used in the long run. The full XAUI implementation on the ATCA fabric interface will be available.

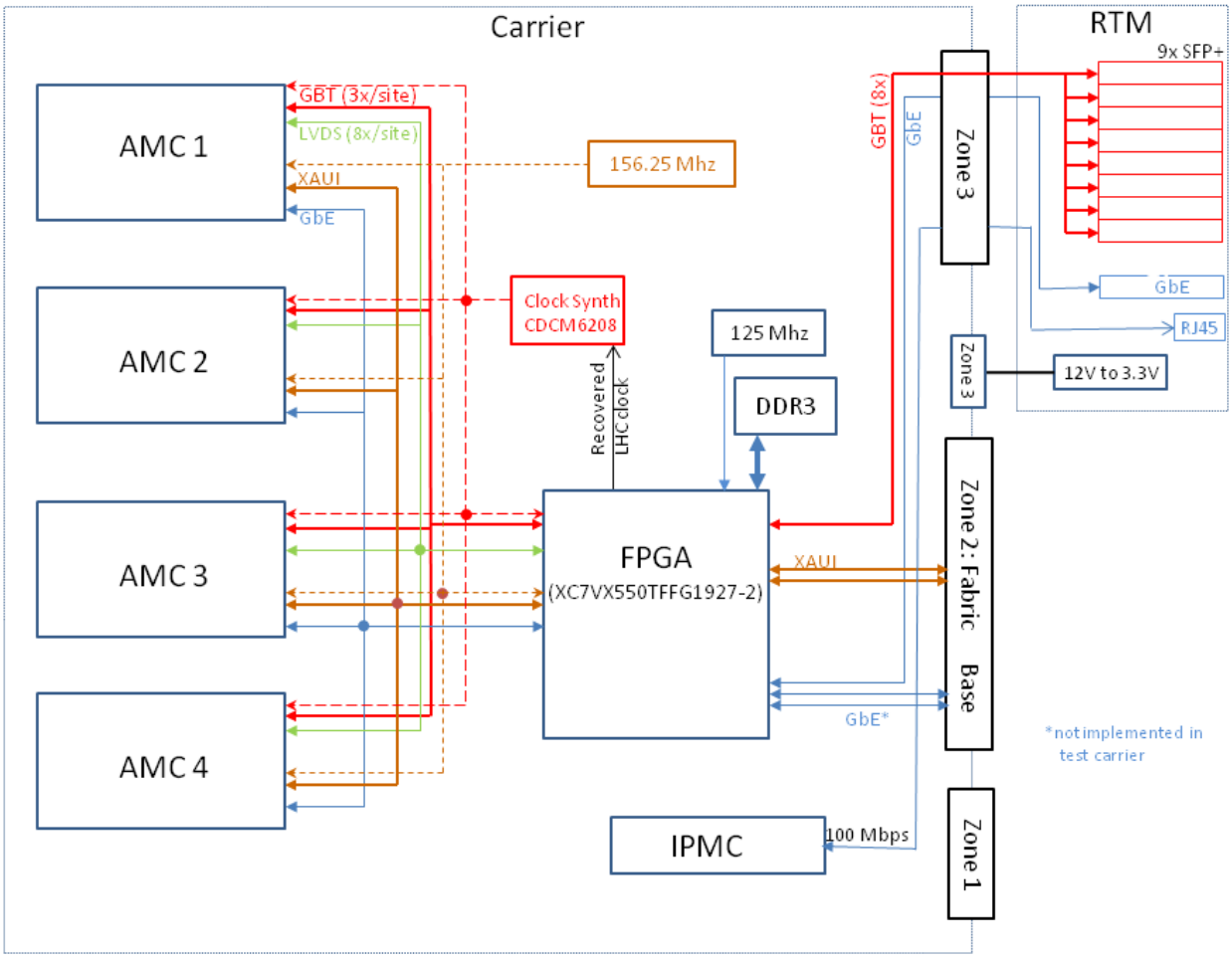

Figure 1: A block diagram of the data and clock connections on the test version of the ATCA Carrier. For later versions, two ATCA base gigabit ethernet connections will be added and all gigabit or slower Ethernet connections, including the 100 Mbps IPMC Ethernet will go through a switch on either the carrier or RTM. All other interfaces are complete on the test carrier.

Tx/Rx Count	Reference Clock	Intended Protocol	Type
Group 1: Transceiver connections to each AMC bay (4xAMC for 32 in total)			
4	156.25 Mhz	1 x XAUI	GTH[(2)]
3 (1)	ATLAS recovered	3 x GBT	GTH
1	125 Mhz	GbE	GTH
Group 2: LVDS differential pair connections to each AMC bay (4x for 32 in total)			
8	Any	Decoded trigger information	SelectIO[(3)]
Group 3: Transceiver connections to RTM			
8 (5)	ATLAS recovered	8 x GBT	GTH
1	125 Mhz	GbE	GTH
Group 4: Transceiver connections to ATCA backplane			
8	156.25 Mhz	2 x XAUI	GTH
2	125 Mhz	2 x GbE	GTH

Table 1: The data connections on the ATCA carrier grouped by destination and clock domain. The intended protocol and signal types are also shown. The numbers in parentheses are the minimal number of connections needed by LAr.

Port Type	Connection: Count – Dest	FPGA Bank / GTH Channel(s)	Intended Use
GBT	3 (1) – AMC 1 3 (1) – AMC 2 3 (1) – AMC 3 3 (1) – AMC 4 8 (5) – RTM	214/1,2,3 215/1,2,3 216/1,2,3 217/1,2,3 213/all, 214/0, 215/0, 216/0, 217/0	ATLAS trigger control (input) and event data transmitted upon L1 accept. Clock recovery.
XAUI	1 – AMC 1 1 – AMC 2 1 – AMC 3 1 – AMC 4 2 – ATCA fabric	114/all 115/all 116/all 117/all 118/all, 119/all	Private monitoring data, for example, continuous output of selected channel pulse heights
GbE	1 – AMC 1 1 – AMC 2 1 – AMC 3 1 – AMC 4 1 – RTM 1 – IPMC[4] 2 – ATCA base	218/0 218/1 218/2 218/3 219/3 219/0 219/1,2	Configuration and general communication
LVDS	8 – AMC 1 8 – AMC 2 8 – AMC 3 8 – AMC 4	16 14 19 18	Additional trigger related communication between carrier and AMC sites if needed

Table 2: The connections on the carrier grouped by intended protocol. The table also shows the external connectivity and the FPGA banks associated with each signal (set). The data use is also given. The numbers in parentheses are the minimal number of connections needed by LAr.

3. Carrier Data Processing Capability

The primary task of the carrier is transmitting and receiving data, but it also provides processing capability. All of the data paths in Table 2 are connected to an on carrier FPGA whose primary purpose is data routing, but which can be used to provide processing. The FPGA is a Xilinx Virtex-7 XC7VX550TFFG1927-2[5] with a direct connection to 512 MB of DDR3 RAM. The DDR3 is implemented using two MT41J128M16 chips configured to provide a 32 bit wide data path. The FPGA system clock and DDR3 reference clock use the 125 Mhz oscillator (sec. 5). The FPGA related design is based on that

[4] The IPMC Ethernet connection is a 10/100 Mbps connection, not a gigabit connection.

[5] The carrier design allows the use of either of two other pin-compatible FPGAs, the XC7VX485TFFG1927 or the XC7VX690TFFG1927 in place of the default XC7VX550TFFG1927.

of an AMC board recently designed and tested by the BNL, Stony Brook and Arizona groups. The mandatory processing functions foreseen in FPGA are data routing (sec. 2) and clock recovery (sec. 5), and it is likely that significant processing capacity will remain after the basic functions have been provided.[6]

4. ATCA infrastructure: Management, Power and Monitoring

The carrier will be installed in an ATCA shelf, so it must implement the system management functionality required by the ATCA standard. This includes: (1) all power drawn from the -48V from the ATCA zone 1 power connector, (2) board power management and status monitoring provided through the IPMI[(2)] protocol and ATCA extensions[(3)] implemented as dual I2C buses on the ATCA shelf backplane and controlled locally through an intelligent power management controller (IPMC), (3) ATCA (software based) e-keying, (4) sensor monitoring, status and alarm reporting via the IPMB and (5) management of the AMC bays in the carrier, including the corresponding power management, status and alarm reporting and e-keying handled through device descriptors read from the AMCs. The RTM is not hot-swappable (as allowed by the ATCA standard) but must receive power from the carrier. The LAr carrier uses an ATLAS standard IPMC designed by the Annecy/LAPP ATLAS group [(4)] to provide all board management functions. The ATCA standard also specifies electrostatic shielding and status LEDs both of which are included in the carrier as defined in the standard.

The ATCA standard allows a maximum board power for carrier plus AMCs plus RTM of 400 W. The 48V ATCA controller (IQ65033QGA12EKF-G) and the 48V to 12V controller (PQ60120QZB33NNS-G) used on the carrier are both rated at 400 W. Components need supply voltages at 1.0V (separately for digital logic and FGPA transceivers), 1.2V, 1.5V, 1.8V, 2.5V and 3.3V. All these voltages are provided by DC-to-DC converters. The DC-to-DC converters for 2.5V, 3.3V, FPGA 1.8V and core 1.0V are supplied directly from the 12V ATCA payload power, but the 1.0V MGT, 1.2V and 1.5V have tight ripple tolerances so these converters are powered from a dedicated, low ripple 5V converter (which is itself powered by the 12V payload power)[7]. The power sequencing is either hard-wired using the presence or absence of resistors (test mode) or controlled by IPMC user I/O pins (production). The power available at each voltage is given in Table 3.

Tests of an existing AMC card with a full complement of micropods and a Virtex-7 VC7VX485TFFG1927-2 FPGA, indicate that each AMC site is likely to require 80W, leaving 80W for the carrier and RTM together. On the AMC card, the power demand is dominated by the FPGA transceivers. Because the carrier has lower data rates and processing requirements, the power demands on the carrier are expected to be somewhat less than for the AMC card(s).

The standard also specifies that status, sensor and alarm information be provided using the IPMB protocol implemented between the shelf manager and the carrier and between the carrier and its AMC cards. Table 4 shows the sensors available on the carrier. Some sensors are connected directly to the sensor bus (S) from the IPMC, but this bus also is connected to an I2C switch which provides two

[6] The FPGA choice is motivated by the transceiver count and data rate capabilities.
[7] The FPGA and FPGA power sequencing designs are taken from the existing SBU/BNL/AZ AMC card.

additional subsidiary I2C sensor buses, S0 and S1, which are required to access the full sensor suite. The switch is a PCA9543ADR located at (binary) I2C address 1110000X. The data from all sensors, including those on the AMCs, are collected by the IPMC. In all cases, e-keying descriptors will be used to provide the information needed for the carrier and shelf manager to discover what sensors are available and to report the status and alarms.

Source	Available Current
48V ATCA module	8.33 A (400 W)
12V total payload (48V to 12V)	33.3 A (400 W)
3.3V management	3.6 A
3.3V	8 A (from 12V)
2.5V	8 A (from 12V)
1.8V (linear, MGTVCCAUX)	3 A (from 12V)
1.8V (linear, VCC1V8)	3 A (from 12V)
1.0V, core	16 A (from 12V)
5.0 V preregulator	16 A (from 12V)
1.5V	8 A (from 5V)
1.2V	8 A (from 5V)
1.0V, GTX/GTH	16 A (from 5V)
AMC 3.3V management (ea. site)	0.165 mA
AMC 12V payload (ea. site)	80 W

Table 3: The voltages available on the carrier and the maximum current provided by each. Note that the total power from the all on-carrier voltages lower than 12V plus the power to the AMC sites must not exceed the 400 W available from the 12V payload power.

Sensor Type	Chip Designator, Type	Sensor Bus, Address
Temperature	U6, TMP100NA/250	S, 1001000X
"	U7,	S, 1001010X
"	U4,	S, 1001011X
"	U5,	S, 1001100X
Current monitor, ATCA 12V payload power	U8, LTC2945	S0, 1100111X
" " AMC1 12V " "	U9	S0, 1100110X
" " AMC2 12V " "	U12	S0, 1101000X
" " AMC3 12V " "	U10	S0, 1101001X
" " AMC4 12V " "	U11	S0, 1101010X
" " RTM 12V " "	U47	S0, 1101011X
FPGA internal voltage and temperature	FPGA	S0, set by f/w
Current monitor, ATCA 1.2V (FPGA)	U14, LTC2945	S1, 1101000X
" " " 1.5V "	U16	S1, 1101010X
" " " 2.5V	U17	S1, 1101101X
" " " 3.3V	U13	S1, 1101001X
" " " 5V	U15	S1, 1101011X
" " " 1.0V (FPGA)	U18	S1, 1101100X
" " " 1.0V (FPGA)	U19	S1, 1101110X
" " " 1.8V	U74	S1, 1100111X
" " " 1.8V (FPGA GTH)	U75	S1, 1101111X

Table 4: IPMB/I2C accessible sensors on the carrier. The "S" bus is directly connected to the IPMC sensor bus. The "S0" and "S1" buses are connected to the "S" bus through the I2C switch.

The IPMC has several optional features available, and the LAr carrier uses two of these. The IPMC 100 Mbps Ethernet interface is connected to an RJ45 socket on the RTM (and to a hardware switch or the FPGA in v2). It is used for general communication with the IPMC processor, for IPMC software upgrades, and it can be used as the master for the on-board JTAG chain. The IPMC also has user definable I/O pins. Some of these are used in the carrier as select, enable or monitoring lines. These are described in Table 5.

IPMC User Pin	Purpose
IPM_IO2	Test point (TP33, output)
USR2	1.2V power good (I)
USR3	1.5V power good (I)
USR4	1.8V power good (I)
USR5	2.5V power good (I)
USR6	3.3V power good (I)
USR7	5.0V power good (I)
USR8	Enable 1.0V DC-to-DC (O) ; Has resistor bypass
USR9	Enable 1.2V and 1.5V DC-to-DC (O); Has resistor bypass
USR10	Enable 2.5V and 3.3V DC-to-DC (O) ; Has resistor bypass
USR11	VTTVREF power good (I)
USR12	MGTVCCAUX (1.8V) power good (I)
USR13	VCCINT (1.0V) power good (I)
USR14	MGTAVCC (1.0V) power good (I)
USR16	I2C switch reset (O)
USR17	JTAG: connector or IPMC source select (O); Has jumper bypass
USR19	FPGA Boot memory select (See Table 7, J2)

Table 5: The IPMC user I/O pins used on the carrier.

The FPGA and its boot memories are programmed using the Xilinx JTAG interface. The JTAG can be driven either by a cable connected to a header on the carrier or RTM back panel (testing) or by an Ethernet connection to the IPMC (in situ). If the GbE switch functionality is provided in the FPGA, care will be required to ensure that Ethernet connection is not broken by the programming process.

5. Clock(s) generation and distribution

Clocks are needed on the carrier for general system use and to provide reference clocks for data communication. There are four fundamental clock sources provided on the carrier: (1) a 125 Mhz oscillator, (2) a 156.25 Mhz oscillator, (3) a 40.079 Mhz oscillator, and (4) an LHC clock recovered in the FPGA from the ATLAS GBT optical fiber connection to the RTM. Figure 2 and Table 6 summarize the connections driven by these clocks. The 40.079 Mhz oscillator is input to an Si5338 clock generator. The Si5338 outputs are connected to the are connected to the FPGA GBT banks and to the secondary input of a CDCM6208 clock generator. The recovered ATLAS clock is input the primary channel of the CDCM6208. The CDCM6208 synthesizer outputs are connected to the FCLKA ports on the four AMC bays, and to the FPGA RefClk0 inputs (as shown in Table 2) for the quads used for the GBT signals

between the carrier and AMC bays and between the FPGA and the RTM. There are only eight total outputs from the CDCM6208, so some FPGA GBT quads get this reference clock from an adjacent quad using the Xilinx "north" or "south" reference clock mechanism.

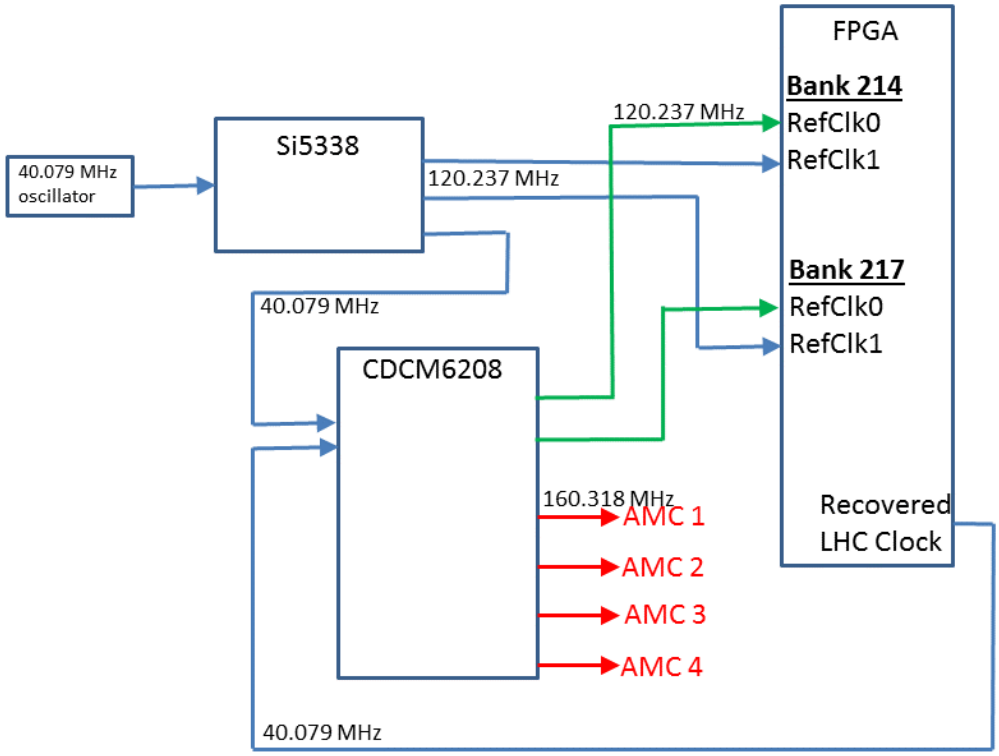

Figure 2: The clock distribution network. The frequency expected for each signal is also shown. (The Si5338 and CDCM6302 are quite flexible, so other frequencies can also be generated if desired.)

Clock Source	Drives
125 Mhz (GbE)	FPGA system clock FPGA Bank 218, RefClk0 (and bank 219 using the north/south reference clock mechanism)
156.25 Mhz (XAUI)	AMC FCLKA (all sites) FPGA Banks 115, 118 RefClk0 (and banks 114, 116, 117, and 119 using the north/south reference clock mechanism)
40.079 Mhz oscillator	Si5338
40.079 Mhz recovered LHC clock	CDCM6208 Clock Synthesizer, primary channel
Si5338 Clock Synthesizer	CDCM6208 Clock Synthesizer, secondary channel FPGA Banks 214, 217; RefClk1 (and to banks 213, 215, 216 and 218 using the north/south reference clock mechanism)
CDCM6208 Clock Synthesizer	AMC TCLKA (all sites) FPGA Banks 214, 217; RefClk0 (and to banks 213, 215, 216 and 218 using the north/south reference clock mechanism)

Table 6: The carrier clock sources and their uses

The synthesizer input select signal REFSEL and the I2C controls of the CDCM6208 clock synthesizer are sourced from the FPGA. The synthesizer SYNCHn, RSTn, STATUS0, and STATUS1 synthesizer signals are also connected to the FPGA. The FPGA firmware must ensure that the FPGA pins CLK_SYNCn (=SYNCn) and CLK_RSTn (=RSTn) are driven high for the synthesizer to function, and the appropriate value of CLKSEL (=REFCLK) must be chosen. The Si5338 (oscillator) input is chosen if CLKSEL=0, otherwise the recovered ATLAS clock input is used. The ATCA default firmware uses the Si5338 as the source with the frequencies as shown in Figure 2.

The 40.079 MHz oscillator is input to Si5338 clock generator chip. One Si5338 output is connected to the secondary input channel of the CDCM6208 clock synthesizer. This provides a stable 40.079 MHz input whether or not the recovered clock is available. Two of the other outputs are connected to FPGA banks 214 and 217 RefClk1 inputs to provide a GBT clock.

As with the FPGA design, this clock distribution system is based on the design used on the existing test AMC. The same clock synthesizer chip is used, and a similar distribution network is provided. Tests using data transmitted between two AMCs with independent synthesizers show the synthesizer provides the low-jitter needed to meet the error rate demands.

6. JTAG, I2C

In addition to the data transfer and ATCA infrastructure related buses, the carrier also has on board JTAG and I2C buses. The ATCA and AMC standards specify JTAG connections between the carrier and AMC bays. These are implemented on the carrier as a single chain, and the AMC payload power good signal(s) at each bay are used to automatically select whether the chain bypasses the AMC bay or is passed through the AMC bay. When bypassed, the AMC TDI, TCK and TMS signals to the bay are disabled (high impedance) and the TDO from the bay is bypassed using a multiplexor. The chain is connected to the RTM in the same manner as to the AMC bays. The same chain is also passed through the FPGA JTAG port where it will be used to program the FPGA boot memory, to configure the FPGA directly for testing new firmware, and to provide the terminal connection used for debugging. The FPGA is the first device on the chain, followed by each of the AMC bays in numerical order and finally by the RTM interface.

The JTAG chain can be mastered by one of two sources: (1) the IPMC JTAG master (production, in situ) or (2) an external source connected by a cable to a header on either the carrier (J11) or the RTM back panel (J2) (testing). The source selection is controlled by a jumper (J19) which can be set either to force either one of the two sources or to allow selection by the IPMC using a user I/O line (USR17).

The IPMB protocol required by the AMC and ATCA standards uses I2C for the underlying transfer protocol. The ATCA standard also specifies a sensor I2C bus mastered by the IPMC as described in Sec. 4. An additional, independent I2C bus on the carrier interconnects the FPGA and the clock generators (Sec. 5) and is used to configure and monitor the clock generators. This bus can be accessed by the IPMC (via the I2C sensor bus connection to the FPGA) with appropriate firmware in the FPGA.

7. Jumpers

The low-level carrier configuration can be set using onboard jumpers. These are primarily intended for use in early versions of the board and for testing outside an ATCA shelf. Table 7 lists the jumpers and defines their functionality.

Jumper	Function
J2	FPGA Boot: 1<->2: Primary flash; open, secondary; 2<->3, IPMC USR19 select
J3	Force enabling of the ATCA 12V payload power (normally removed)
J4	IPMC reset (normally removed)
J5	Allow 12V regulation without distributing power to components (2<->4 connected) or with distribution 12V as normal (1<->2; 3<->4)
J6	Force enabling of ATCA -48 channel B (normally removed)
J7	Force enabling of ATCA -48 channel A (normally removed)
J8	RTM JTAG bypass (removed if RTM is connected; present if not)
J19	JTAG source select. (normally 2<->3)
J27	FPGA JTAG bypass (normally removed; install only if FPGA not present)
J29	Force enabling of AMC 1, 3.3V (normally 2<->3)
J31	Force enabling of AMC 1, 12V (normally 2<->3)
J32	Force enabling of AMC 1, “or” (normally 2<->3)
J33	Force enabling of AMC 2, 3.3V (normally 2<->3)
J34	Force enabling of AMC 2, 12V (normally 2<->3)
J35	Force enabling of AMC 2, “or” (normally 2<->3)
J36	Force enabling of AMC 3, 3.3V (normally 2<->3)
J37	Force enabling of AMC 3, 12V (normally 2<->3)
J38	Force enabling of AMC 3, “or” (normally 2<->3)
J40	Force enabling of AMC 4, 12V (normally 2<->3)
J41	Force enabling of AMC 4, “or” (normally 2<->3)
J42	Force enabling of AMC 4, 3.3V (normally 2<->3)
J43	Force enabling of RTM 3.3V (normally 2<->3)
J44	Force enabling of RTM 12V (normally 2<->3)
J45	Force enabling of RTM “or” (normally 2<->3)

Table 7: Jumper functionality

8. RTM

As described earlier in section 2, a rear transition module (RTM) is used to provide some of the connectivity between the carrier and external hardware. The LAr carrier RTM provides SFP+ cages on the back panel for nine carrier transceiver channels: eight GBT channels[8] and a single GbE connection, and an RJ45 connector for the IPMC 100 Mbps Ethernet connectionIt also has JTAG connectors on the back panel providing access to the onboard JTAG chain and the IPMC JTAG slave interface. In addition to GBT data signals and 3.3V and 12V power, the RTM Zone 3 connector has a full AMC-style management interface.

[8] The production version of the carrier requires a maximum of five GBT links. Initial test versions will provide eight possible links to explore various layout options.

An RTM power switch is located on the back panel. This allows direct on/off control of the RTM DC-to-DC converter providing overall power to the RTM. The switch is provided purely as a precautionary convenience. The initial 12V power to the RTM through the zone 3 power connector is controlled by the IPMC in the same manner as for the AMC sites. The ATCA standard blue LED is part of the RTM.

The RTM data connection to the carrier is a standard ATCA connector (TE Connectivity/AMP 6469048-1) located in carrier zone 3. A second zone 3 connector (TE Connectivity 5-5223963-1) provides 3.3V management power and 12V payload power to the RTM. The LAr RTM is not hot swappable, but the interface needed to implement a fully ATCA compliant hot-swappable RTM with an onboard MMC and management through the carrier IPMB is provided on the zone 3 connector should it be needed. The complete list of zone 3 connections is given in Appendix B.

Appendix A: AMC slot data connectivity summary

Table 8 shows a summary of the data and clock signals available on the AMC connectors. In accordance with the definition provided by the AMC and ATCA specifications, the data transceiver port signal directions are shown from the carrier view. That is, transmit (Tx) means a signal sourced by the carrier, and receive (Rx) means the opposite. The standard power, IMPB and JTAG connections are not shown in the table but they are implemented. The IPMC has numbered sets of signals for each possible AMC site with one additional set available. The correspondence between the AMC site number and the IPMC set number is shown in Table 9.

AMC Port	Purpose
0	GbE
1	-
2	SBU reserved (μ LVDS)
3	SBU reserved (μ LVDS)
4	N.C. (LAPP reserved)
5	N.C. (LAPP reserved)
6	SBU reserved (μ LVDS)
7	SBU reserved (μ LVDS)
8	XAUI, Lane 0
9	XAUI, Lane 1
10	XAUI, Lane 2
11	XAUI, Lane 3
12	GBT 1
13	GBT 2
14	-
15	LVDS
TCLKC/D	-
17	LVDS
18	LVDS
19	LVDS
20	GBT3
FCLKA	LHC Clock (Synth out)
TCLKA	156.25 (XAUI)

Table 8: The AMC ports available on the carrier. The protocols shown are those intended for the LAr use. However, on the carrier the signals are connected to an FPGA, so there is considerable flexibility in the protocol choice.

AMC/RTM Site	AMC 1	AMC 2	AMC 3	AMC 4	RTM
IPMC Control Set	1	2	3	4	8

Table 9: The correspondence between AMC or RTM site number and the AMC interface control set number on the IPMC

Appendix B: Zone 3 Connections between the carrier and RTM

Function	Pin(s)	Function	Pin(s)	Function	Pin(s)	Function	Pin(s)
Power & Control		GBT R1 Txp	A1	GBT R5 Txp	A5	GbE Txp	E3
SCL (IPMB)	E1	Txn	B1	Txn	B5	Txn	F3
SDA (IPMB)	F1	Rxp	C1	Rxp	C5	Rxp	G3
IPMC Txp	E2	Rxn	D1	Rxn	D5	Rxn	H3
IPMC Txn	F2	GBT R2 Txp	A2	GBT R6 Txp	A6		
IPMC Rxp	G2	Txn	B2	Txn	B6		
IPMC Rxn	H2	Rxp	C2	Rxp	C6		
GA0	A9	Rxn	D2	Rxn	D6		
GA1	B9	GBT R3 Txp	A3	GBT R7 Txp	A7		
GA2	C9	Txn	B3	Txn	B7		
EXT_RST_N	D9	Rxp	C3	Rxp	C7		
TRST	B10	Rxn	D3	Rxn	D7		
TDO	C10	GBT R4 Txp	A4	GBT R8 Txp	A8		
TDI, RTM	D10	Txn	B4	Txn	B8		
TCK	E10	Rxp	C4	Rxp	C8		
TMS	F10	Rxn	D4	Rxn	D8		
Enable#	G10						
PS1#	H10						
Connector: carrier JTAG chain				Connector: IPMC Slave			
TCK		E4		TCK		E9	
TDO		F4		TDO		F9	
TMS		G4		TMS		G9	
TDI		H4		TDI		H9	

Table 10: The Zone 3 data and control connections. The transmit and receive signal directions are defined with respect to the carrier: Tx means from the carrier to the RTM, and Rx means to the carrier from the RTM.

Appendix C: PCB Layout information

The ATCA carrier layout is based upon experience gained during the layouts of the AMC test board and the FM2112 Ethernet switch test board. The board thickness and area, and thus the trace geometry constraints and lengths, differ among all three so a straight copy of the layout parameters and stack up is not possible. The ATCA LVDS and serial transceiver differential pairs are laid out as length-matched 100 Ω pairs, and the DDR3 differential pair traces will be length-matched at 80 Ω/pair. In addition, blocks of DDR3 signals will also be length matched to 200 mils as was done, and demonstrated to function properly, on the AMC optical test board.

The constraints on ATCA board thickness, component height and board flatness will be followed for the carrier as will the grounding and LED requirements. The dielectric material to be used in the ATCA carrier is FR408HR, a choice made in consultation with the PCB manufacturer. The carrier parts placement is shown in Figure 2 (top) and Figure 3 (bottom), and the stack up is shown in Figure 4. The total thickness is 94.6 mils, just under the ATCA maximum thickness of 96 mils. The minimum trace width is 3.5 mils, and the differential pair spacing is 10 mils. The maximum finished through hole size is 8 mils (on an 18 mil pad).

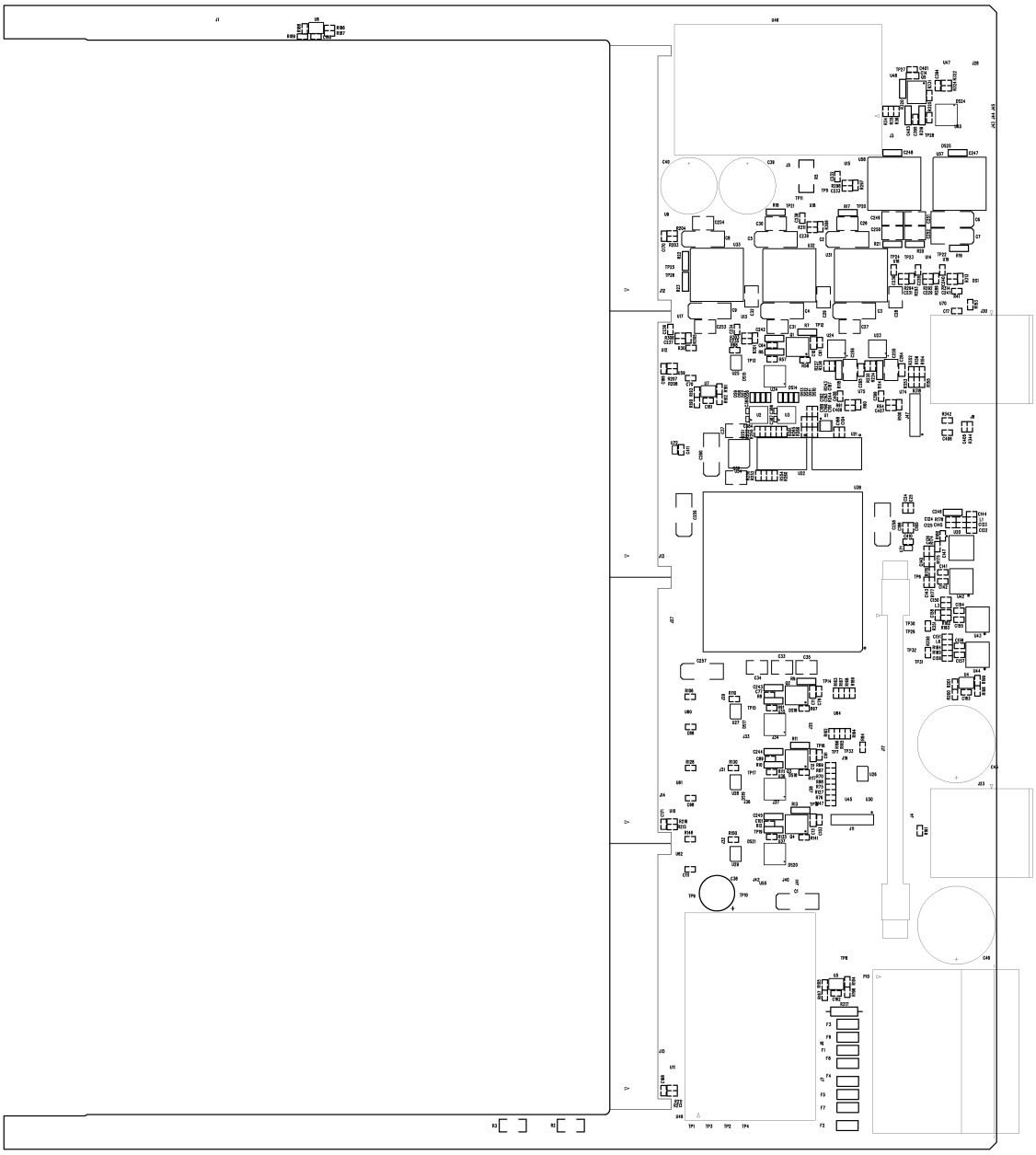

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Figure 3: The top view of the ATCA carrier initial parts placement.

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Figure 4: The bottom view of the ATCA Carrier initial parts placement. Although this is the bottom, the view is oriented as seen from the top.

Layer	Calc Thickness	Primary Stack	Description
	0.0005		Taiyo 4000-BN
Layer - 1	0.0020		**1/2oz Sig (Std Plt)**
	0.0031	1080HRC	FR408HR
Layer - 2	0.0006		**1/2oz P/G**
	0.0040	0.0040	FR408HR
Layer - 3	0.0006		**1/2oz Sig**
	0.0050	1080 106	FR408HR
Layer - 4	0.0006		**1/2oz P/G**
	0.0040	0.0040	FR408HR
Layer - 5	0.0006		**1/2oz Sig**
	0.0050	1080 106	FR408HR
Layer - 6	0.0006		**1/2oz P/G**
	0.0040	0.0040	FR408HR
Layer - 7	0.0006		**1/2oz P/G**
	0.0051	1080 106	FR408HR
Layer - 8	0.0006		**1/2oz P/G**
	0.0040	0.0040	FR408HR
Layer - 9	0.0006		**1/2oz P/G**
	0.0051	106 1080	FR408HR
Layer - 10	0.0006		**1/2oz P/G**
	0.0040	0.0040	FR408HR
Layer - 11	0.0006		**1/2oz P/G**
	0.0050	106 1080	FR408HR
Layer - 12	0.0006		**1/2oz Sig**
	0.0040	0.0040	FR408HR
Layer - 13	0.0006		**1/2oz P/G**
	0.0050	106 1080	FR408HR
Layer - 14	0.0006		**1/2oz Sig**
	0.0040	0.0040	FR408HR
Layer - 15	0.0006		**1/2oz P/G**
	0.0050	106 1080	FR408HR
Layer - 16	0.0006		**1/2oz Sig**
	0.0040	0.0040	FR408HR
Layer - 17	0.0006		**1/2oz P/G**
	0.0031	1080HRC	FR408HR
Layer - 18	0.0020		**1/2oz Sig (Std Plt)**
	0.0005		Taiyo 4000-BN

Figure 5: Initial ATCA carrier stack up. This was defined following discussion with the PCB manufacturer.

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