

**FPGA - CONFIGURATION - BANK 0 / BANK 14****20150112 PG 27**

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AF35	FPGA_TCK	TCK_0
AF34	FPGA_TMS	TMS_0
AG34	FPGA_TDO	TDO_0
AG35	FPGA_TDI	TDI_0
AE10	FPGA_PROG	PROGRAM_B_0
AE11	FPGA_DONE	DONE_0
AE34	SCK - FLASH	CCLK_0
BC27	SI/IO0 - FLASH	IO_L1P_T0_D00_MOSI_14
BD27	SO/IO1 - FLASH	IO_L2P_T0_D02_14
BD29	WP#/IO2 - FLASH	IO_L2N_T0_D03_14
BD30	HOLD#/IO3 - FLASH	IO_L2N_T0_D03_14
BA29	FLASH_CS#	IO_L6P_T0_FCS_B_14

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**FPGA - GENERAL PURPOSE I/O - BANK 14**


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AY31	OUTPUT	FPGA_CLK_SYNCn	SYNC CDCM6208 clock outputs (not really needed)	IO_L9P_T1_DQS_14
BA31	OUTPUT	FPGA_CLK_RSTn	Reset CDCM6208 clock chip	IO_L9NT1_DQS_D13_14
AY28	OUTPUT	FPGA_CLKSEL	Switch between local oscillator and ATLAS clock	IO_L10P_T1_D14_14
AV29	OPEN DRAIN	FPGA_SCL0	I2C clock line, from IPMC Sensor 0	IO_L14N_T2_SRCC_14
AN27	OPEN DRAIN	FPGA_SDA0	I2C data line	IO_L15P_T2_DQS_RDWR_B_14
AP27	OPEN DRAIN	FPGA_SCL1	I2C clock line, to Clock Synthesizer	IO_L15N_T2_DQS_DOUT_CSO_B_14
AT28	OPEN DRAIN	FPGA_SDA1	I2C data line	IO_L16P_T2_CSI_B_14
AP29	INPUT	FPGA_IPMC_PGOOD_A	Power Good	IO_L17P_T2_A14_D30_14
AP30	INPUT	FPGA_IPMC_PGOOD_B		IO_L17N_T2_A13_D29_14
AR28	INPUT	FPGA_IPMC_ALARM_B		IO_L18P_T2_A12_D28_14
AK28	INPUT	CLK_STATUS0	Status bit from CDCM6208 clock chip	IO_L21N_T3_DQS_A06_D22_14
AM27	INPUT	CLK_STATUS1	Status bit from CDCM6208 clock chip	IO_L22P_T3_A05_D21_14

## FPGA - AMC2 LVDS - BANK 14

## PG 27

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AV27	AMC2_LVDS_TX1P	IO_L12P_T1_MRCC_14
AV28	AMC2_LVDS_TX1N	IO_L12N_T1_MRCC_14
AU30	AMC2_LVDS_RX1P	IO_L13P_T2_MRCC_14
AV30	AMC2_LVDS_RX1N	IO_L13N_T2_MRCC_14
BB30	AMC2_LVDS_TX2P	IO_L4P_T0_D04_14
BC30	AMC2_LVDS_TX2N	IO_L4N_T0_D05_14
BC28	AMC2_LVDS_RX2P	IO_L5P_T0_D06_14
BC29	AMC2_LVDS_RX2N	IO_L5N_T0_D07_14
AW29	AMC2_LVDS_TX3P	IO_L7P_T1_D09_14
AY29	AMC2_LVDS_TX3N	IO_L7N_T1_D10_14
AW27	AMC2_LVDS_RX3P	IO_L8P_T1_D11_14
AY27	AMC2_LVDS_RX3N	IO_L8N_T1_D12_14
AJ29	AMC2_LVDS_TX4P	IO_L23P_T3_A03_D19_14
AK29	AMC2_LVDS_TX4N	IO_L23N_T3_A02_D18_14
AL28	AMC2_LVDS_RX4P	IO_L24P_T3_A01_D17_14
AL29	AMC2_LVDS_RX4N	IO_L24N_T3_A00_D16_14

## FPGA - AMC1 XAUI PORTS - BANK 114

PG 36

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AF4	AMC1_XAUI_TX0P	MGTXTP0_114_AF4
AF3	AMC1_XAUI_TX0N	MGTXTXN0_114_AF3
AD8	AMC1_XAUI_RX0P	MGTXRX0_114_AD8
AD7	AMC1_XAUI_RX0N	MGTXRXN0_114_AD7
AE2	AMC1_XAUI_TX1P	MGTXTP1_114_AE2
AE1	AMC1_XAUI_TX1N	MGTXTXN1_114_AE1
AC6	AMC1_XAUI_RX1P	MGTXRX1_114_AC6
AC5	AMC1_XAUI_RX1N	MGTXRXN1_114_AC5
AD4	AMC1_XAUI_TX2P	MGTXTP2_114_AD4
AD3	AMC1_XAUI_TX2N	MGTXTXN2_114_AD3
AA6	AMC1_XAUI_RX2P	MGTXRX2_114_AA6
AA5	AMC1_XAUI_RX2N	MGTXRXN2_114_AA5
AC2	AMC1_XAUI_TX3P	MGTXTP3_114_AC2
AC1	AMC1_XAUI_TX3N	MGTXTXN3_114_AC1
Y8	AMC1_XAUI_RX3P	MGTXRX3_114_Y8
Y7	AMC1_XAUI_RX3N	MGTXRXN3_114_Y7

## FPGA - AMC2 XAUI PORTS - BANK 115

PG 36

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AB4	AMC2_XAUI_TX0P	MGTXTP0_115_AB4
AB3	AMC2_XAUI_TX0N	MGTXTXN0_115_AB3
W6	AMC2_XAUI_RX0P	MGTXRX0_115_W6
W5	AMC2_XAUI_RX0N	MGTXRXN0_115_W5
AA2	AMC2_XAUI_TX1P	MGTXTP1_115_AA2
AA1	AMC2_XAUI_TX1N	MGTXTXN1_115_AA1
V8	AMC2_XAUI_RX1P	MGTXRX1_115_V8
V7	AMC2_XAUI_RX1N	MGTXRXN1_115_V7
Y4	AMC2_XAUI_TX2P	MGTXTP2_115_Y4
Y3	AMC2_XAUI_TX2N	MGTXTXN2_115_Y3
U6	AMC2_XAUI_RX2P	MGTXRX2_115_U6
U5	AMC2_XAUI_RX2N	MGTXRXN2_115_U5
W2	AMC2_XAUI_TX3P	MGTXTP3_115_W2
W1	AMC2_XAUI_TX3N	MGTXTXN3_115_W1
T8	AMC2_XAUI_RX3P	MGTXRX3_115_T8
T7	AMC2_XAUI_RX3N	MGTXRXN3_115_T7
U10	BK115_XAUI_CLK+	MGTREFCLK0P_115_U10
U9	BK115_XAUI_CLK-	MGTREFCLK0N_115_U9

## FPGA - AMC3 XAUI PORTS - BANK 116

PG 37

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V4	AMC3_XAUI_TX0P	MGTXTP0_116_V4
V3	AMC3_XAUI_TX0N	MGTXTXN0_116_V3
R6	AMC3_XAUI_RX0P	MGTXRX0_116_R6
R5	AMC3_XAUI_RX0N	MGTXRXN0_116_R5
U2	AMC3_XAUI_TX1P	MGTXTP1_116_U2
U1	AMC3_XAUI_TX1N	MGTXTXN1_116_U1
P8	AMC3_XAUI_RX1P	MGTXRX1_116_P8
P7	AMC3_XAUI_RX1N	MGTXRXN1_116_P7
T4	AMC3_XAUI_TX2P	MGTXTP2_116_T4
T3	AMC3_XAUI_TX2N	MGTXTXN2_116_T3
N6	AMC3_XAUI_RX2P	MGTXRX2_116_N6
N5	AMC3_XAUI_RX2N	MGTXRXN2_116_N5
R2	AMC3_XAUI_TX3P	MGTXTP3_116_R2
R1	AMC3_XAUI_TX3N	MGTXTXN3_116_R1
M8	AMC3_XAUI_RX3P	MGTXRX3_116_M8
M7	AMC3_XAUI_RX3N	MGTXRXN3_116_M7

## FPGA - AMC4 XAUI PORTS - BANK 117

PG 37

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P4	AMC4_XAUI_TX0P	MGTXTP0_117_P4
P3	AMC4_XAUI_TX0N	MGTXTXN0_117_P3
L6	AMC4_XAUI_RX0P	MGTXRX0_117_L6
L5	AMC4_XAUI_RX0N	MGTXRXN0_117_L5
N2	AMC4_XAUI_TX1P	MGTXTP1_117_N2
N1	AMC4_XAUI_TX1N	MGTXTXN1_117_N1
K8	AMC4_XAUI_RX1P	MGTXRX1_117_K8
K7	AMC4_XAUI_RX1N	MGTXRXN1_117_K7
M4	AMC4_XAUI_TX2P	MGTXTP2_117_M4
M3	AMC4_XAUI_TX2N	MGTXTXN2_117_M3
J6	AMC4_XAUI_RX2P	MGTXRX2_117_J6
J5	AMC4_XAUI_RX2N	MGTXRXN2_117_J5
L2	AMC4_XAUI_TX3P	MGTXTP3_117_L2
L1	AMC4_XAUI_TX3N	MGTXTXN3_117_L1
H8	AMC4_XAUI_RX3P	MGTXRX3_117_H8
H7	AMC4_XAUI_RX3N	MGTXRXN3_117_H7

## FPGA - XAUI FABRIC CHANNEL 1 - BANK 118

PG 37

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K4	Z2_BK118_XAUI_TX0P	MGTXTXP0_118_K4
K3	Z2_BK118_XAUI_TX0N	MGTXTXN0_118_K3
G6	Z2_BK118_XAUI_RX0P	MGTXRXPO_118_G6
G5	Z2_BK118_XAUI_RX0N	MGTXRXN0_118_G5
J2	Z2_BK118_XAUI_TX1P	MGTXTXP1_118_J2
J1	Z2_BK118_XAUI_TX1N	MGTXTXN1_118_J1
F8	Z2_BK118_XAUI_RX1P	MGTXRX1P_118_F8
F7	Z2_BK118_XAUI_RX1N	MGTXRXN1_118_F7
H4	Z2_BK118_XAUI_TX2P	MGTXTXP2_118_H4
H3	Z2_BK118_XAUI_TX2N	MGTXTXN2_118_H3
E6	Z2_BK118_XAUI_RX2P	MGTXRX2P_118_E6
E5	Z2_BK118_XAUI_RX2N	MGTXRXN2_118_E5
G2	Z2_BK118_XAUI_TX3P	MGTXTXP3_118_G2
G1	Z2_BK118_XAUI_TX3N	MGTXTXN3_118_G1
D8	Z2_BK118_XAUI_RX3P	MGTXRX3P_118_D8
D7	Z2_BK118_XAUI_RX3N	MGTXRXN3_118_D7
E10	BK118_XAUI_CLK+	MGTREFCLKOP_118_E10
E9	BK118_XAUI_CLK-	MGTREFCLKON_118_E9

## FPGA - XAUI FABRIC CHANNEL 2 - BANK 119

## PG 37

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F4	Z2_BK119_XAUI_TX0P	MGTXTXP0_119_F4
F3	Z2_BK119_XAUI_TX0N	MGTXTXN0_119_F3
D4	Z2_BK119_XAUI_RX0P	MGTXRXPO_119_D4
D3	Z2_BK119_XAUI_RX0N	MGTXRXN0_119_D3
E2	Z2_BK119_XAUI_TX1P	MGTXTXP1_119_E2
E1	Z2_BK119_XAUI_TX1N	MGTXTXN1_119_E1
C6	Z2_BK119_XAUI_RX1P	MGTXRX1P_119_C6
C5	Z2_BK119_XAUI_RX1N	MGTXRXN1_119_C5
C2	Z2_BK119_XAUI_TX2P	MGTXTXP2_119_C2
C1	Z2_BK119_XAUI_TX2N	MGTXTXN2_119_C1
B8	Z2_BK119_XAUI_RX2P	MGTXRX2P_119_B8
B7	Z2_BK119_XAUI_RX2N	MGTXRXN2_119_B7
B4	Z2_BK119_XAUI_TX3P	MGTXTXP3_119_B4
B3	Z2_BK119_XAUI_TX3N	MGTXTXN3_119_B3
A6	Z2_BK119_XAUI_RX3P	MGTXRX3P_119_A6
A5	Z2_BK119_XAUI_RX3N	MGTXRXN3_119_A5

## FPGA - GBT ZONE 3 - BANK 213

## PG 38

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AK41	Z3_BK213_GBT_TX0P	MGTXTXP0_213_AK41
AK42	Z3_BK213_GBT_TX0N	MGTXTXN0_213_AK42
AK37	Z3_BK213_GBT_RX0P	MGTXRXPO_213_AK37
AK38	Z3_BK213_GBT_RX0N	MGTXRXN0_213_AK38
AJ43	Z3_BK213_GBT_TX1P	MGTXTXP1_213_AJ43
AJ44	Z3_BK213_GBT_TX1N	MGTXTXN1_213_AJ44
AJ39	Z3_BK213_GBT_RX1P	MGTXRX1P_213_AJ39
AJ40	Z3_BK213_GBT_RX1N	MGTXRXN1_213_AJ40
AH41	Z3_BK213_GBT_TX2P	MGTXTXP2_213_AH41
AH42	Z3_BK213_GBT_TX2N	MGTXTXN2_213_AH42
AG39	Z3_BK213_GBT_RX2P	MGTXRX2P_213_AG39
AG40	Z3_BK213_GBT_RX2N	MGTXRXN2_213_AG40
AG43	Z3_BK213_GBT_TX3P	MGTXTXP3_213_AG43
AG44	Z3_BK213_GBT_TX3N	MGTXTXN3_213_AG44
AE39	Z3_BK213_GBT_RX3P	MGTXRX3P_213_AE39
AE40	Z3_BK213_GBT_RX3N	MGTXRXN3_213_AE40

## FPGA - GBT AMC1 &amp; ZONE 3 - BANK 214

## PG 38

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AF41	Z3_AMC1_BK213_GBT_T	MGTXTXP0_214_AF41
AF42	Z3_AMC1_BK213_GBT_T	MGTXTXN0_214_AF42
AD37	Z3_AMC1_BK213_GBT_R	MGTXRXPO_214_AD37
AD38	Z3_AMC1_BK213_GBT_R	MGTXRXN0_214_AD38
AE43	AMC1_BK213_GBT_TX1P	MGTXTXP1_214_AE43
AE44	AMC1_BK213_GBT_TX1N	MGTXTXN1_214_AE44
AC39	AMC1_BK213_GBT_RX1F	MGTXRX1P_214_AC39
AC40	AMC1_BK213_GBT_RX1N	MGTXRXN1_214_AC40
AD41	AMC1_BK213_GBT_TX2P	MGTXTXP2_214_AD41
AD42	AMC1_BK213_GBT_TX2N	MGTXTXN2_214_AD42
AA39	AMC1_BK213_GBT_RX2F	MGTXRX2P_214_AA39
AA40	AMC1_BK213_GBT_RX2N	MGTXRXN2_214_AA40
AC43	AMC1_BK213_GBT_TX3P	MGTXTXP3_214_AC43
AC44	AMC1_BK213_GBT_TX3N	MGTXTXN3_214_AC44
Y37	AMC1_BK213_GBT_RX3F	MGTXRX3P_214_Y37
Y38	AMC1_BK213_GBT_RX3N	MGTXRXN3_214_Y38
AA35	GBT_REFCLK0_BK214+	MGTREFCLK0P_214_AA35
AA36	GBT_REFCLK0_BK214-	MGTREFCLK0N_214_AA36
AB37	GBT_REFCLK1_BK214+	MGTREFCLK1P_214_AB37
AB38	GBT_REFCLK1_BK214-	MGTREFCLK1N_214_AB38

## FPGA - GBT AMC2 &amp; ZONE 3 - BANK 215

PG 38

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AB41	Z3_AMC2_GBT_TX0P	MGTXXP0_215_AB41
AB42	Z3_AMC2_GBT_TX0N	MGTXXN0_215_AB42
W39	Z3_AMC2_GBT_RX0P	MGTXXP0_215_W39
W40	Z3_AMC2_GBT_RX0N	MGTXXN0_215_W40
AA43	AMC2_GBT_TX1P	MGTXXP1_215_AA43
AA44	AMC2_GBT_TX1N	MGTXXN1_215_AA44
V37	AMC2_GBT_RX1P	MGTXXP1_215_V37
V38	AMC2_GBT_RX1N	MGTXXN1_215_V38
Y41	AMC2_GBT_TX2P	MGTXXP2_215_Y41
Y42	AMC2_GBT_TX2N	MGTXXN2_215_Y42
U39	AMC2_GBT_RX2P	MGTXXP2_215_U39
U40	AMC2_GBT_RX2N	MGTXXN2_215_U40
W43	AMC2_GBT_TX3P	MGTXXP3_215_W43
W44	AMC2_GBT_TX3N	MGTXXN3_215_W44
T37	AMC2_GBT_RX3P	MGTXXP3_215_T37
T38	AMC2_GBT_RX3N	MGTXXN3_215_T38

## FPGA - GBT AMC3 &amp; ZONE 3 - BANK 216

## PG 39

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V41	Z3_AMC3_GBT_TX0P	MGTXTXP0_216_V41
V42	Z3_AMC3_GBT_TX0N	MGTXTXN0_216_V42
R39	Z3_AMC3_GBT_RX0P	MGTXRXPO_216_R39
R40	Z3_AMC3_GBT_RX0N	MGTXRXNO_216_R40
U43	AMC3_GBT_TX1P	MGTXTXP1_216_U43
U44	AMC3_GBT_TX1N	MGTXTXN1_216_U44
P37	AMC3_GBT_RX1P	MGTXRX1_216_P37
P38	AMC3_GBT_RX1N	MGTXRXN1_216_P38
T41	AMC3_GBT_TX2P	MGTXTXP2_216_T41
T42	AMC3_GBT_TX2N	MGTXTXN2_216_T42
N39	AMC3_GBT_RX2P	MGTXRX2_216_N39
N40	AMC3_GBT_RX2N	MGTXRXN2_216_N40
R43	AMC3_GBT_TX3P	MGTXTXP3_216_R43
R44	AMC3_GBT_TX3N	MGTXTXN3_216_R44
M37	AMC3_GBT_RX3P	MGTXRX3_216_M37
M38	AMC3_GBT_RX3N	MGTXRXN3_216_M38

## FPGA - GBT AMC4 &amp; ZONE 3 - BANK 217

## PG 39

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P41	Z3_AMC4_GBT_TX0P	MGTXTXP0_217_P41
P42	Z3_AMC4_GBT_TX0N	MGTXTXN0_217_P42
L39	Z3_AMC4_GBT_RX0P	MGTXRXPO_217_L39
L40	Z3_AMC4_GBT_RX0N	MGTXRXNO_217_L40
N43	AMC4_GBT_TX1P	MGTXTXP1_217_N43
N44	AMC4_GBT_TX1N	MGTXTXN1_217_N44
K37	AMC4_GBT_RX1P	MGTXRX1P_217_K37
K38	AMC4_GBT_RX1N	MGTXRXN1_217_K38
M41	AMC4_GBT_TX2P	MGTXTXP2_217_M41
M42	AMC4_GBT_TX2N	MGTXTXN2_217_M42
J39	AMC4_GBT_RX2P	MGTXRX2P_217_J39
J40	AMC4_GBT_RX2N	MGTXRXN2_217_J40
L43	AMC4_GBT_TX3P	MGTXTXP3_217_L43
L44	AMC4_GBT_TX3N	MGTXTXN3_217_L44
H37	AMC4_GBT_RX3P	MGTXRX3P_217_H37
H38	AMC4_GBT_RX3N	MGTXRXN3_217_H38
J35	GBT_REFCLK0_BK217+	MGTREFCLK0P_217_J35
J36	GBT_REFCLK0_BK217-	MGTREFCLK0N_217_J36
L35	GBT_REFCLK1_BK217+	MGTREFCLK1P_217_L35
L36	GBT_REFCLK1_BK217-	MGTREFCLK1N_217_L36

## FPGA - GbE AMC1 - 4 - BANK 218

## PG 39

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K41	AMC1_GbE_TXOP	MGTXTXP0_218_K41
K42	AMC1_GbE_TXON	MGTXTXN0_218_K42
G39	AMC1_GbE_RXOP	MGTXRXPO_218_G39
G40	AMC1_GbE_RXON	MGTXRXN0_218_G40
J43	AMC2_GbE_TXOP	MGTXTXP1_218_J43
J44	AMC2_GbE_TXON	MGTXTXN1_218_J44
F37	AMC2_GbE_RXOP	MGTXRX1_218_F37
F38	AMC2_GbE_RXON	MGTXRXN1_218_F38
H41	AMC3_GbE_TXOP	MGTXTXP2_218_H41
H42	AMC3_GbE_TXON	MGTXTXN2_218_H42
E39	AMC3_GbE_RXOP	MGTXRX2_218_E39
E40	AMC3_GbE_RXON	MGTXRXN2_218_E40
G43	AMC4_GbE_TXOP	MGTXTXP3_218_G43
G44	AMC4_GbE_TXON	MGTXTXN3_218_G44
D37	AMC4_GbE_RXOP	MGTXRX3_218_D37
D38	AMC4_GbE_RXON	MGTXRXN3_218_D38
E35	GbE_REFCLK_BK218+	MGTREFCLKOP_218_E35
E36	GbE_REFCLK_BK218-	MGTREFCLKON_218_E36

## FPGA - GbE TO IPMC &amp; ZONE 2 &amp; 3 - BANK 219

PG 39

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F41	FPGA_BK219_GbE_TX0P	MGTXTXP0_219_F41
F42	FPGA_BK219_GbE_TX0N	MGTXTXN0_219_F42
D41	FPGA_BK219_GbE_RX0P	MGTXRX0_219_D41
D42	FPGA_BK219_GbE_RX0N	MGTXRXN0_219_D42
E43	Z2_BK219_GbE_TX1P	MGTXTXP1_219_E43
E44	Z2_BK219_GbE_TX1N	MGTXTXN1_219_E44
C39	Z2_BK219_GbE_RX1P	MGTXRX1_219_C39
C40	Z2_BK219_GbE_RX1N	MGTXRXN1_219_C40
C43	Z2_BK219_GbE_TX2P	MGTXTXP2_219_C43
C44	Z2_BK219_GbE_TX2N	MGTXTXN2_219_C44
B37	Z2_BK219_GbE_RX2P	MGTXRX2_219_B37
B38	Z2_BK219_GbE_RX2N	MGTXRXN2_219_B38
B41	Z3_BK219_GbE_TX3P	MGTXTXP3_219_B41
B42	Z3_BK219_GbE_TX3N	MGTXTXN3_219_B42
A39	Z3_BK219_GbE_RX3P	MGTXRX3_219_A39
A40	Z3_BK219_GbE_RX3P	MGTXRXN3_219_A40

**DDR3 MEMORY INTERFACE - BANK 34****PG 40**

BA18	DDRdm0	IO_L1P_T0_34
BB18	DDRdata0	IO_L1N_T0_34
BC19	DDRdata1	IO_L2P_T0_34
BC18	DDRdata2	IO_L2N_T0_34
BB17	DDRdqs0	IO_L3P_T0_DQS_34
BC17	DDRdqs0n	IO_L3N_T0_DQS_34
BD17	DDRdata3	IO_L4P_T0_34
BD16	DDRdata4	IO_L4N_T0_34
BC15	DDRdata5	IO_L5P_T0_34
BD15	DDRdata6	IO_L5N_T0_34
BB16	DDRdata7	IO_L6P_T0_34
AW17	DDRdm1	IO_L7P_T1_34
AY16	DDRdata8	IO_L7N_T1_34
AY18	DDRdata9	IO_L8P_T1_34
AY17	DDRdata10	IO_L8N_T1_34
AW16	DDRdqs1	IO_L9P_T1_DQS_34
AW15	DDRdqs1n	IO_L9N_T1_DQS_34
BA16	DDRdata11	IO_L10P_T1_34
BA15	DDRdata12	IO_L10N_T1_34
AV18	DDRdata13	IO_L11P_T1_SRCC_34
AV17	DDRdata14	IO_L11N_T1_SRCC_34
AU15	DDRdata15	IO_L12P_T1_MRCC_34

**DDR3 MEMORY INTERFACE - BANK 35****PG 41**

BB22	DDRadr13	IO_L1P_T0_AD4P_35
BB21	DDRadr12	IO_L1N_T0_AD4N_35
BC22	DDRadr11	IO_L2P_T0_AD12P_35
BD22	DDRadr10	IO_L2P_T0_AD12N_35
BC20	DDRCLKp	IO_L3P_T0_DQS_AD5P_35
BD19	DDRCLKn	IO_L3N_T0_DQS_AD5N_35
BD21	DDRadr9	IO_L4P_T0_35
BD20	DDRadr8	IO_L4N_T0_35
BA21	DDRadr7	IO_L5P_T0_AD13P_35
BB20	DDRadr6	IO_L5N_T0_AD13N_35
BA20	DDRadr5	IO_L6P_T0_35
BA19	DDRadr4	IO_L6N_T0_VREF_35
AW22	DDRadr3	IO_L7P_T1_AD6P_35
AY22	DDRadr2	IO_L7N_T1_AD6N_35
AV20	DDRadr1	IO_L8P_T1_AD14P_35
AW20	DDRadr0	IO_L8N_T1_AD14N_35
AW21	DDRba2	IO_L9P_T1_DQS_AD7P_35
AY21	DDRba1	IO_L9N_T1_DQS_AD7N_35
AW19	DDRba0	IO_L10P_T1_AD15P_35
AY19	DDRrasn	IO_L10N_T1_AD15N_35
AU22	DDRcasn	IO_L11P_T1_SRCC_35
AV22	DDRwen	IO_L11N_T1_SRCC_35
AU20	DDRcsn	IO_L12P_T1_MRCC_35
AT21	SYSCLKp	IO_L13P_T2_MRCC_35
AU21	SYSCLKn	IO_L13N_T2_MRCC_35
AP21	DDRcke	IO_L15P_T2_DQS_35
AP20	DDRodt	IO_L15N_T2_DQS_35

**DDR3 MEMORY INTERFACE - BANK 36****PG 42**

AV14	DDRdata24	IO_L13P_T2_MRCC_36
AW14	DDRdata25	IO_L13N_T2_MRCC_36
AW11	DDRdata26	IO_L14P_T2_SRCC_36
AW10	DDRdata27	IO_L14N_T2_SRCC_36
AY13	DDRdqs3	IO_L15P_T2_DQS_36
BA13	DDRdqs3n	IO_L15N_T2_DQS_36
AY12	DDRdm3	IO_L16P_T2_36
AY11	DDRdata28	IO_L16N_T2_36
BA11	DDRdata29	IO_L17P_T2_36
BA10	DDRdata30	IO_L17N_T2_36
AY14	DDRdata31	IO_L18P_T2_36
BA14	DDRrstn	IO_L18N_T2_36
BB11	DDRdm2	IO_L19P_T3_36
BB12	DDRdata16	IO_L20P_T3_36
BC12	DDRdata17	IO_L20N_T3_36
BD12	DDRdqs2	IO_L21P_T3_DQS_36
BD11	DDRdqs2n	IO_L21N_T3_DQS_36
BB13	DDRdata18	IO_L22P_T3_36
BC13	DDRdata19	IO_L22N_T3_36
BC14	DDRdata20	IO_L23P_T3_36
BD14	DDRdata21	IO_L23N_T3_36
BC10	DDRdata22	IO_L24P_T3_36
BD10	DDRdata23	IO_L24N_T3_36

**FPGA - GPIO - BANK 15****PG 43**

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BA24	GPIO_LED_0_LS	IO_L6P_T0_15_BA24
BA25	GPIO_LED_1_LS	IO_L6N_T0_VREF_15_BA25
BA26	GPIO_LED_2_LS	IO_L5P_T0_AD9P_15_BA26
BB26	GPIO_LED_3_LS	IO_L5N_T0_AD9N_15_BB26
BB25	GPIO_LED_4_LS	IO_L3P_T0_DQS_AD1P_15_BB25
AY23	GPIO_LED_5_LS	IO_L8P_T1_AD10P_15_AY23
BA23	GPIO_LED_6_LS	IO_L8N_T1_AD10N_15_BA23
AV23	GPIO_LED_7_LS	IO_L11P_T1_SRCC_15_AV23
AU25	RECOVERED_CLKP	IO_L12P_T1_MRCC_15_AU25
AU26	RECOVERED_CLKN	IO_L12N_T1_MRCC_15_AU26

## FPGA - AMC1 LVDS - BANK 16

## PG 44

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AU33	AMC1_LVDS_TX1P	IO_L12P_T1_MRCC_16_AU33
AV33	AMC1_LVDS_TX1N	IO_L12N_T1_MRCC_16_AV33
AV32	AMC1_LVDS_RX1P	IO_L13P_T2_MRCC_16_AV32
AW32	AMC1_LVDS_RX1N	IO_L13N_T2_MRCC_16_AW32
AJ32	AMC1_LVDS_TX2P	IO_L4P_T0_16_AJ32
AK32	AMC1_LVDS_TX2N	IO_L4N_T0_16_AK32
AL30	AMC1_LVDS_RX2P	IO_L5P_T0_16_AL30
AM31	AMC1_LVDS_RX2N	IO_L5N_T0_16_AM31
AN32	AMC1_LVDS_TX3P	IO_L7P_T1_16_AN32
AN33	AMC1_LVDS_TX3N	IO_L7N_T1_16_AN33
AR33	AMC1_LVDS_RX3P	IO_L8P_T1_16_AR33
AT33	AMC1_LVDS_RX3N	IO_L8N_T1_16_AT33
BD31	AMC1_LVDS_TX4P	IO_L23P_T3_16_BD31
BD32	AMC1_LVDS_TX4N	IO_L23N_T3_16_BD32
BD34	AMC1_LVDS_RX4P	IO_L24P_T3_16_BD34
BD35	AMC1_LVDS_RX4N	IO_L24N_T3_16_BD35

## FPGA - AMC4 LVDS - BANK 18

## PG 45

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H30	AMC4_LVDS_TX1P	IO_L12P_T1_MRCC_18_H30
G30	AMC4_LVDS_TX1N	IO_L12N_T1_MRCC_18_G30
H32	AMC4_LVDS_RX1P	IO_L13P_T2_MRCC_18_H32
H33	AMC4_LVDS_RX1N	IO_L13N_T2_MRCC_18_H33
C32	AMC4_LVDS_TX2P	IO_L4P_T0_18_C32
C33	AMC4_LVDS_TX2N	IO_L4N_T0_18_C33
B31	AMC4_LVDS_RX2P	IO_L5P_T0_18_B31
B32	AMC4_LVDS_RX2N	IO_L5N_T0_18_B32
E31	AMC4_LVDS_TX3P	IO_L7P_T1_18_E31
D32	AMC4_LVDS_TX3N	IO_L7N_T1_18_D32
E32	AMC4_LVDS_RX3P	IO_L8P_T1_18_E32
E33	AMC4_LVDS_RX3N	IO_L8N_T1_18_E33
U32	AMC4_LVDS_TX4P	IO_L23P_T3_18_U32
U33	AMC4_LVDS_TX4N	IO_L23N_T3_18_U33
T33	AMC4_LVDS_RX4P	IO_L24P_T3_18_T33
R33	AMC4_LVDS_RX4N	IO_L24N_T3_18_R33

## FPGA - AMC3 LVDS - BANK 19

## PG 46

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H28	AMC3_LVDS_TX1P	IO_L12P_T1_MRCC_19_H28
H29	AMC3_LVDS_TX1N	IO_L12N_T1_MRCC_19_H29
K27	AMC3_LVDS_RX1P	IO_L13P_T2_MRCC_19_K27
J27	AMC3_LVDS_RX1N	IO_L13N_T2_MRCC_19_J27
C28	AMC3_LVDS_TX2P	IO_L4P_T0_19_C28
B28	AMC3_LVDS_TX2N	IO_L4N_T0_19_B28
B26	AMC3_LVDS_RX2P	IO_L5P_T0_19_B26
A26	AMC3_LVDS_RX2N	IO_L5N_T0_19_A26
G28	AMC3_LVDS_TX3P	IO_L7P_T1_19_G28
F28	AMC3_LVDS_TX3N	IO_L7N_T1_19_F28
F26	AMC3_LVDS_RX3P	IO_L8P_T1_19_F26
E26	AMC3_LVDS_RX3N	IO_L8N_T1_19_E26
R27	AMC3_LVDS_TX4P	IO_L23P_T3_19_R27
P27	AMC3_LVDS_TX4N	IO_L23N_T3_19_P27
U27	AMC3_LVDS_RX4P	IO_L24P_T3_19_U27
U28	AMC3_LVDS_RX4N	IO_L24N_T3_19_U28