BROOKHAVEN NATIONAL LABORATORY

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VMM1

Front-end ASIC for charge-interpolating micro-pattern gas detectors

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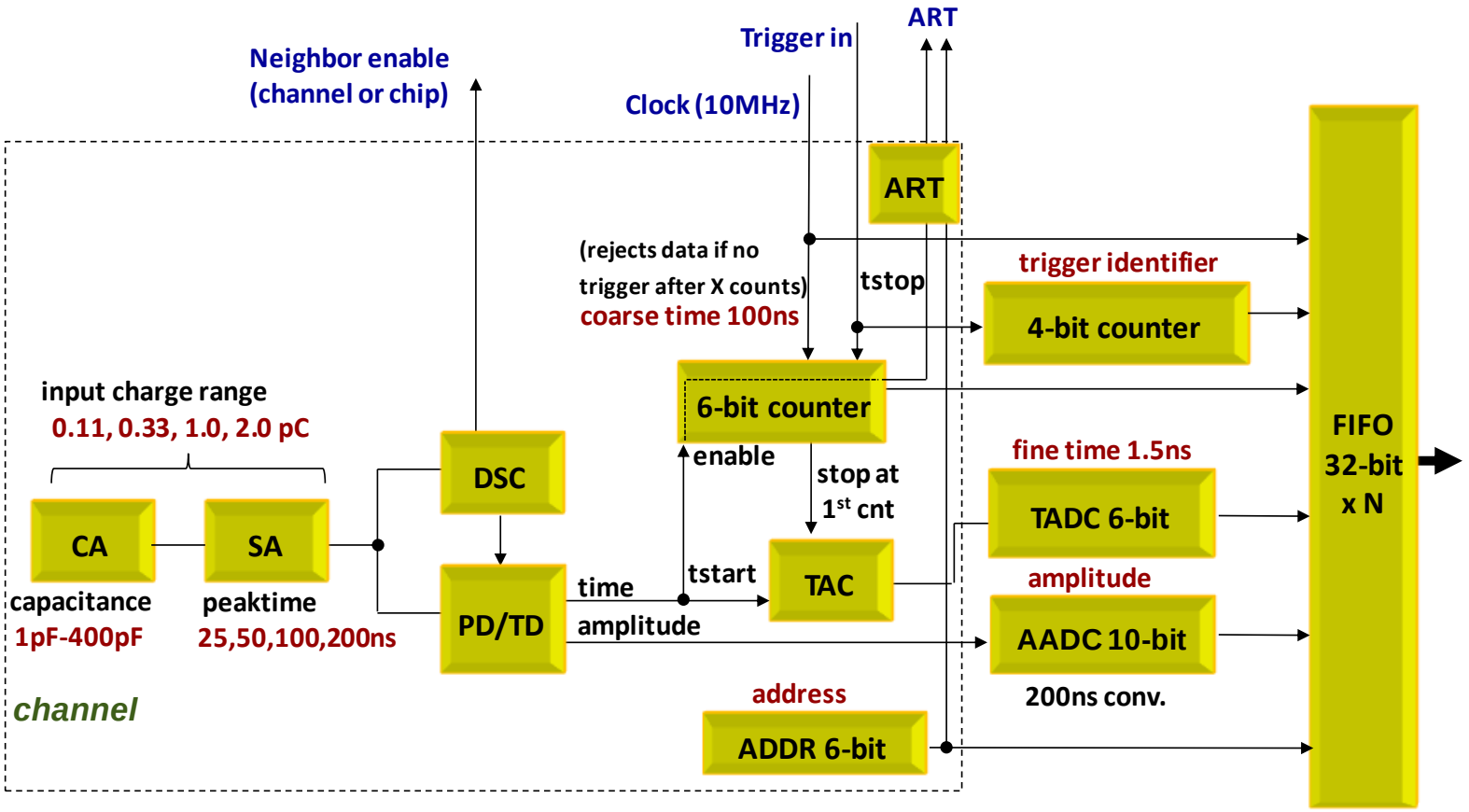
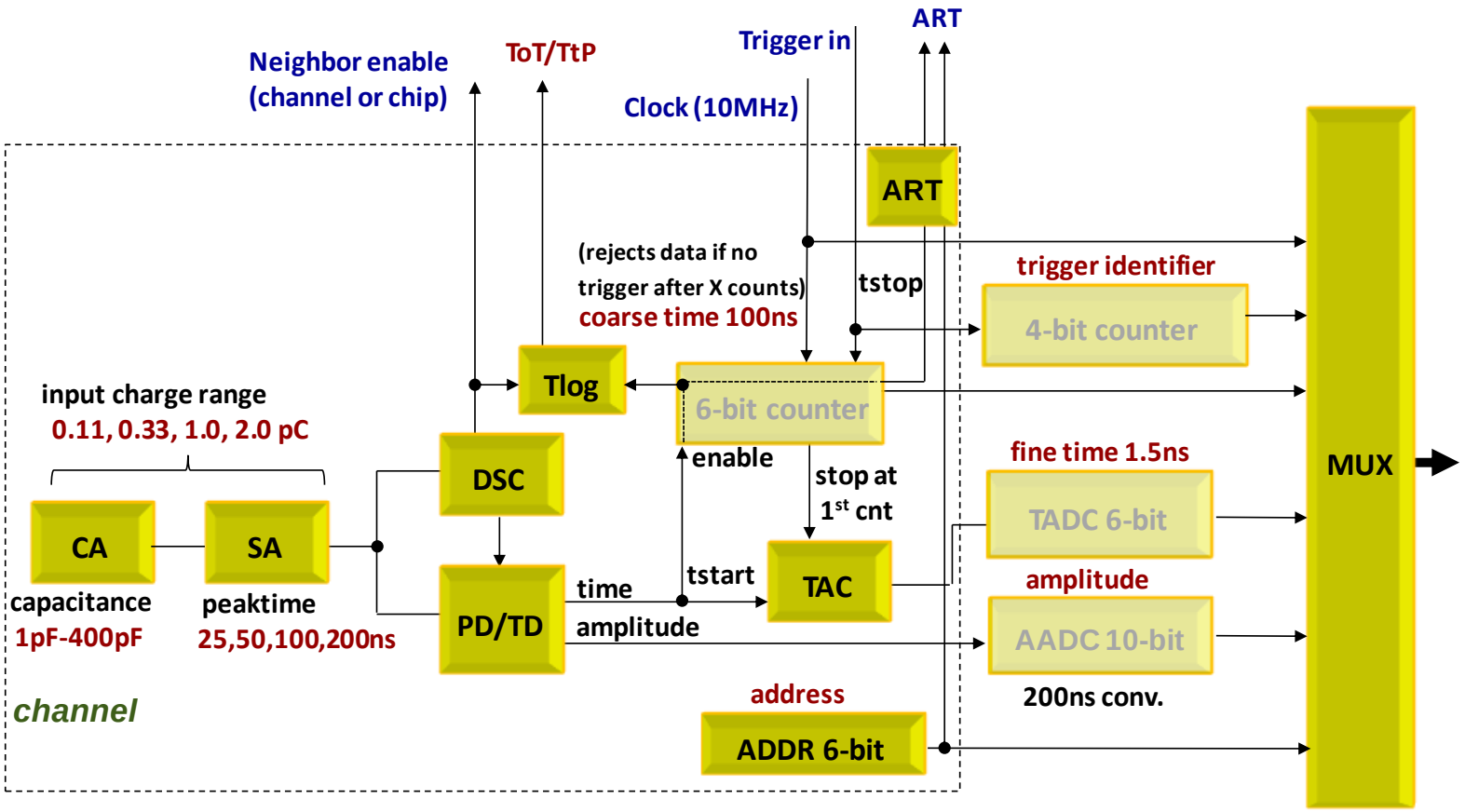
Targeted architecture



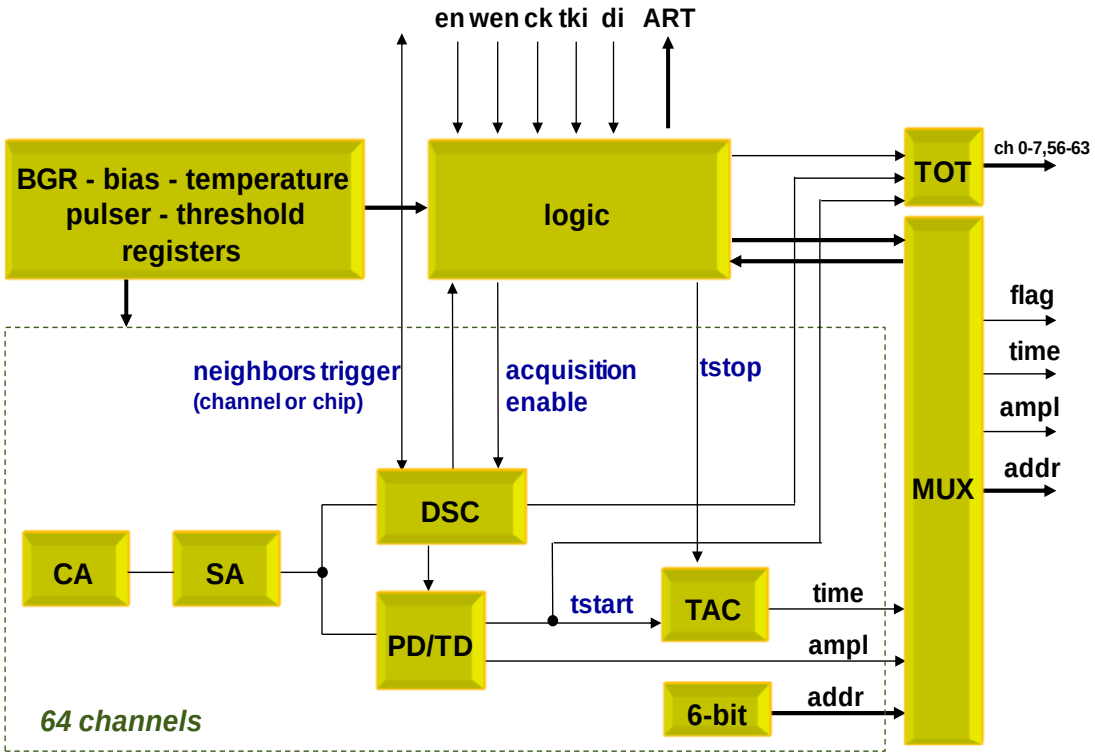
- **64 channels**, adj. polarity, adj. gain (**0.11 to 2 pC**), adj. peaktime (**25-200 ns**) ***note: interest in 5 pC***
- **peak** detection (10-bit) and **time** detection (1.5 ns)
- real-time **first address**
- sub-threshold **neighbor** acquisition (channel or chip)
- 10-bit single-trigger **ADCs**
- derandomizing **buffer** for continuous operation
- integrated threshold and pulse generators
- monitors, channel mask, temperature sensor, 600mV-LVDS interface
- ~ 5 mW per channel, CMOS 130 nm

Initial architecture (first prototype)



- 64 channels, integrates almost all of the **critical functions**
- **MUX** replaces ADCs and FIFO
- external trigger replaces **TAC stop**
- **ADC** architecture being in a separate project
- includes direct **ToT** (time-over-threshold) or **TtP** (time-to-peak) on 16 channels (0-7 and 56-63)
  note: interest in PdT (peak-discharge-to-threshold)

Operation and functions



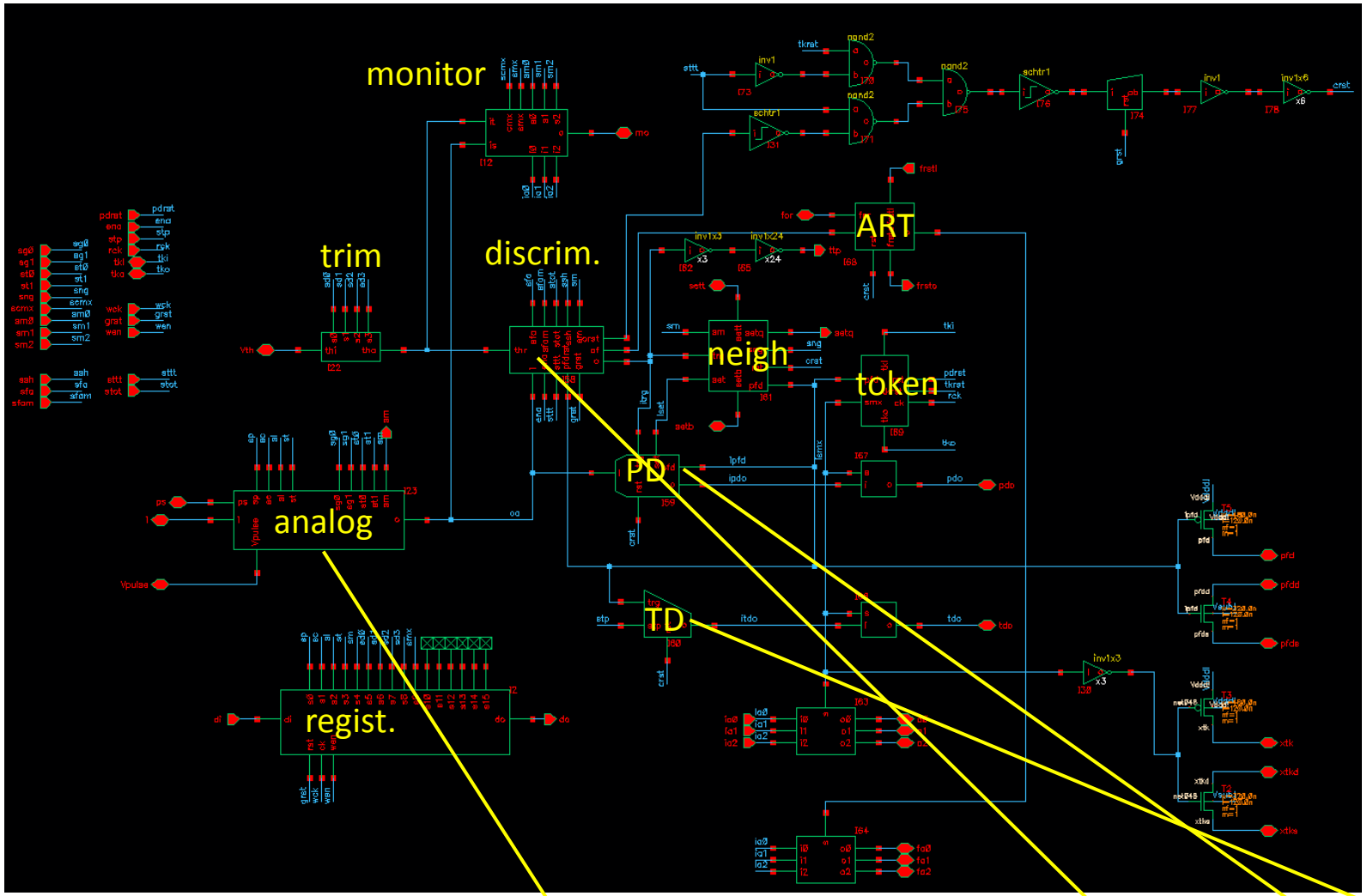
Modes of operation

- **acquisition**: events are detected and processed (amplitude and timing)
  - charge amplification, discrimination, **peak- and time-detection**
  - address in real time (**ART**) of the first event
  - direct timing (**ToT or TtP**) per channel for channels 0-7 and 56-63
- **readout**: sparse mode with **smart token** passing (amplitude, timing, addr.)
- **configuration**: access to global and channel registers

Functions

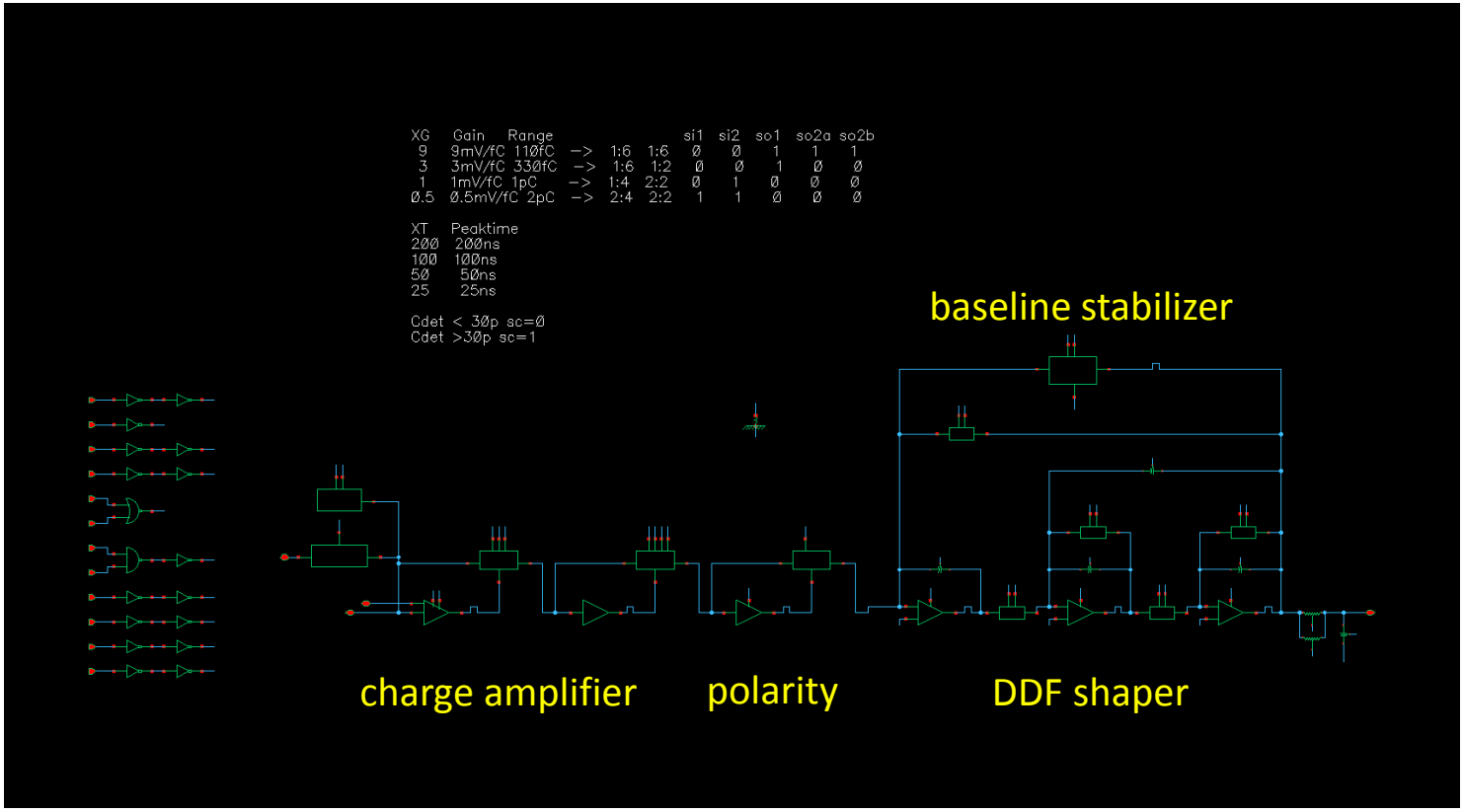
- **common**
  - temperature monitor
  - **pulse generator** (10-bit adjustable amplitude)
  - coarse threshold (10-bit adjustable)
  - **self-reset** option
  - analog monitors
    - analog, trim thresholds, BGR, DACs, temp.
    - analog buffers
- **analog section**
  - **charge amplifier (200pF)**, high-order **DDF shaper**
  - adjustable polarity (negative, positive)
  - gain: 0.5, 1, 3, 9 mV/fC (2, 1, 0.33, 0.11 pC)
  - peaktime: 25, 50, 100, 200 ns
  - test capacitor 1.2pF, channel mask
- **discriminator**
  - trimmer (4-bit adjustable, 1mV)
  - **sub-hysteresis** pulse processing option
  - neighbor logic on channels and chips (ch0, ch63)
- **peak detector multiphase**
- **time detector**
  - TAC ramp (selectable 100, 200, 500, 1000 ns)
  - start at peak-found
  - stop selectable (ena-low or stp-low)
- **ART**
  - address of the **first event in real time**
  - selectable at first threshold or at first peak
  - self-resets in 40ns
  - fflag indicates event
  - address available at fa0-fa5
- **timing per channel**
  - available for channels 0-7 and 56-63
  - selectable between **ToT and TtP**
- **readout**
  - flag at first peak indicates events to readout
  - sparse with **smart token** passing (skips empty chan.)
  - amplitude available at pdo
  - timing available at tdo
  - address available at a0-a5

Channel



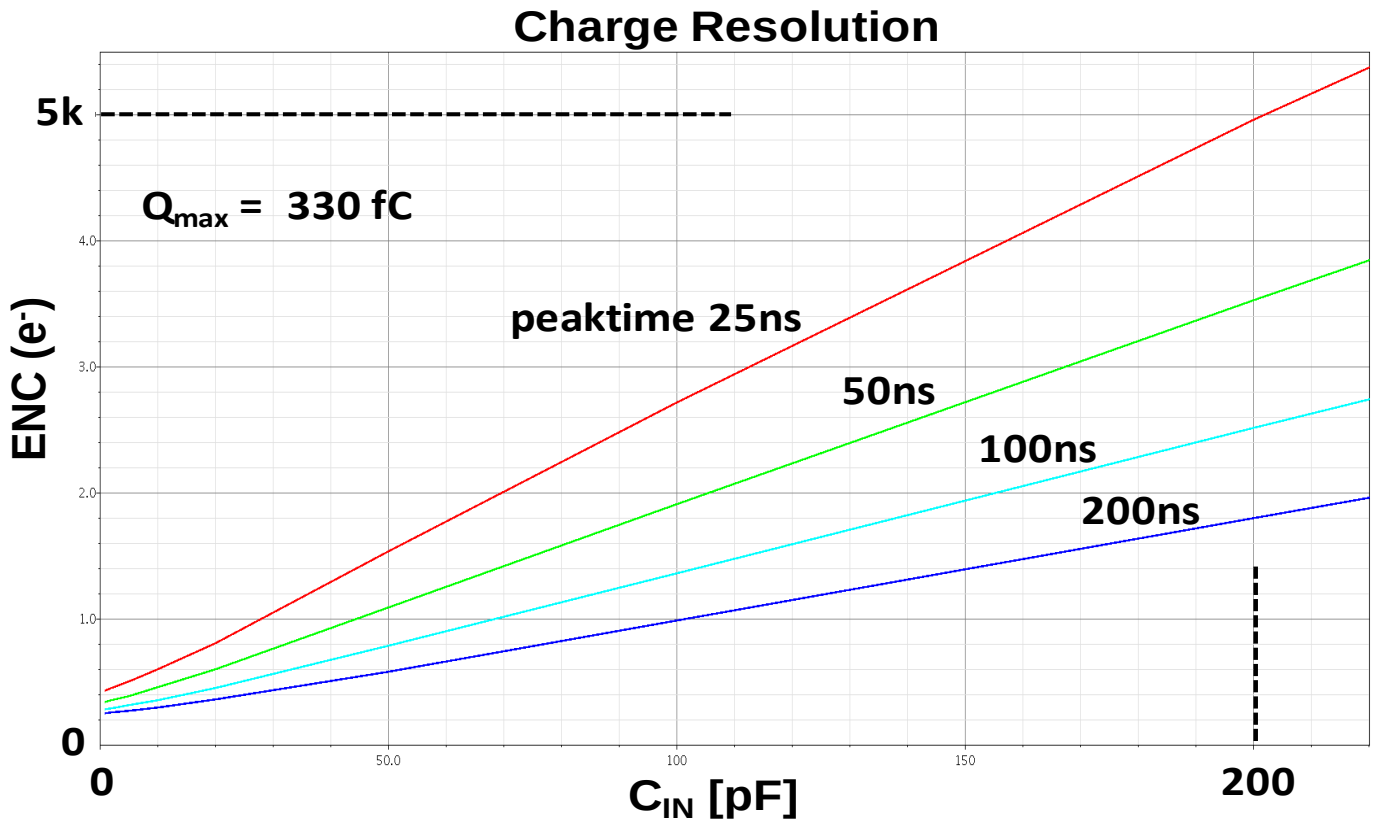
- size 4.7 mm x 100 µm
- power dissipation ~ 4mW at 25 ns peaktime

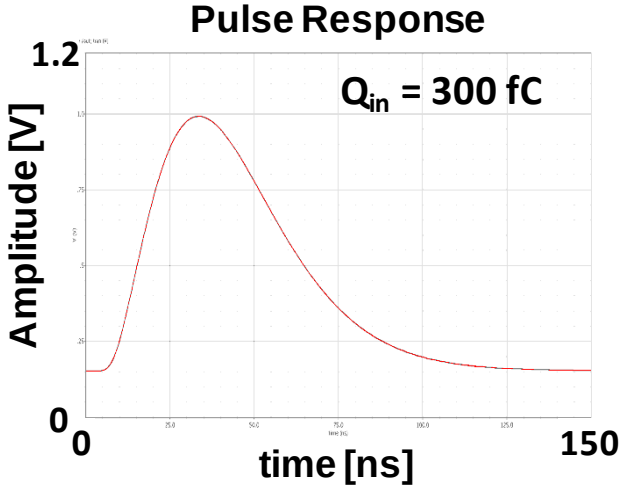
Analog section



- **charge amplifier**
  - two stages, continuous reset, adjustable gain: **0.5, 1, 3, 9 mV/fC (2, 1, 0.33, 011 pC)**
  - optimized for C_{DET} = 200 pF, can operate with C_{DET} = 1pF - 400pF
  - **input MOSFET**: NMOS W/L ≈ 10mm/180nm, I_D ≈ 1.65mA, P_D ≈ 2mW, C_G ≈ 18pF, g_m ≈ 38mS
- **shaper**
  - 3^{dr} order, complex-conjugate poles, **delayed-dissipative feedback** (DDF)
  - adjustable peaking time: **25, 50, 100, 200 ns**
- **baseline stabilizer** (BLH)

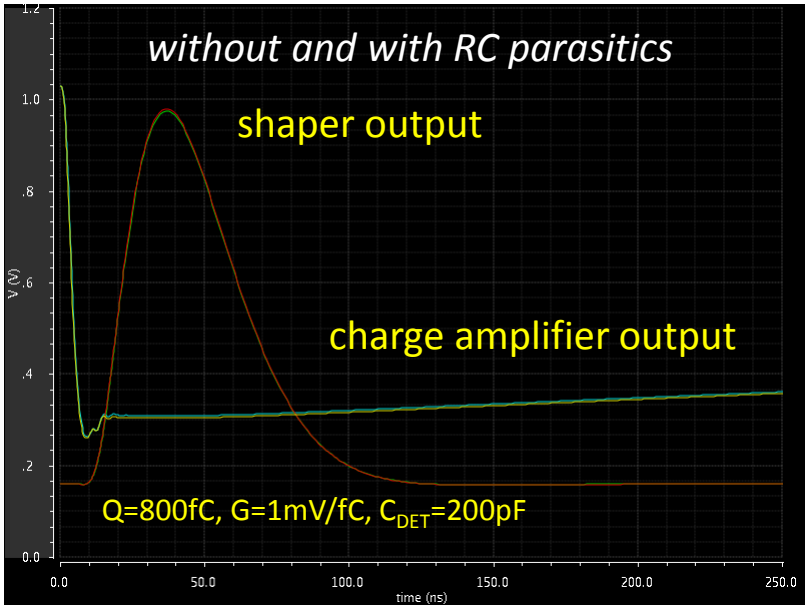
Analog section - simulations 1/2

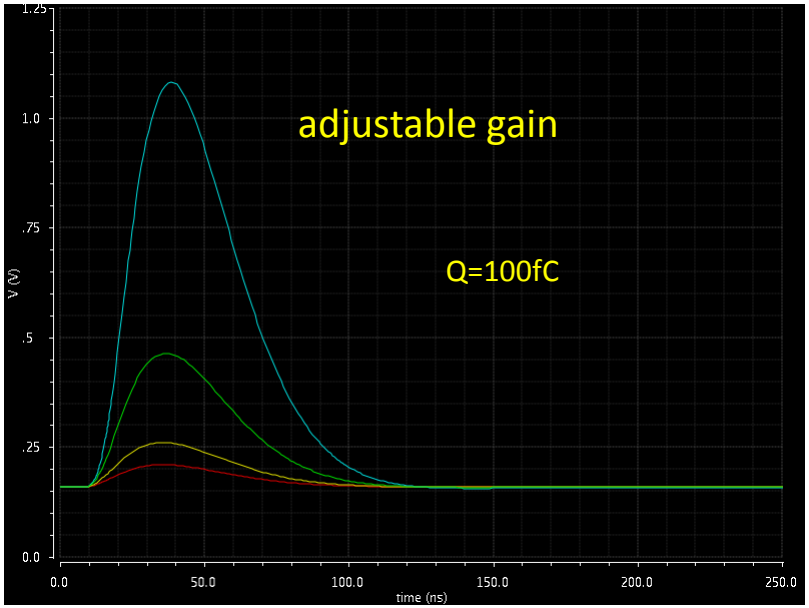


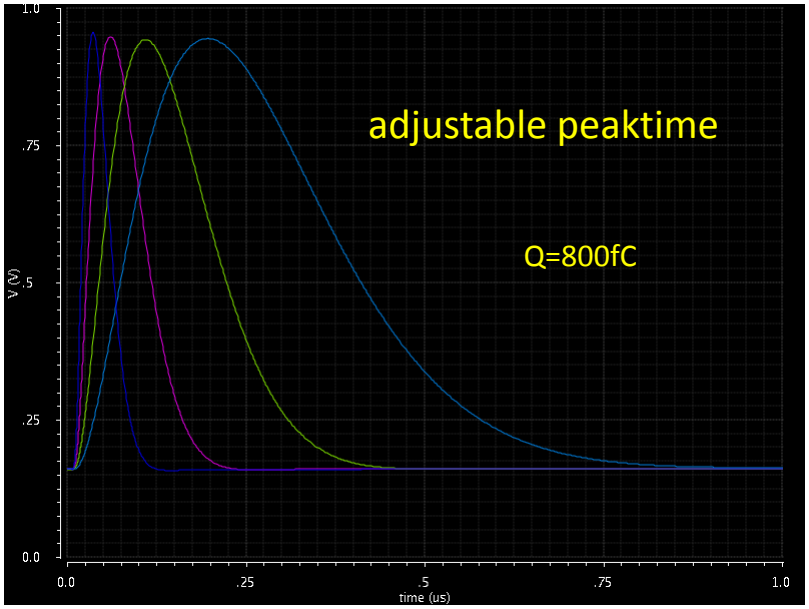


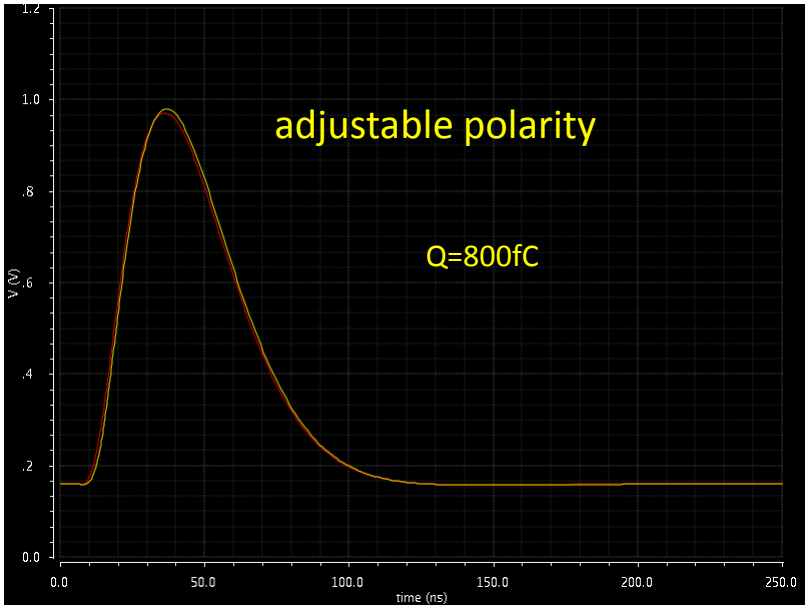
Target resolution < 5,000 e⁻ at 200 pF, 25 ns

Analog section - simulations 2/2



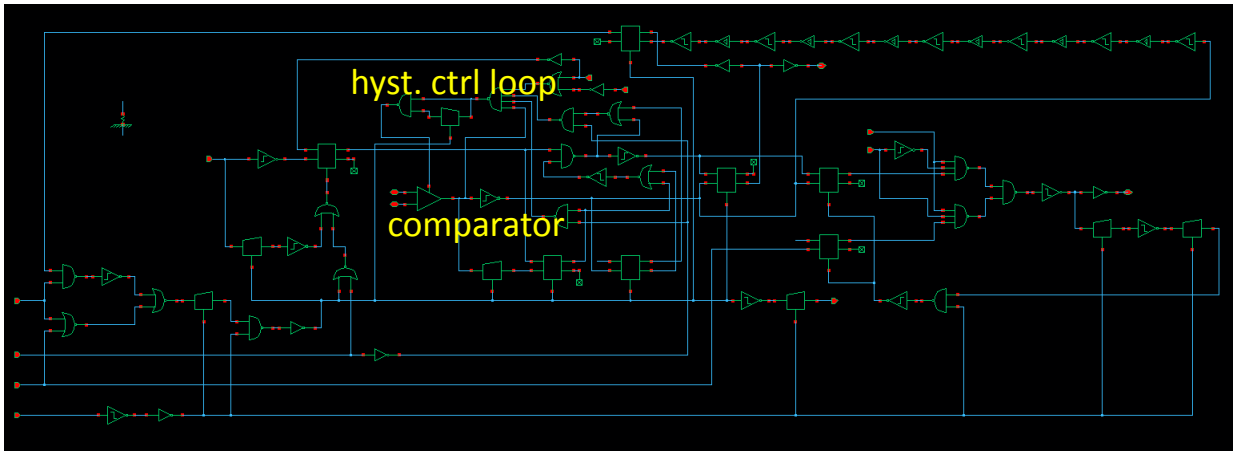


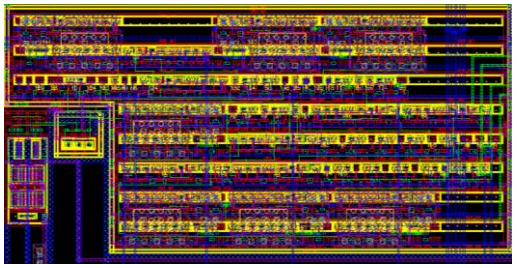




Discriminator and ART

Discriminator

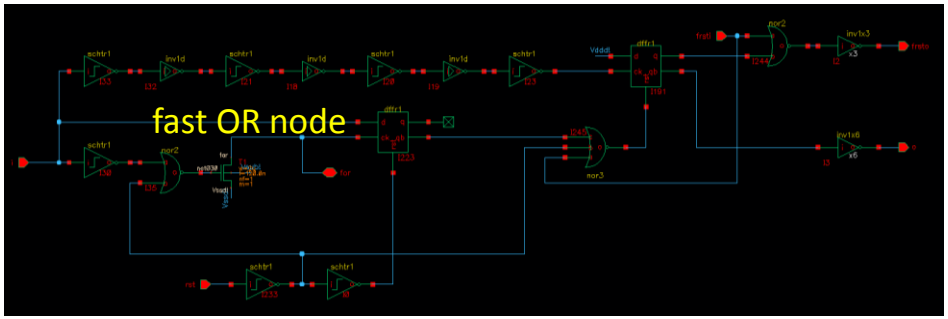


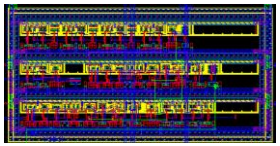


size 130 µm x 70 µm

- comparator hysteresis (positive feedback) ~ 20mV
- comparator response ~ 1ns
- hysteresis control loop reduces effective hysteresis to 1 mV
- can detect events down to 2 mV (signal dynamic range ~ 500)

ART

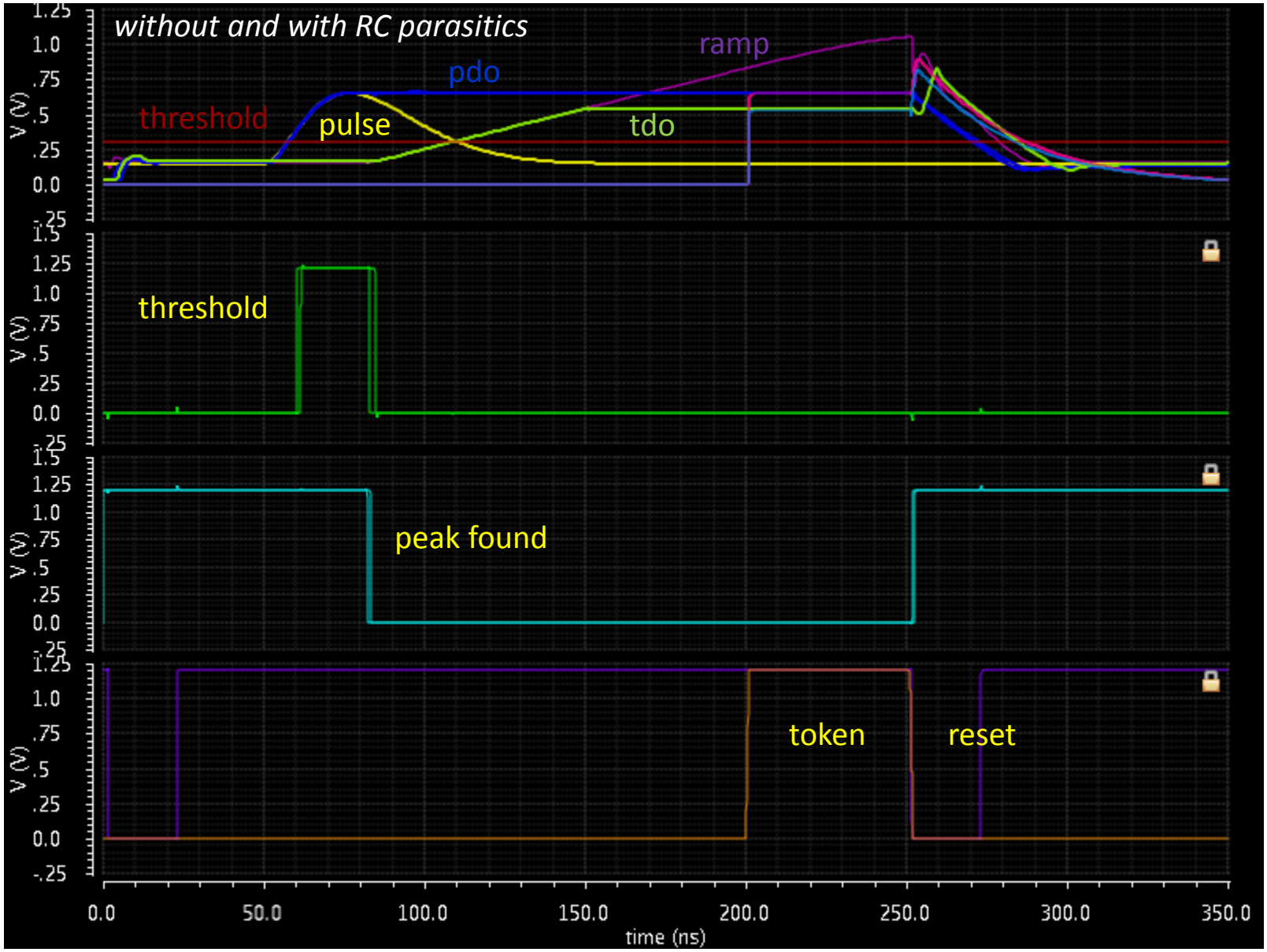




size 50 µm x 25 µm

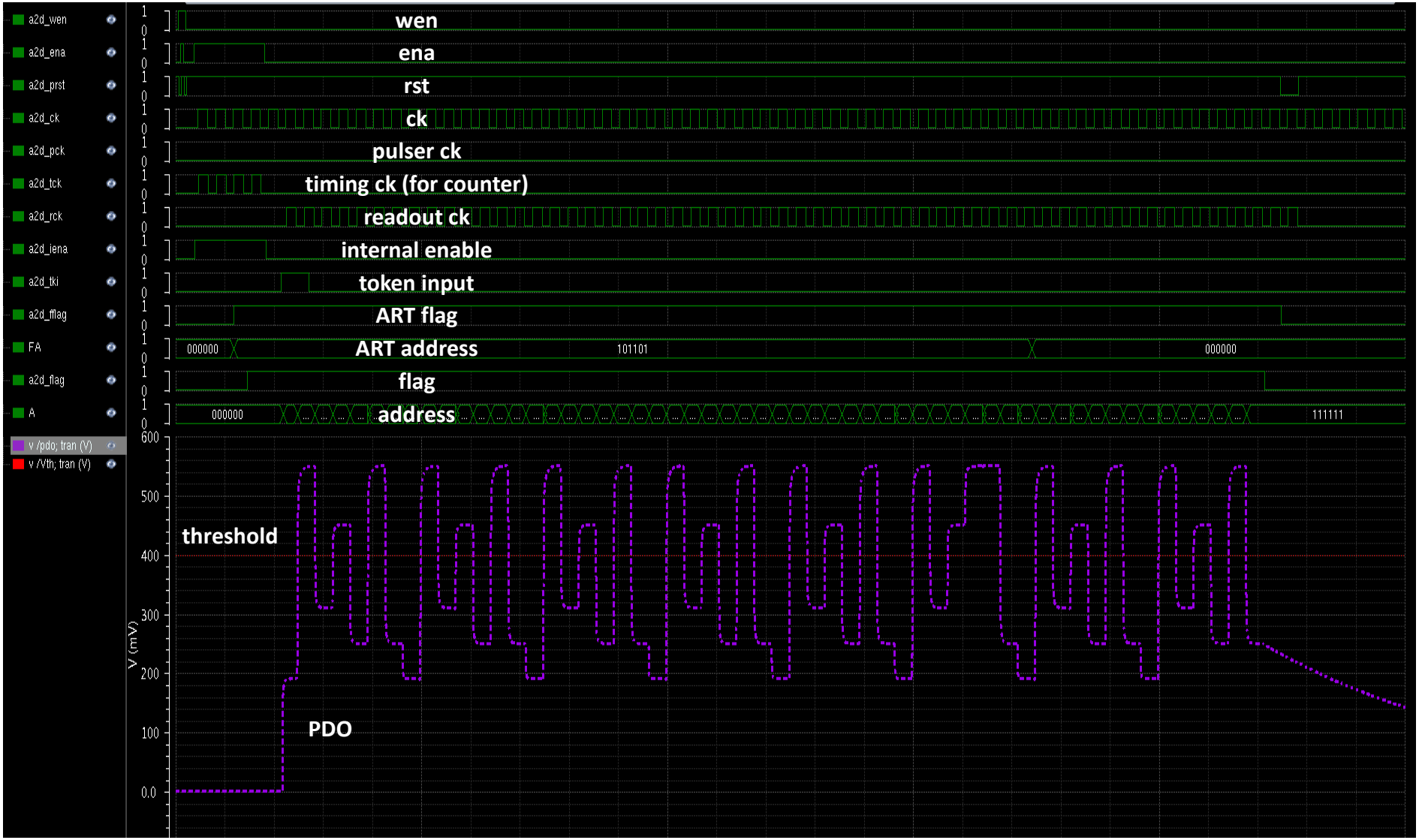
- ART (Address in Real Time) provides address first event
- uses fast OR, multiplexed twice (x 8 and x 8)
- response 2 ns
- within 2 ns, lowest order channel wins

Peak and time detectors - simulations



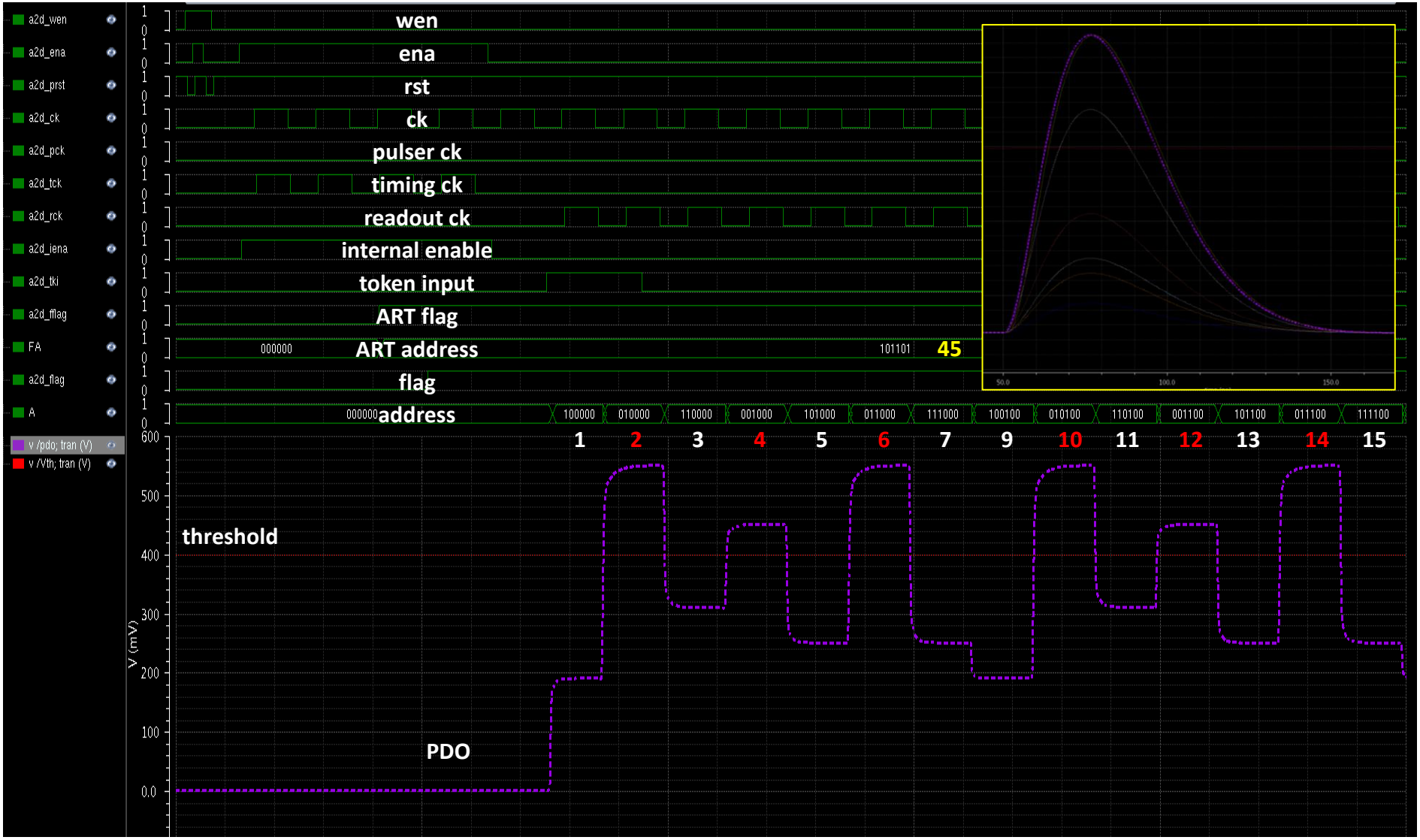
TAC stop signal at 150ns (not visible); timing at peak found (low time walk)

Readout - simulations 1/2



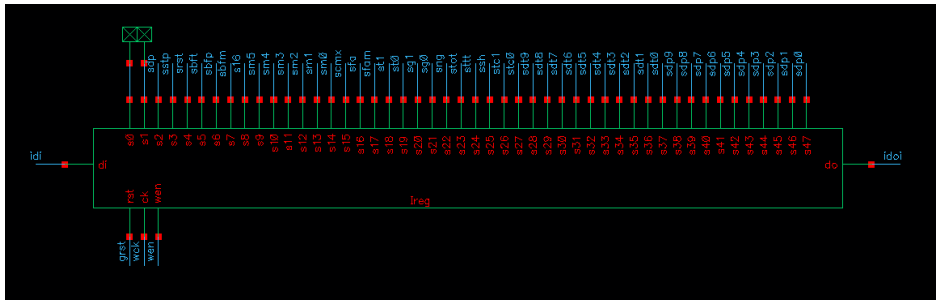
ART at threshold (selectable), flag at peak

Readout - simulations 2/2



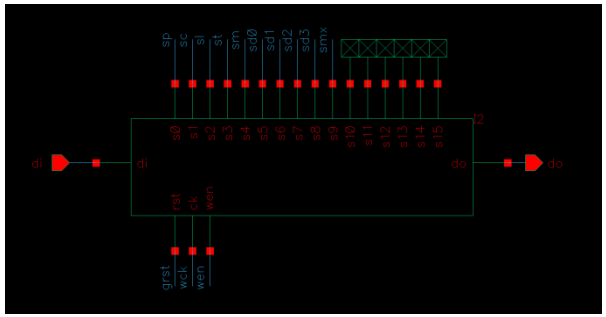
channels 2, 4, 6, 10, 12, 14 exceed threshold; neighbors are collected
channel 45 hits 2 ns earlier than others (ART)

Registers



Common bits

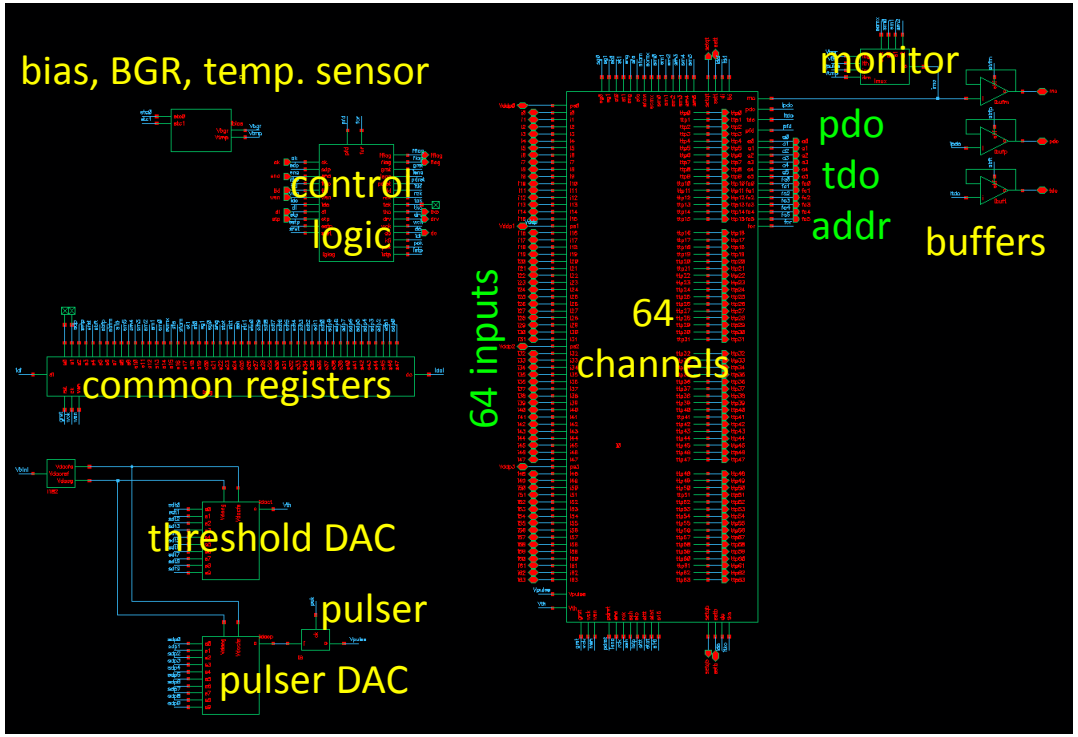
- **sg0,sg1**: **gain** (0.5, 1, 3, 9 mV/fC)(2, 1, 0.33, 0.11 pC)
- **st0,st1**: **peaktime** (25, 50, 100, 200 ns)
- **sng**: **neighbor** (channel and chip) triggering enable
- **stc0,stc1**: **TAC slope** (125, 250, 500, 1000 ns)
- **sdp**: **disable-at-peak**
- **scmx, sm0-sm5**: monitor multiplexing
- **sfa, sfam**: **ART** enable and mode (peak, threshold)
- **sbfm,sbfp,sbft**: buffers enable (mo, pdo, tdo)
- **sstp**: **TAC stop setting** (ena-low or stp-low)
- **ssh**: **sub-hysteresis** discrimination enable
- **sttt,stot**: timing outputs enable and mode (**ToT** or **TtP**)
- **s16**: makes **ch 7 neighbor to ch 56**
- **srst**: **self reset** enable (40ns after flag)
- **sdt0-sdt9**: coarse threshold DAC
- **sdp0-sdp9**: test pulse DAC



Channel bits

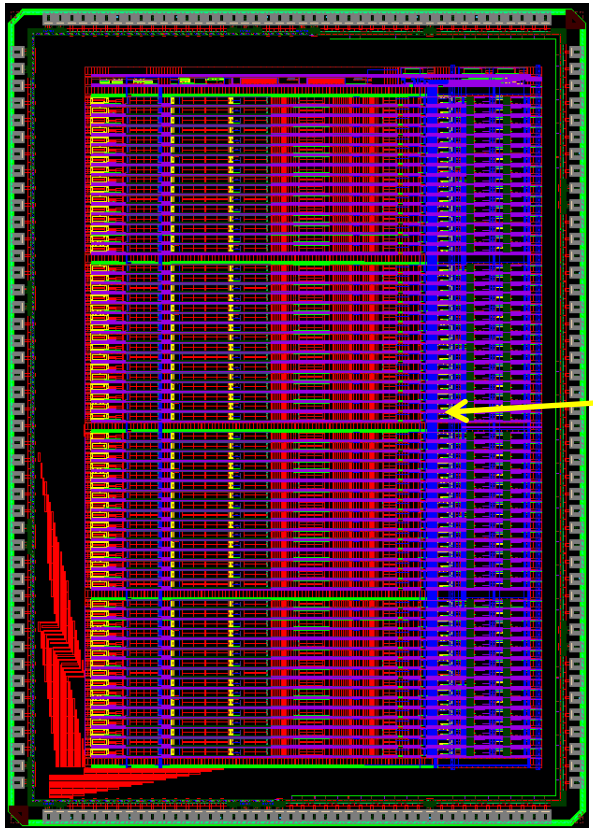
- **sp**: charge **polarity**
- **sc**: large input capacitance mode (C_{DET}>30pF)
- **sl**: leakage generator enable
- **st**: **test capacitor** enable
- **sm**: **mask** enable
- **sd0-sd3**: **trim** threshold DAC
- **smx**: mux monitor mode (**analog or trim threshold**)

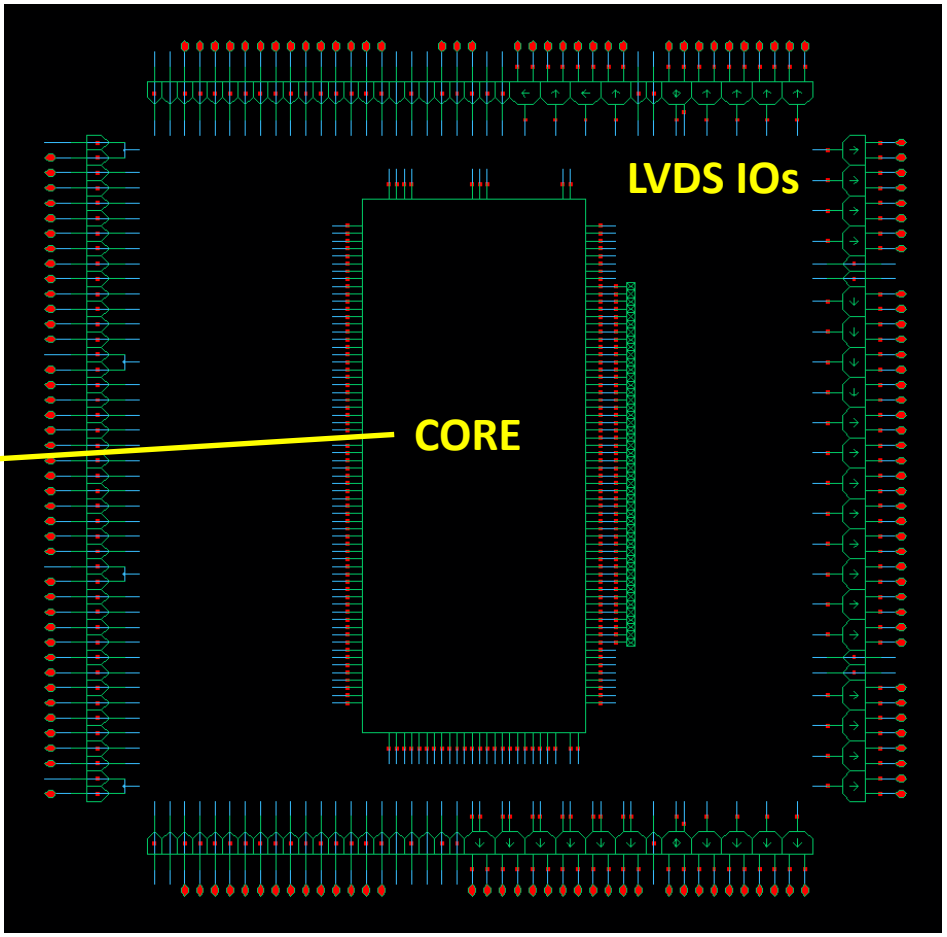
Core



- size 4.7 mm x 7.1 mm
- five banks of MOSCAP filters on bias lines
- power dissipation ~ 300 mW

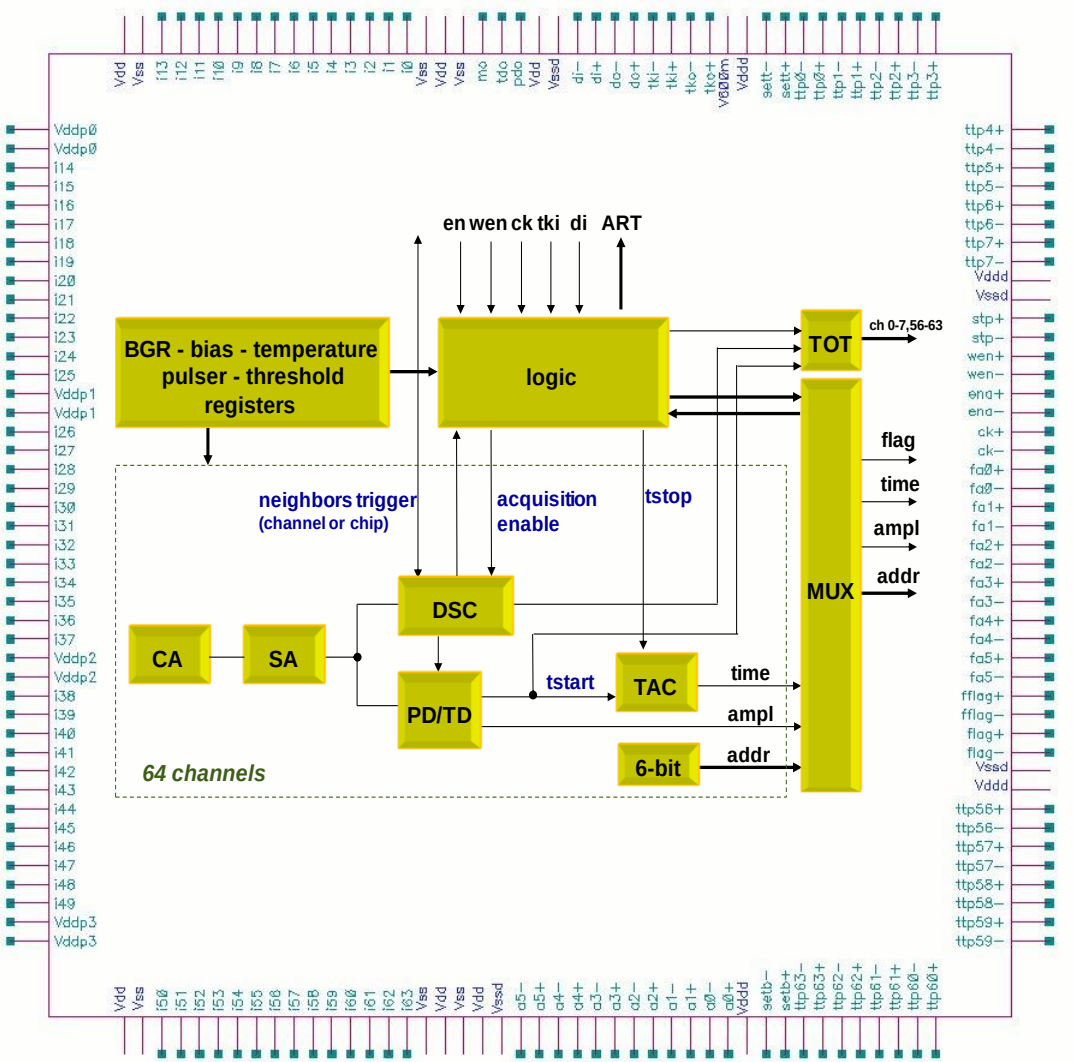
Top level





- size 5.9 mm x 8.4 mm

Pinout



Pinout

- **176** pins (44 each side)
- **Vdd,Vss**: analog supplies 1.2V and grounds 0V
- **Vddd, Vssd**: digital supplies 1.2V and grounds 0V
- **Vddp0-Vddp3**: charge amplifier supplies 1.2V
- **V600m**: reference for LVDS 600mV

- **i0-i63**: **analog inputs**, ESD protected
- **mo**: monitor multiplexed analog output
- **pdo**: **peak detector** multiplexed analog output
- **tdo**: **time detector** multiplexed analog output

- **flag**: event indicator
- **a0-a5**: multiplexed address, tristated (driven with token)
- **ttp0-ttp7** and **ttp56-ttp63**: **ToT or TtP**

- **fflag**: **ART** event indicator
- **fa0-fa5**: ART address output

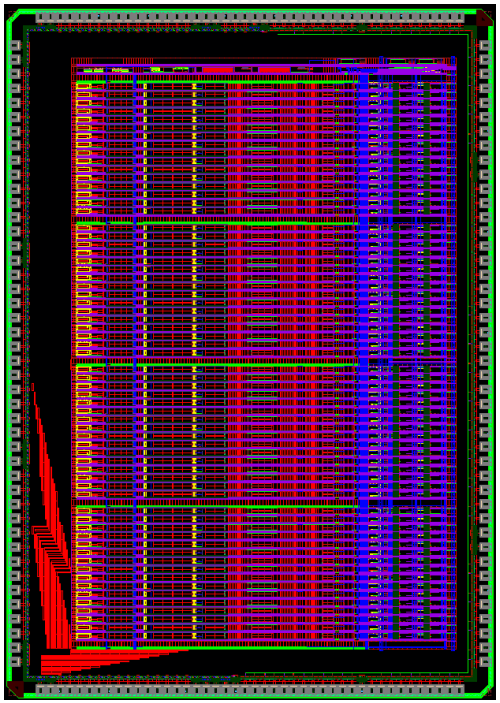
- **stp**: timing stop
- **sett, setb**: ch0, ch63 **neighbor** chip triggers (bi-directional)

- **ena**: acquisition enable
  - ena high, wen low: acquisition mode
  - ena low, wen low: readout mode
  - ena pulse, wen high: global reset
- **wen**: configuration enable
  - wen high: configuration mode
  - wen pulse: acquisition reset
- **ck**: clock
  - in acquisition mode ck is counter clock
  - in readout mode ck is readout clock
  - in configuration mode ck is writein clock

- **tki, tko**: token input and output (3/2 clock wider)
- **di, do**: data configuration input and output (1/2 clock shifted)
  - in acquisition mode di is pulser clock

Schedule and status

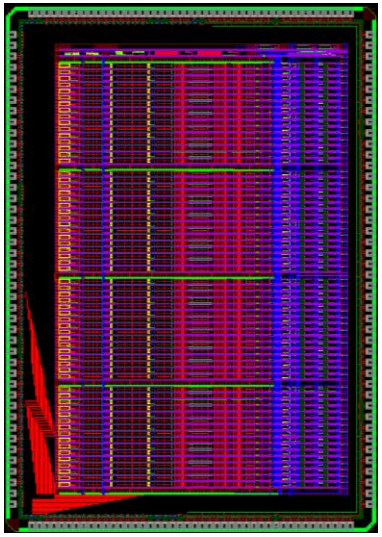
	scheduled	completed
Analog section	Jan 2011	February 2011
Peak/time section	March	April
Common circuitry	April	May
Digital sections	May	July
Physical layout	July	October
Fabrication	September	**Queued for November 7th**

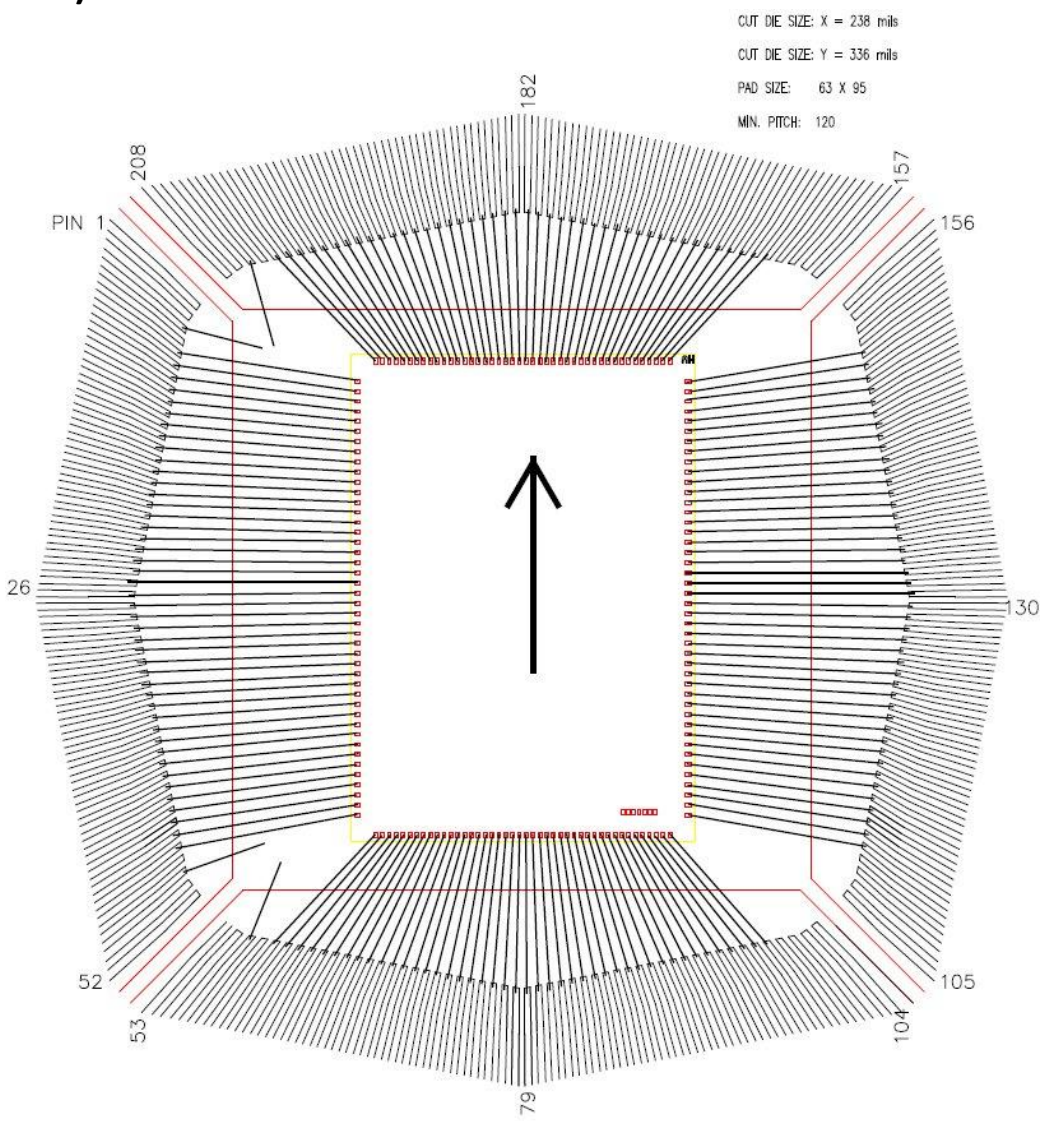


- **technology IBM 8RF CMOS 130 nm**
- **size 5.9 mm x 8.4 mm (~50mm²)**
- **pads count 176, package LQFP 176 ?**

Schedule and status: update March 2012

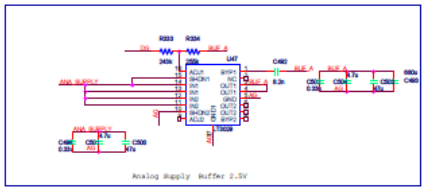
- Packaged in LQFP208 (instead of LQFP 176)
- Received from MOSIS 3/7/2012
- Test board fabricated 3/22/2012
- Test board assembled 3/29/2012
- DAQ development in progress

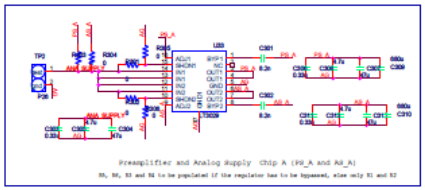


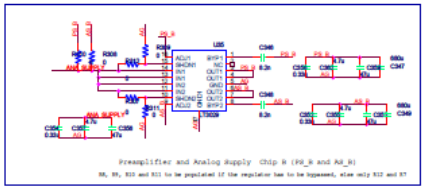


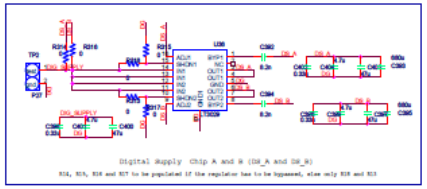
Downbonds at pins 3, 50, 55, 206

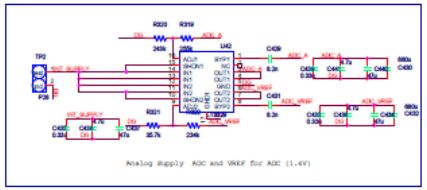
Status as of April 2nd, 2012 - Test Board

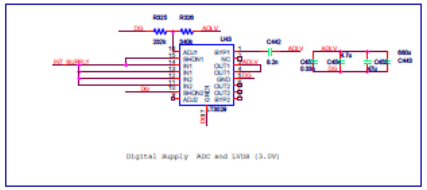


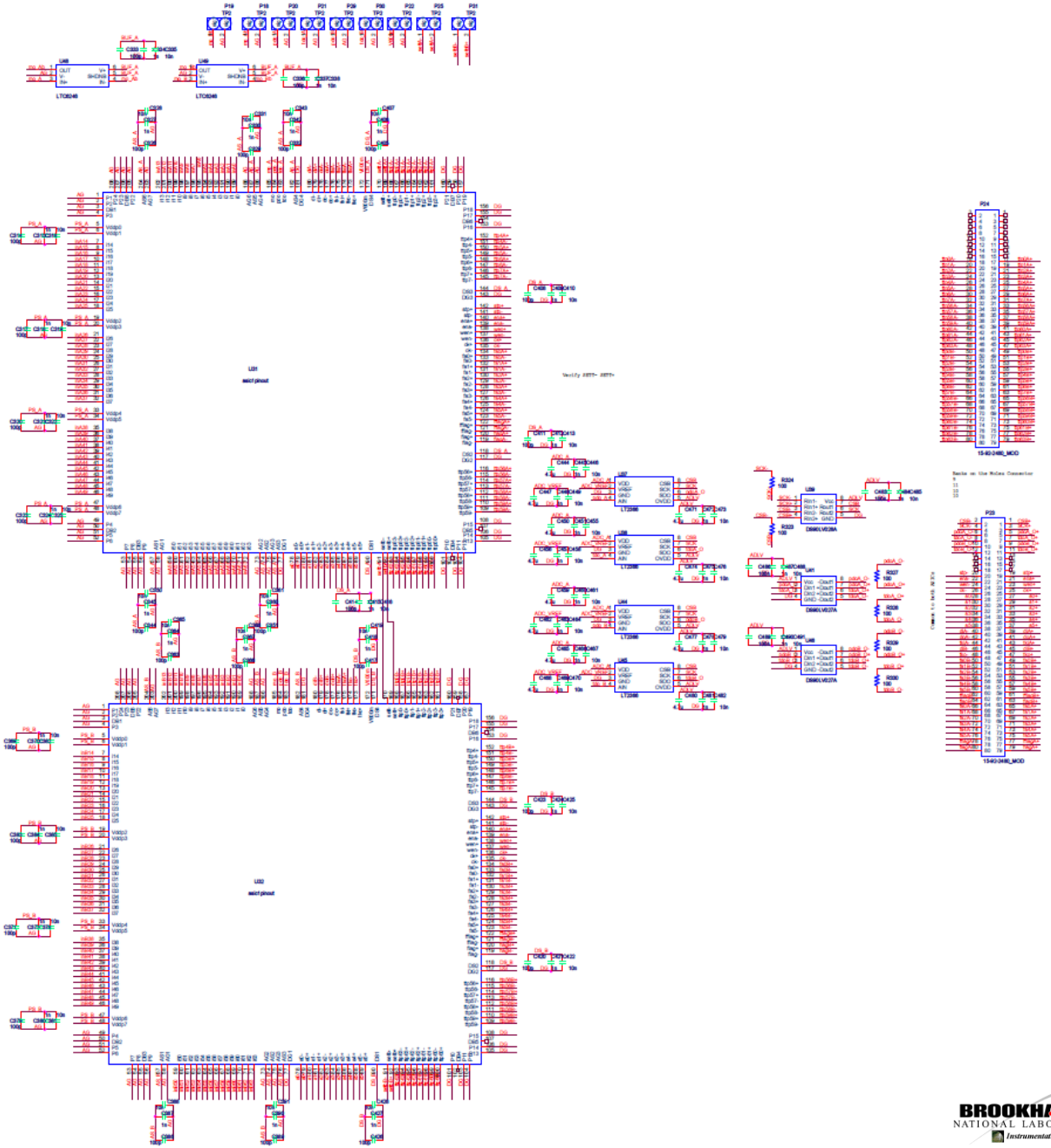




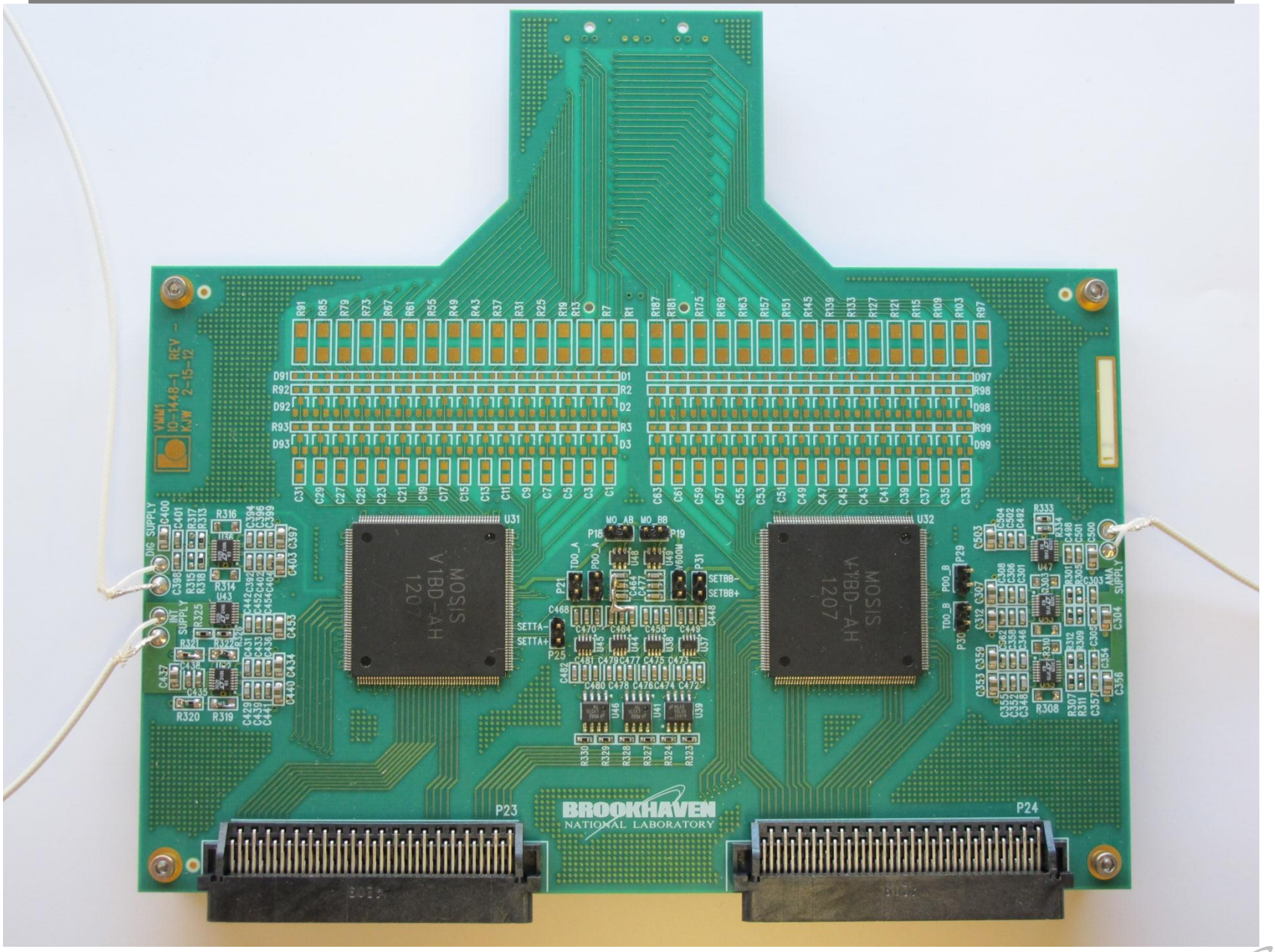




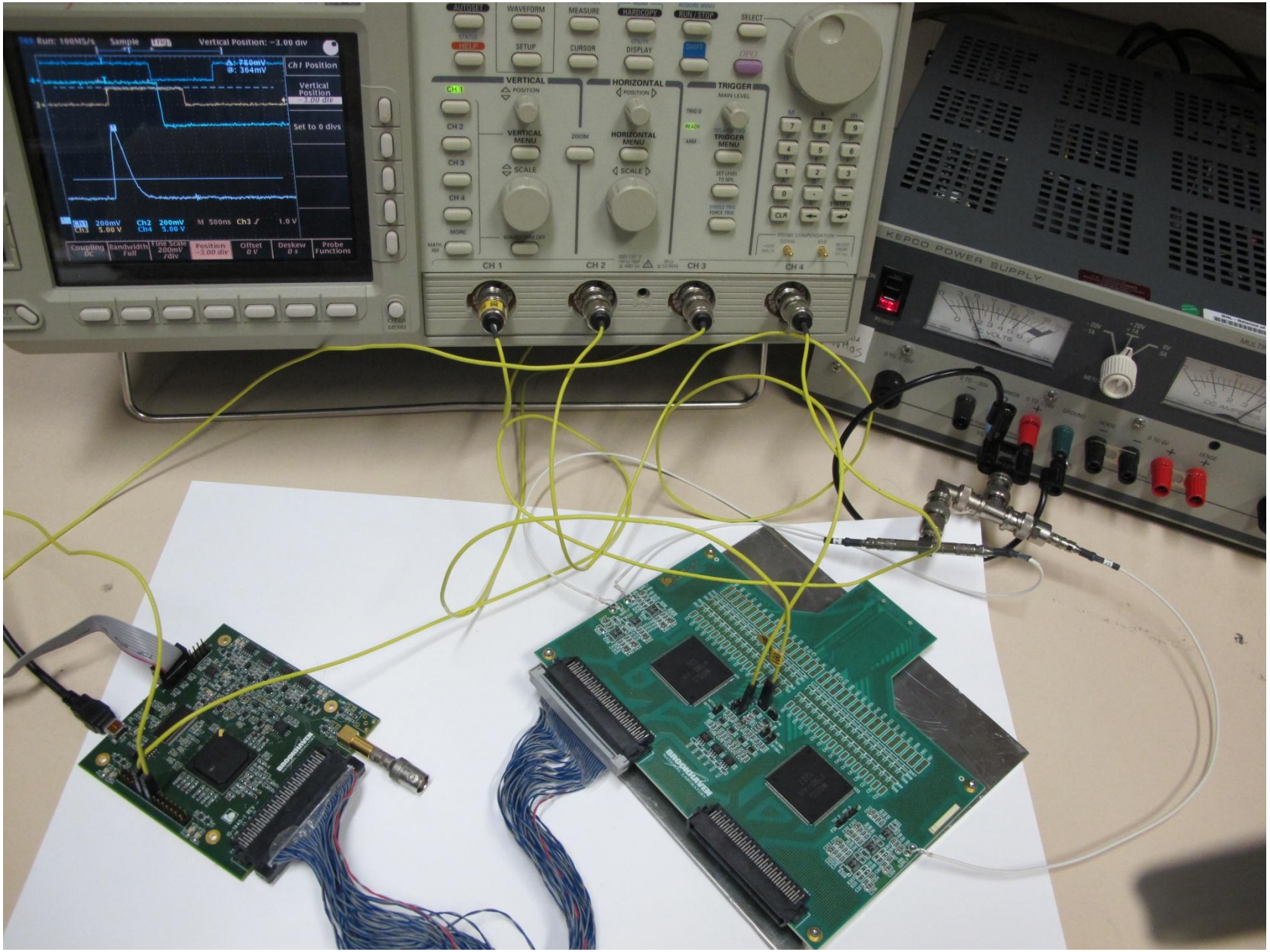




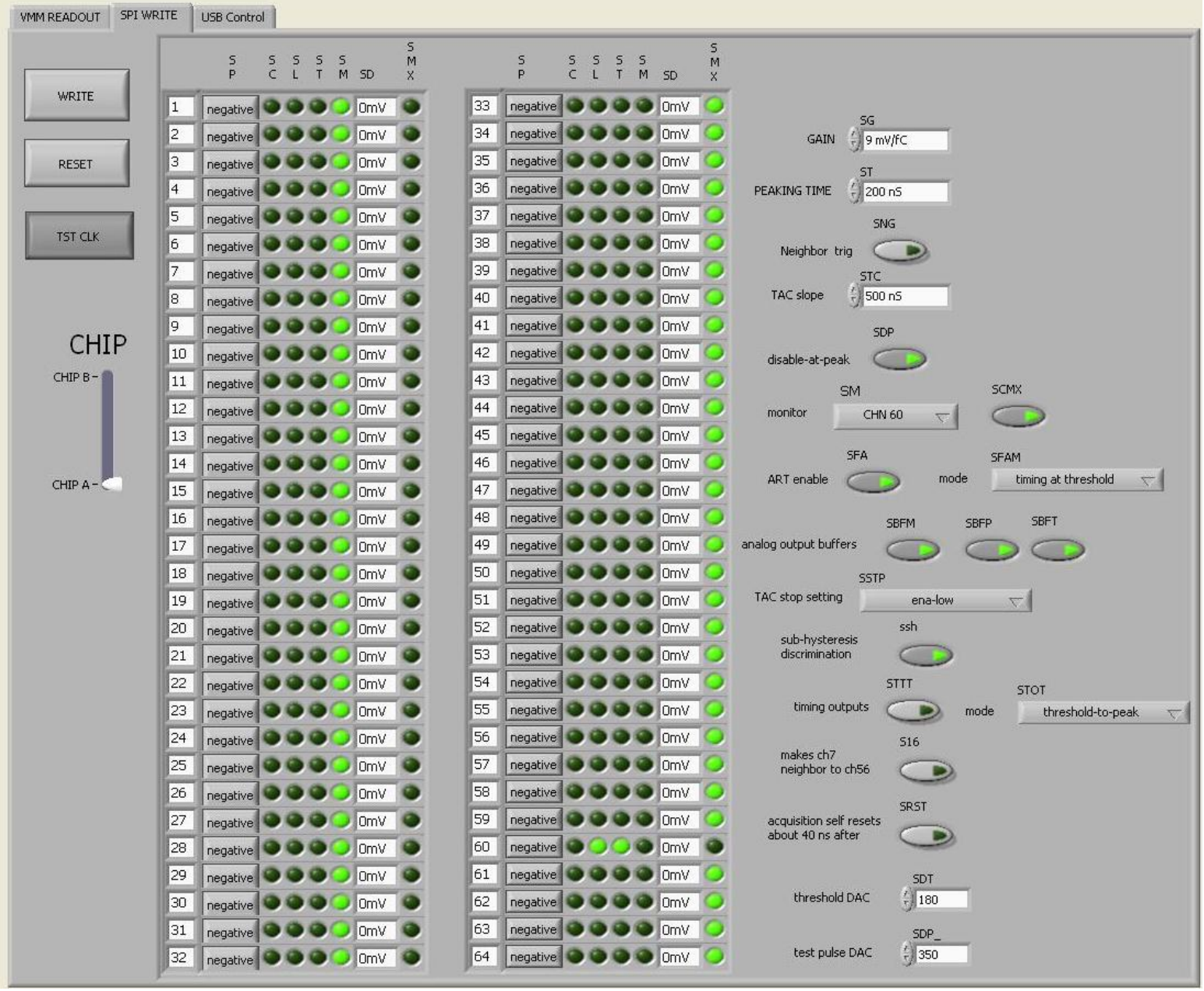
Status as of April 2nd, 2012 - Test Board



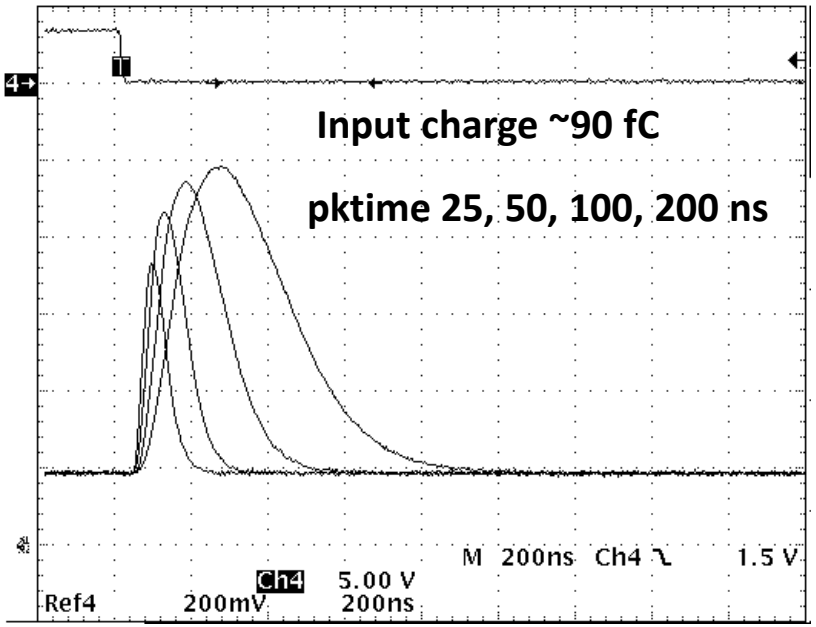
Status as of April 2nd, 2012 - Test System

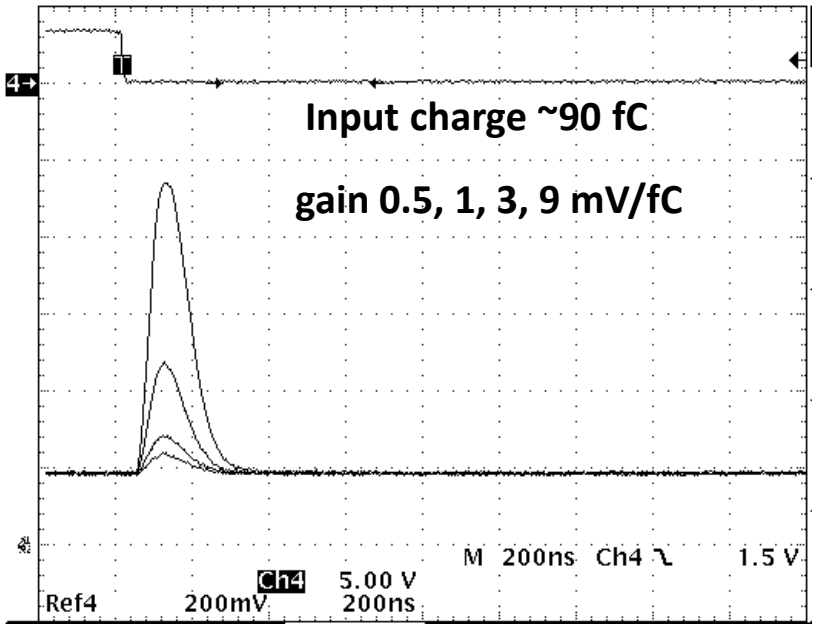


Status as of April 2nd, 2012 - Interface



Preliminary results as of April 2nd, 2012 - Pulse Response

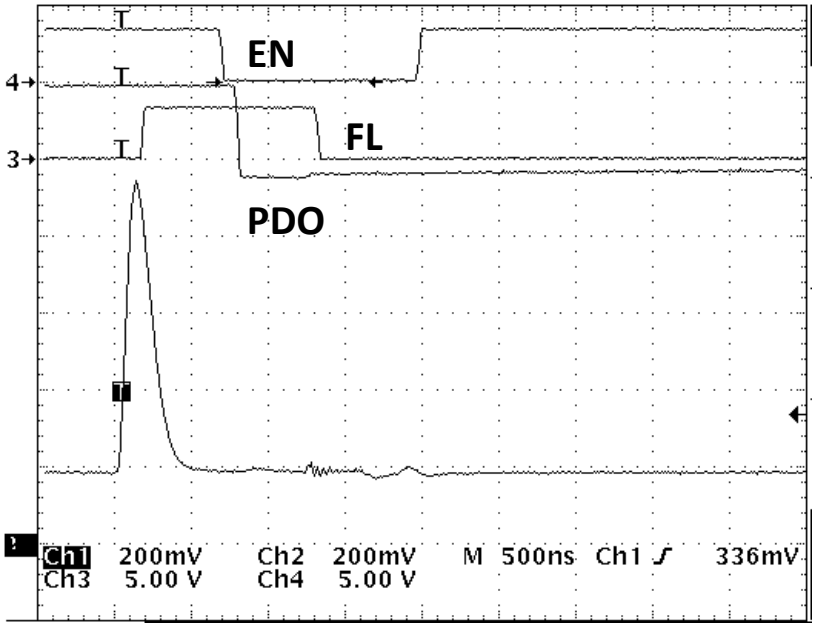


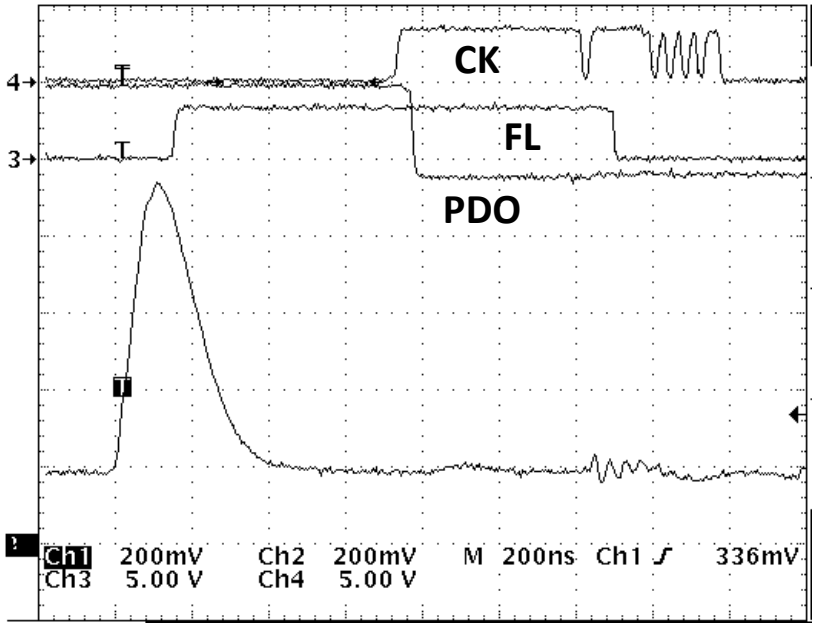


Measured output noise at 9mV/fC

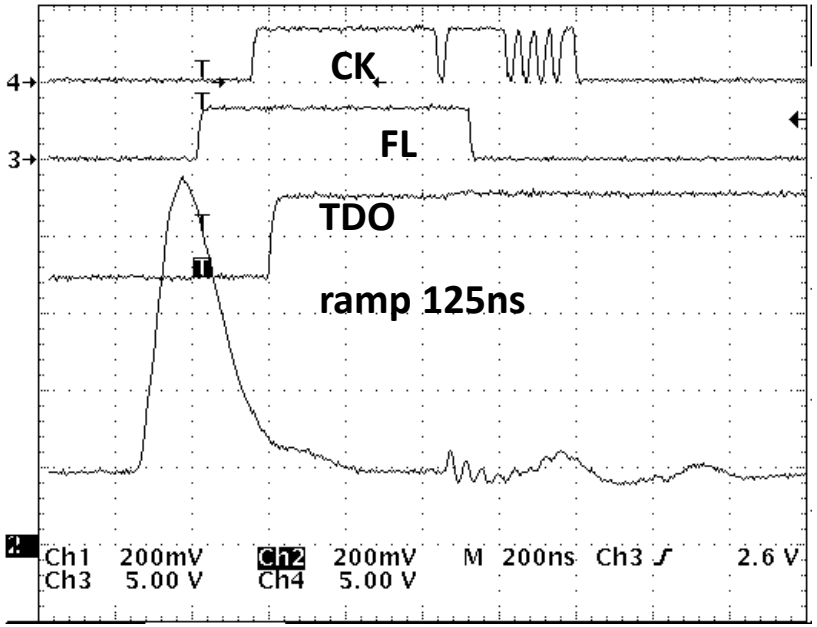
peaktime	outnoise	enc
25, 50, 100, 200 ns	0.49, 0.81, 1.16, 1.52 mV	340, 560, 800, 1050

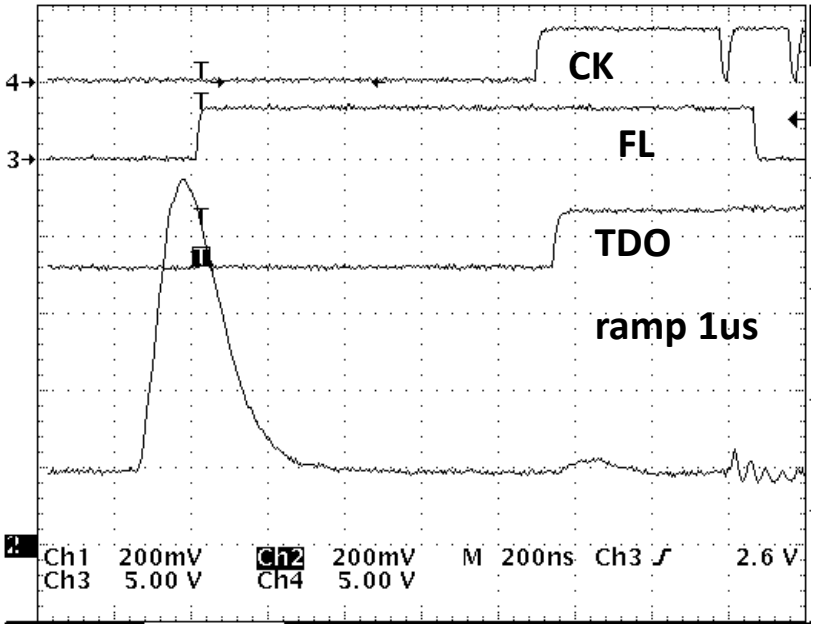
Preliminary results as of April 2nd, 2012 - Peak Detection



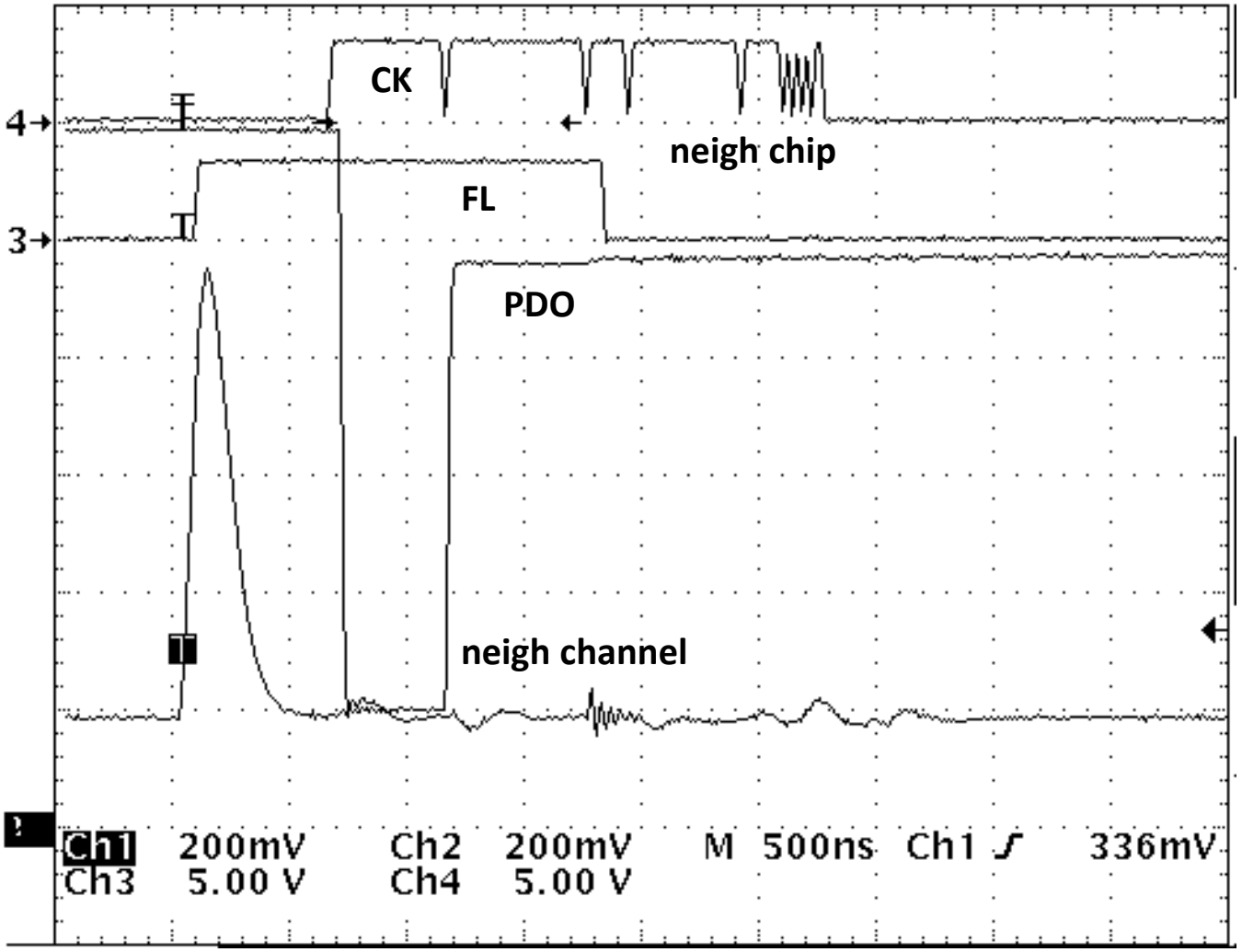


Preliminary results as of April 2nd, 2012 - Timing Detection

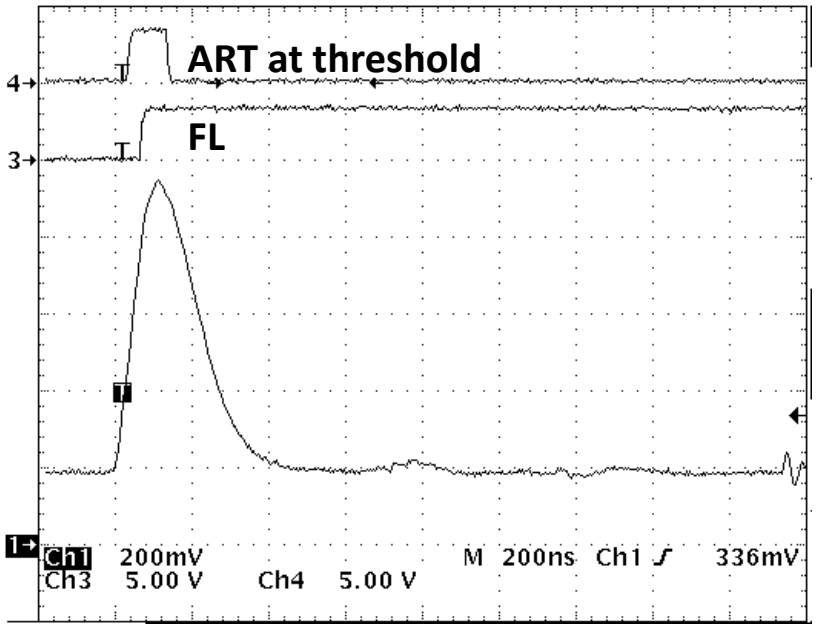


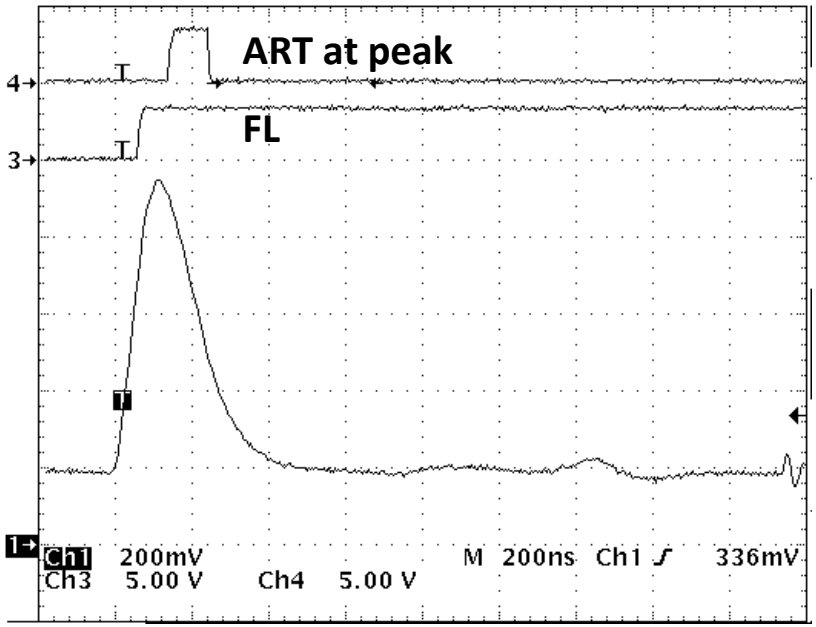


Preliminary results as of April 2nd, 2012 - Neighboring

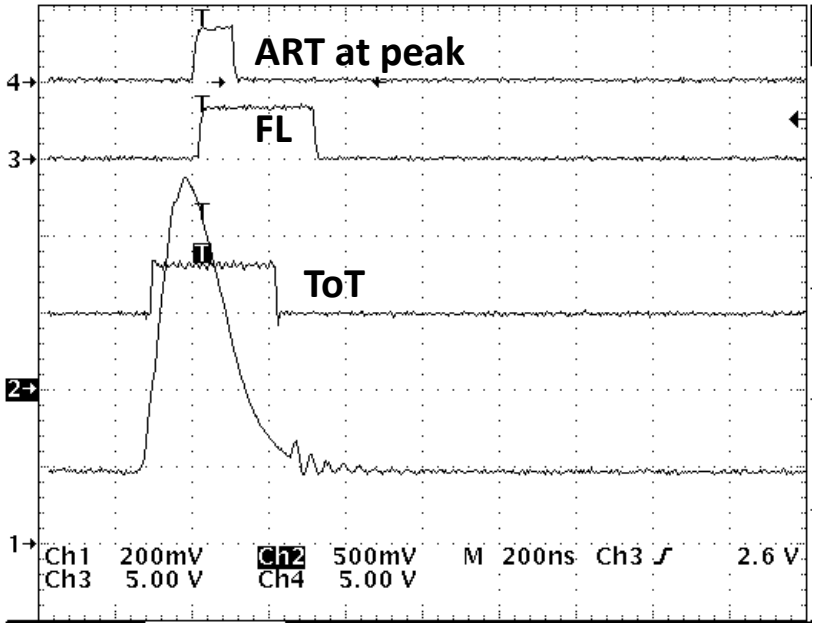


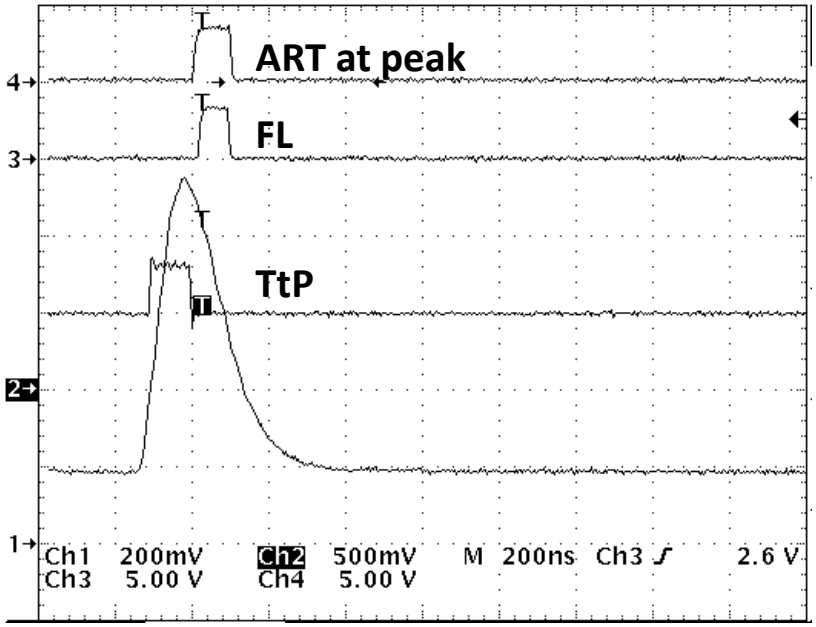
Preliminary results as of April 2nd, 2012 - Fast Flag



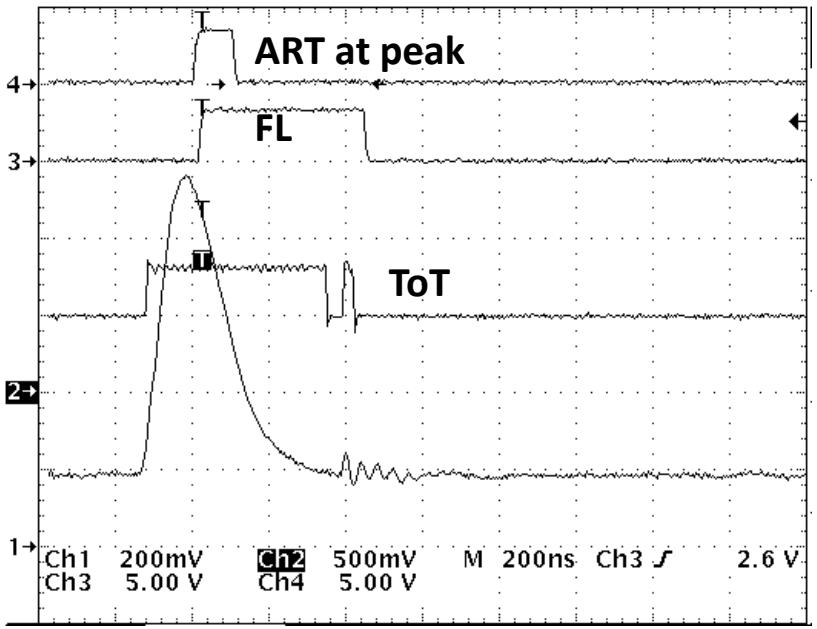


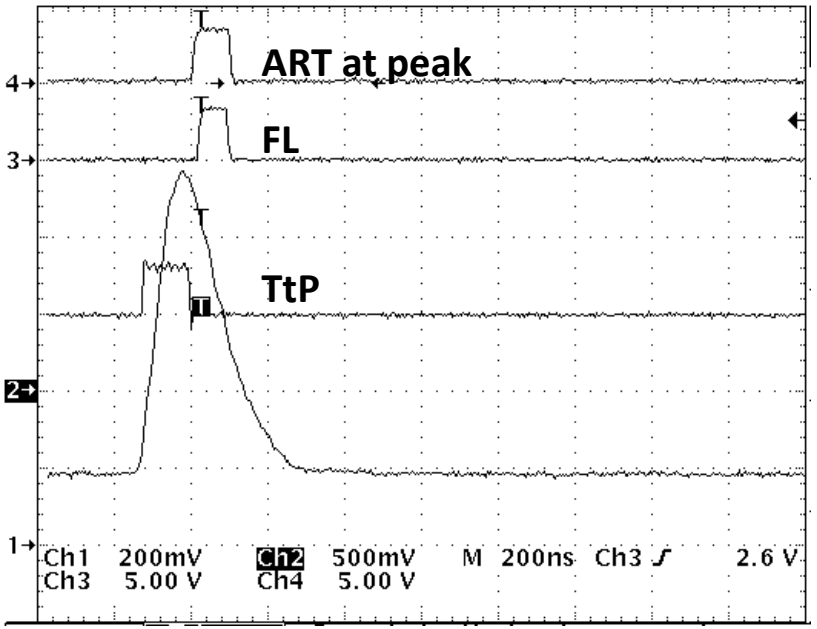
Preliminary results as of April 2nd, 2012 - Timing Outputs 1/2





Preliminary results as of April 2nd, 2012 - Timing Outputs 2/2





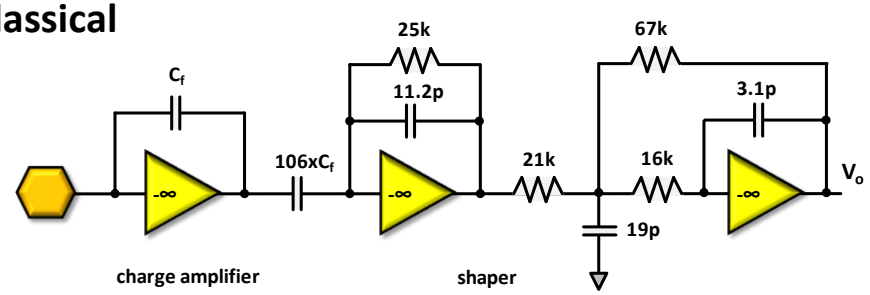
Preliminary results as of April 2nd, 2012 - Summary

- **Most relevant issues so far:**
  - **large leakage from input protection increases noise (~400e^-) and disables positive charge front-end circuit (needs external current compensation, e.g. resistor)**
  - **self-reset function does not reset discriminator**
  - **analog pulse shows some digital pick-up**
  - **mixed signal issues to be investigated**

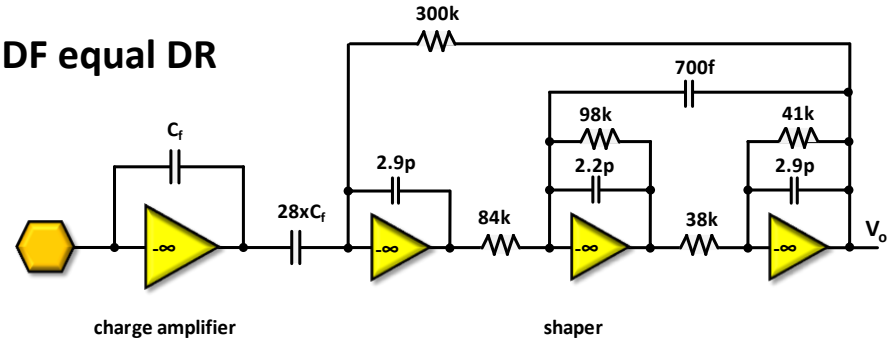
Backup slides

Delayed dissipative feedback (DDF)

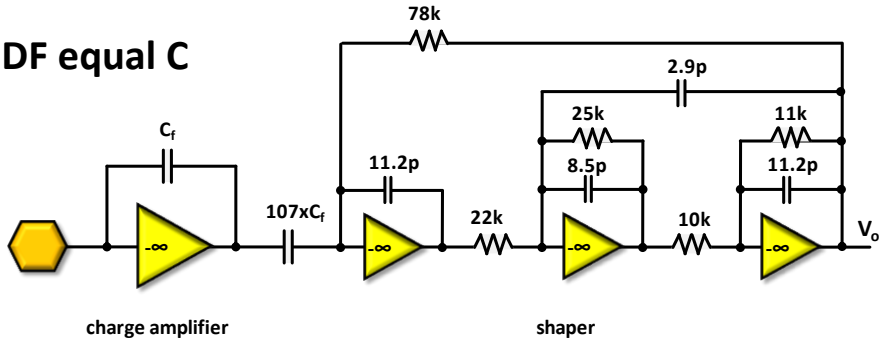
Classical

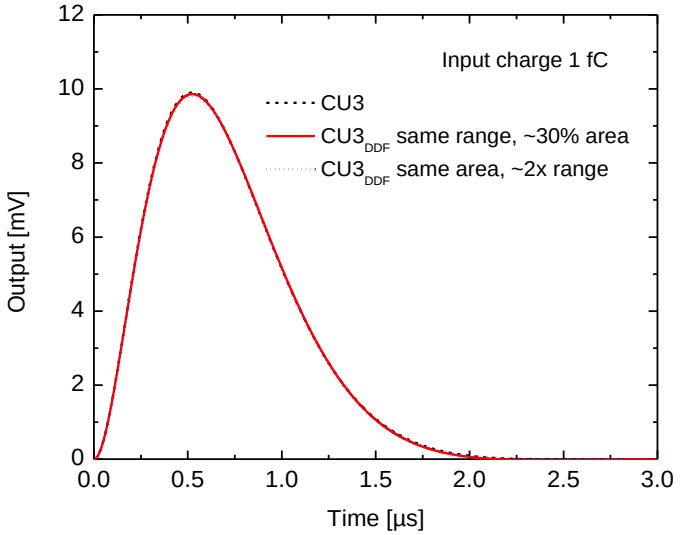


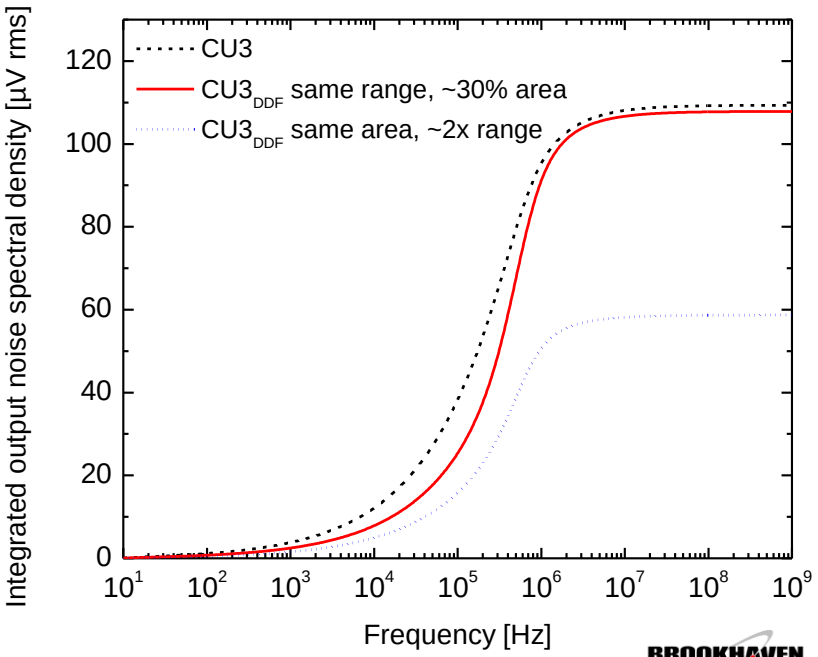
DDF equal DR



DDF equal C

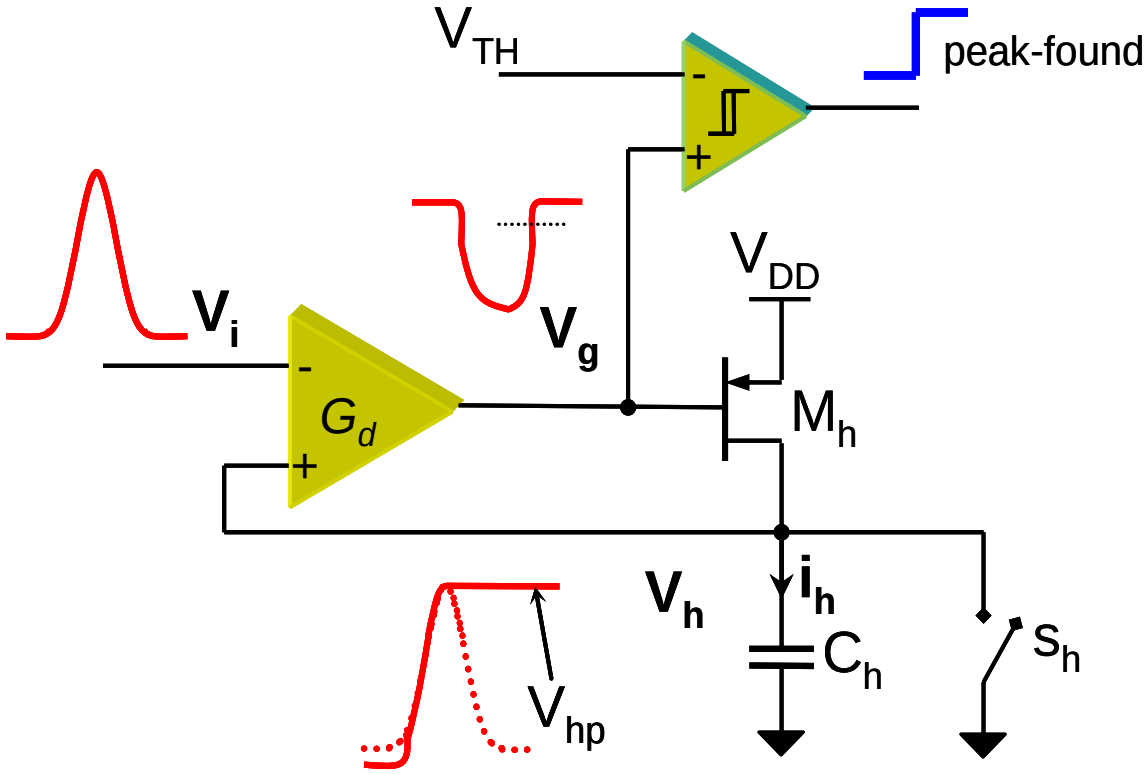






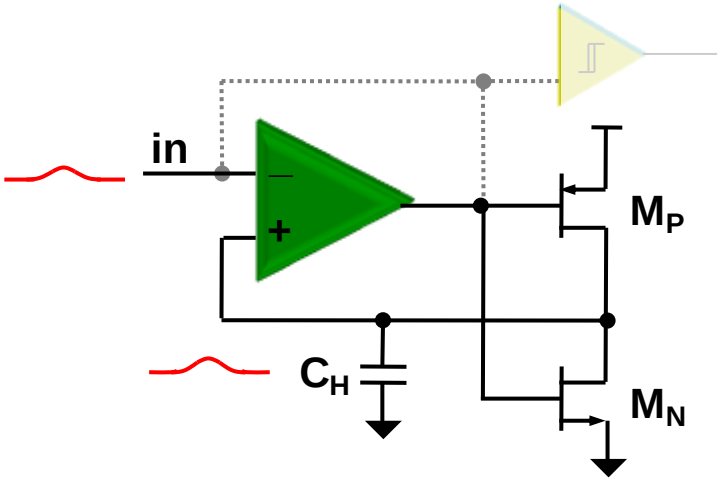
G. De Geronimo et al., IEEE TNS 58 (2011)

Peak detector - classical configuration



- detects and holds peak without external trigger
- provides accurate timing signal (peak found, z-cross on derivative)
- low accuracy (op-amp offset, CMRR)
- poor drive capability

Peak detector - multiphase

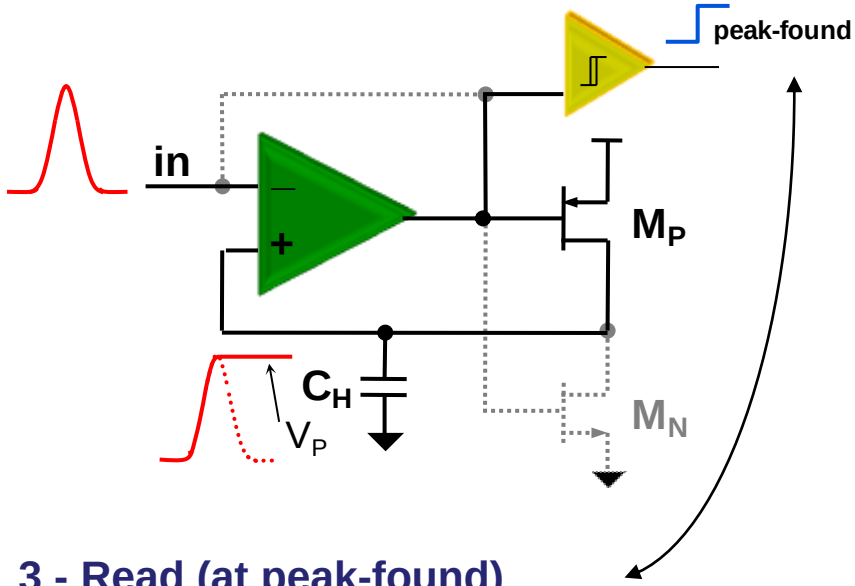


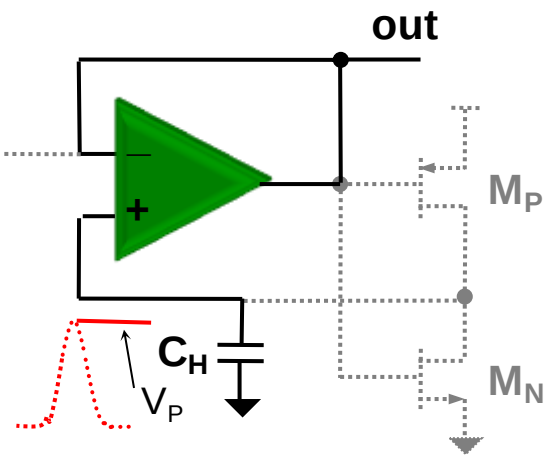
1 - Track (< threshold)

- Analog output is tracked at hold capacitor
- M_P and M_N are both enabled

2 - Peak-detect (> threshold)

- Pulse is tracked and peak is held
- Only M_P is enabled
- Comparator is used as peak-found



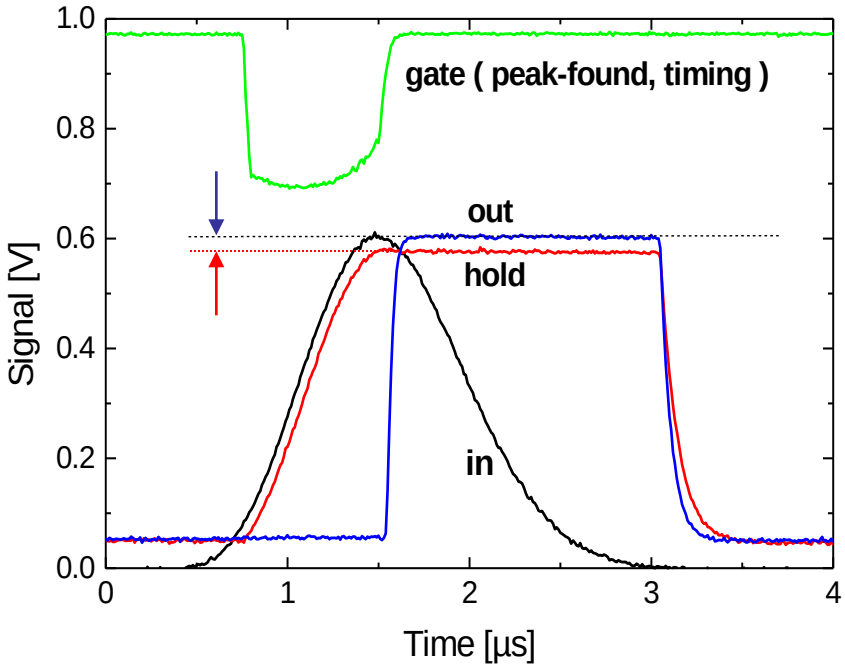


3 - Read (at peak-found)

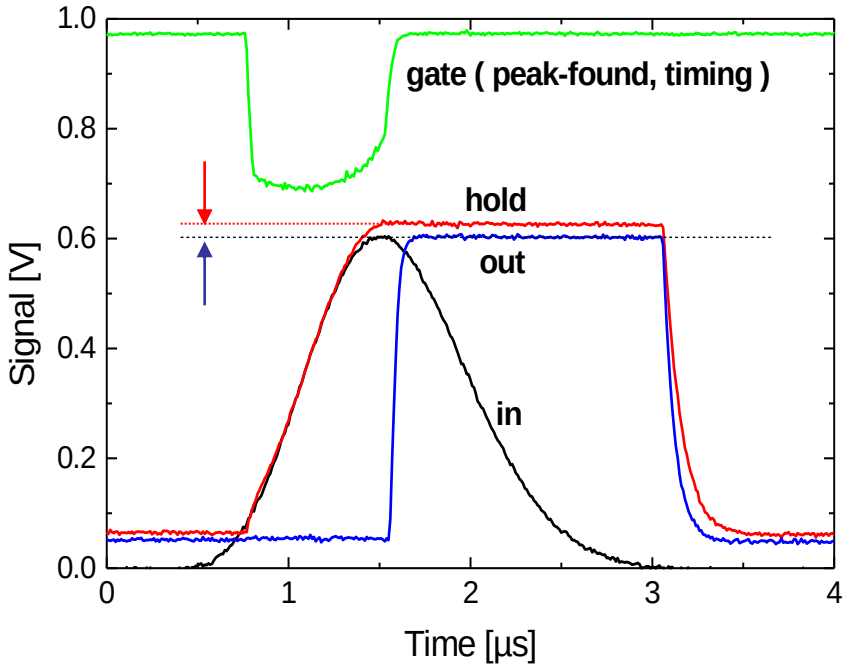
- Amplifier re-configured as buffer
- High drive capability
- Amplifier offsets is canceled
- Enables rail-to-rail operation
- Accurate timing
- Some pile-up rejection

Peak detector - multiphase

Chip 1 – negative offset



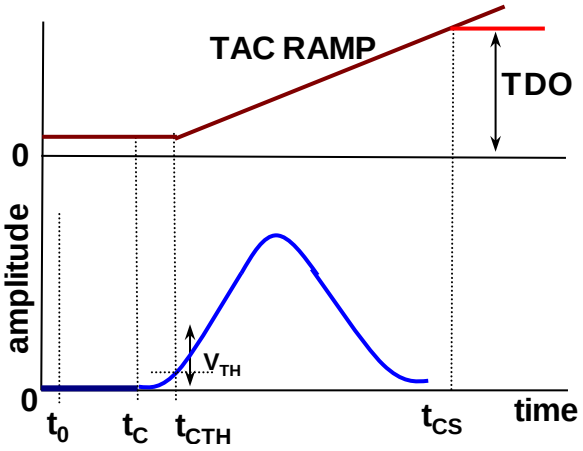
Chip 2 – positive offset



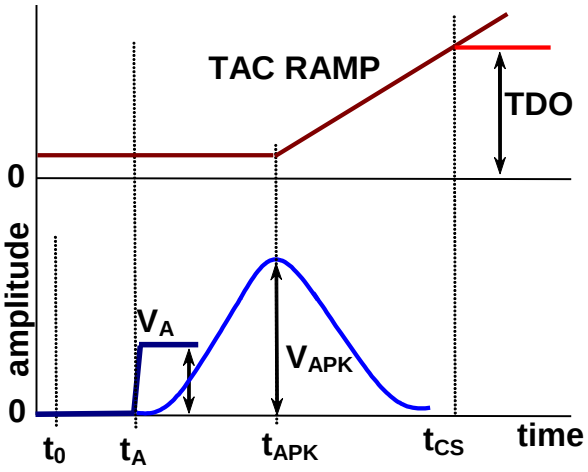
Peak detector - timing function

Compare **timing at threshold crossing** with **timing at peak**

Threshold crossing



Peak detection



$$\sigma_t \approx \frac{ENC}{Q \left.\frac{ds}{dt}\right|_{@\,threshold}}$$

output slope normalized to unit charge

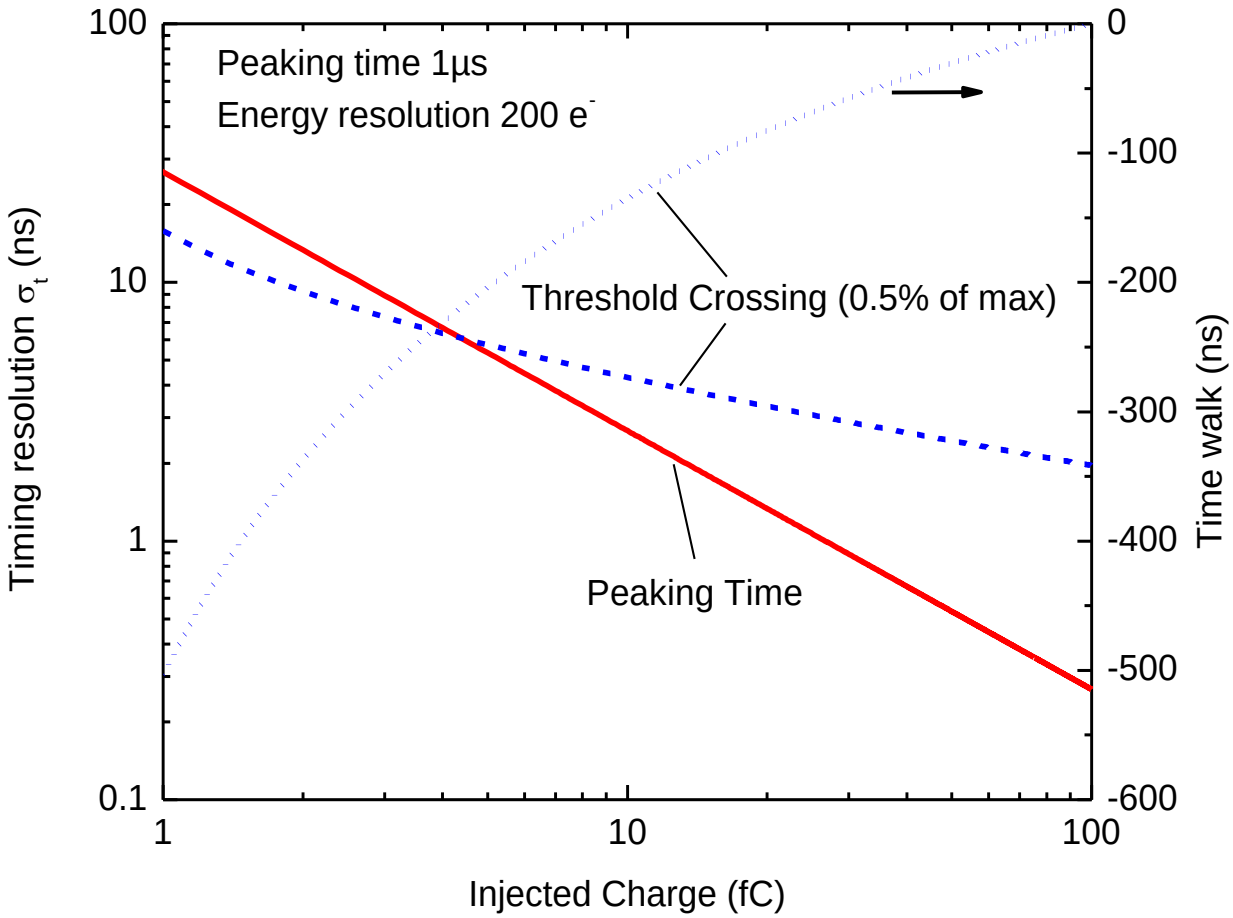
$$\sigma_t \approx \frac{ENC \cdot \tau_p \lambda_p}{Q\ \rho_p}$$

Time-walk strongly dependent on amplitude

Time-walk almost independent of amplitude (equivalent to zero crossing on differential)

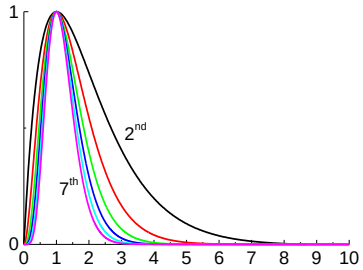
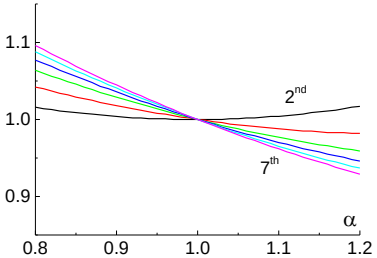
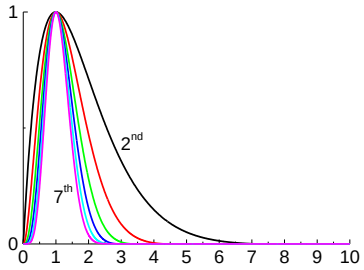
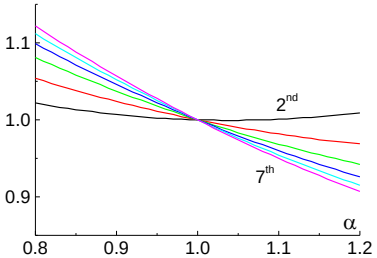
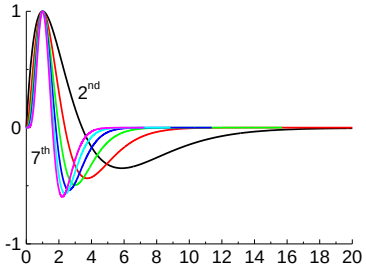
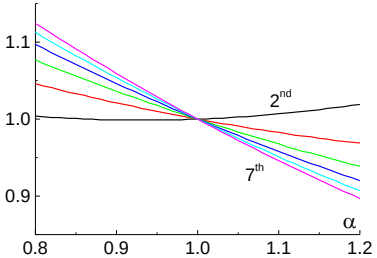
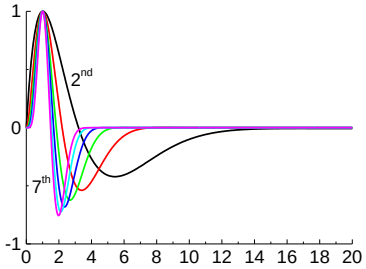
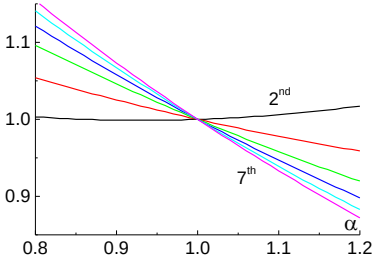
Peak detector - timing function

Compare **timing at threshold crossing** with **timing at peak**



$$\sigma_t \approx \frac{ENC \cdot \tau_p \lambda_p}{Q\ \rho_p}$$

Shaper coefficients for amplitude and timing resolution

Filter	Shape	a_w	$a_f(1)$	a_p	$\rho_f(\alpha_f)=a_f(\alpha_f)/a_f(1)$	τ_w/τ_p	$-\rho_p$	η_p	λ_p
RU-2		0.92	0.59	0.92		7.49	0.98	-	-
RU-3		0.82	0.54	0.66		5.04	1.85	0.30	1.64
RU-4		0.85	0.53	0.57		4.17	2.50	0.44	1.60
RU-5		0.89	0.52	0.52		3.72	3.01	0.52	1.60
RU-6		0.92	0.52	0.48		3.46	3.40	0.57	1.61
RU-7		0.94	0.51	0.46		3.28	3.74	0.61	1.62
CU-2		0.93	0.59	0.88		6.17	1.05	-	-
CU-3		0.85	0.54	0.61		3.92	2.07	0.31	1.59
CU-4		0.91	0.53	0.51		3.16	2.95	0.48	1.57
CU-5		0.96	0.52	0.46		2.84	3.65	0.58	1.58
CU-6		1.01	0.52	0.42		2.66	4.22	0.63	1.60
CU-7		1.04	0.52	0.40		2.55	4.71	0.65	1.62
RB-2		1.03	0.75	1.01		16.6	0.34	0.29	-
RB-3		1.11	0.78	0.76		9.87	0.69	0.41	-
RB-4		1.30	0.81	0.66		7.67	0.98	0.47	-
RB-5		1.47	0.85	0.62		6.61	1.20	0.51	-
RB-6		1.61	0.87	0.59		5.96	1.39	0.54	-
RB-7		1.74	0.90	0.57		5.53	1.55	0.56	-
CB-2		1.08	0.80	1.02		12.9	0.47	0.33	-
CB-3		1.27	0.86	0.76		7.29	0.91	0.45	-
CB-4		1.58	0.93	0.67		5.58	1.32	0.52	-
CB-5		1.87	0.98	0.62		4.80	1.66	0.56	-
CB-6		2.10	1.03	0.60		4.39	1.92	0.58	-
CB-7		2.33	1.06	0.57		4.10	2.15	0.61	-