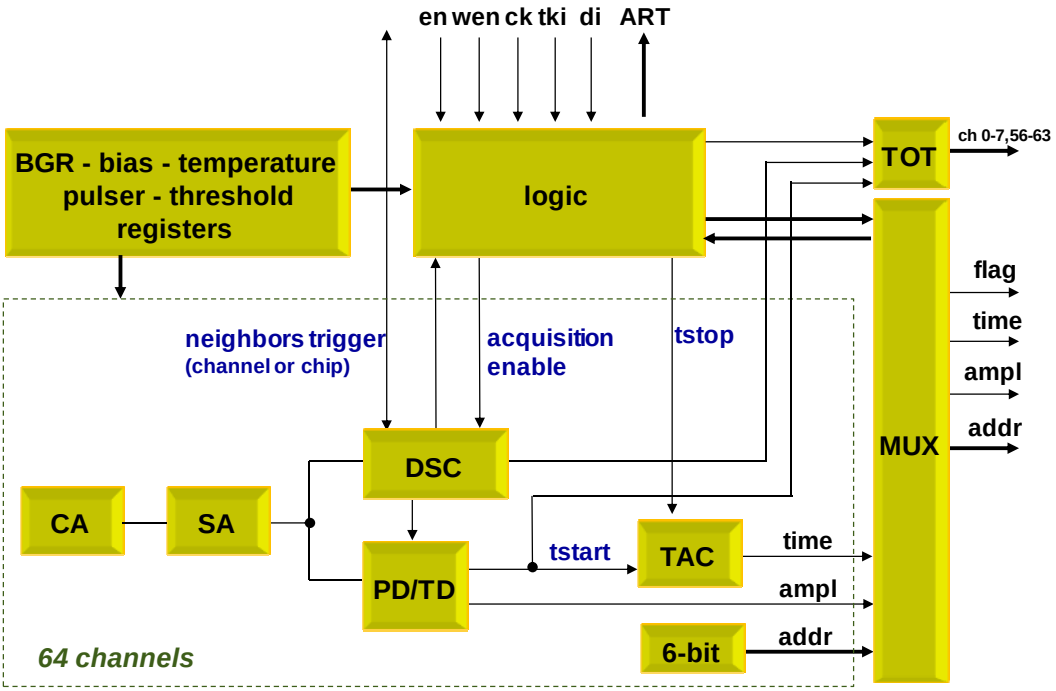
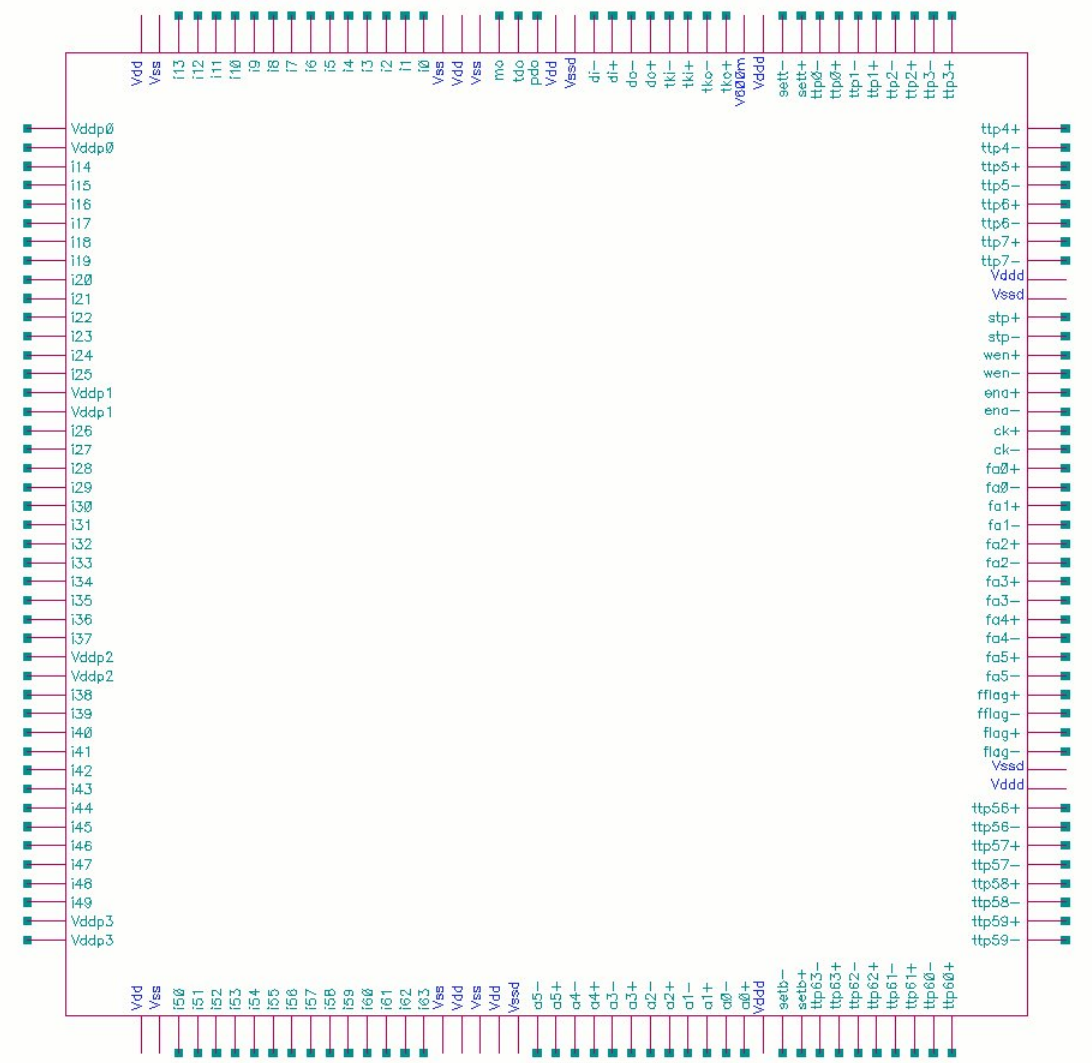
VMM1


en wen ck tki di ART
BGR - bias - temperature pulser - threshold registers
logic
TOT
ch 0-7,56-63
flag
time
ampl
addr
MUX
neighbors trigger
(channel or chip)
acquisition enable
tstop
DSC
CA
SA
PD/TD
tstart
TAC
time
ampl
6-bit
addr
64 channels


Vddp0
Vddp0
i14
i15
i16
i17
i18
i19
i20
i21
i22
i23
i24
i25
Vddp1
Vddp1
i26
i27
i28
i29
i30
i31
i32
i33
i34
i35
i36
i37
Vddp2
Vddp2
i38
i39
i40
i41
i42
i43
i44
i45
i46
i47
i48
i49
Vddp3
Vddp3
ttp4+
ttp4−
ttp5+
ttp5−
ttp6+
ttp6−
ttp7+
ttp7−
Vddd
Vssd
stp+
stp−
wen+
wen−
ena+
ena−
ck+
ck−
fa0+
fa0−
fa1+
fa1−
fa2+
fa2−
fa3+
fa3−
fa4+
fa4−
fa5+
fa5−
fflag+
fflag−
flag+
flag−
Vssd
Vddd
ttp56+
ttp56−
ttp57+
ttp57−
ttp58+
ttp58−
ttp59+
ttp59−

- **Technology**
  - IBM 130nm, 1.2V, packaging: QFN 176

- **Modes of operation**
  - acquisition: events are detected and processed (amplitude and timing)
    - charge amplification, discrimination, peak- and time-detection
    - address in real time (ART) of the first event
    - timing (over-threshold or to peak) per channel available for channels 0-7 and 56-63
  - readout: events are read out in sparse mode with token passing (amplitude, timing, address)
  - configuration: global and channel registers

- **Main functionalities and settings**
  - global
    - temperature monitor
    - pulse generator (10-bit adjustable amplitude)
    - coarse threshold (10-bit adjustable)
    - self-reset option
    - analog monitor at *mo*
      - analog outputs, trimmed thresholds, (Band-Gap Reference) BGR, threshold, pulser amplitude , temperature sensor
    - high-drive analog buffers on *mo*, *pdo*, *tdo*
    - smart resets
  - analog section
    - charge amplification and high-order shaping
    - adjustable polarity (negative, positive)
    - gain: 0.5, 1, 3, 9 mV/fC (2, 1, 0.33, 0.11 pC)
    - peaktime: 25, 50, 100, 200 ns
    - test capacitor, channel mask
  - discriminator
    - trimmer (4-bit adjustable, 1mV)
    - sub-hysteresis processing
    - neighbor logic on channels and chips (ch0, ch63)
  - peak detector
    - multi-phase
  - time detector
    - TAC ramp (selectable 100ns or 200ns)
    - starts at peak-found
    - stop selectable (*ena*-low or *stp*-low)
  - ART
    - address of the first event in real time
    - selectable at first threshold or at first peak
    - self-resets in 40ns
    - *fflag* indicates event
    - address available at *fa0-fa5*
  - timing per channel
    - available for channels 0-7 and 56-63
    - selectable between time-over-threshold and time-to-peak
  - readout

        - *flag* at first peak indicates events to readout
        - sparse with token passing
        - amplitude available at *pdo*
        - timing available at *tdo*
        - address available at *a0-a5*
    - interfaces
        - analog IOs ESD protected
        - digital IOs LVDS 600mV +/- 150mV
    - analog monitors
        - analog outputs, trimmed thresholds, BGR, threshold, pulser, temperature sensor

- **Pinout**
    - 176 pins (44 each side)
    - *Vdd,Vss*: analog supplies 1.2V and grounds 0V
    - *Vddd, Vssd*: digital supplies 1.2V and grounds 0V
    - *Vddp0-Vddp3*: charge amplifier supplies 1.2V
    - *V600m*: reference for LVDS 600mV
    - *i0-i63*: analog inputs, ESD protected
    - *mo*: monitor multiplexed analog output
    - *pdo*: peak detector multiplexed analog output
    - *tdo*: time detector multiplexed analog output
    - *flag*: event indicator
    - *a0-a5*: multiplexed address output, tristated (driven with token)
    - *ttp0-ttp7* and *ttp56-ttp63*: time-over-threshold or time-to-peak digital outputs
    - *fflag*: ART event indicator
    - *fa0-fa5*: ART address output
    - *sett*: ch0 neighbor trigger
    - *setb*: ch63 neighbor trigger
    - *ena*: acquisition enable
        - *ena* high, *wen* low: acquisition mode
            - internally enabled after 40ns from *ena* high
        - *ena* low, *wen* low: readout mode
        - *ena* pulse, *wen* high: global reset
    - *wen*: configuration enable
        - *wen* high: configuration mode
        - *wen* pulse: acquisition reset
    - *ck*: clock
        - in acquisition mode *ck* is timing counter clock (not used in this version)
        - in readout mode *ck* is readout clock
        - in configuration mode *ck* is readout clock
    - *stp*: timing stop
    - *tki, tko*: token input and output (3/2 clock widen)
    - *di, do*: data configuration input and output (1/2 clock shifted)
        - in acquisition *di* becomes pulser clock

- **Registers**
    - global bits
        - *sg0,sg1*: gain (0.5, 1, 3, 9 mV/fC)(2, 1, 0.33, 0.11 pC)
        - *st0,st1*: peaktime (25, 50, 100, 200 ns)
        - *sng*: neighbor (channel and chip) triggering enable
        - *stc*: TAC slope adjustment

- *sdp*: disable-at-peak
- *scmx, sm0-sm5*: monitor multiplexing
- *sfa, sfam*: ART enable and mode (peak, threshold)
- *sbfm,sbfp,sbft*: buffers enable (*mo*, *pdo*, *tdo*)
- *sstp*: TAC stop setting (*ena*-low or *stp*-low)
- *ssh*: sub-hysteresis discrimination enable
- *sttt,stot*: timing outputs enable and mode (tot or ttp)
- *s16*: makes ch7 neighbor to ch56
- *srst*: self reset (40ns after *flag*)
- *sdt0-sdt9*: coarse threshold dac
- *sdp0-sdp9*: test pulse dac

o channel bits

- *sp*: polarity
- *sc*: large input capacitance mode (Cin>30pF)
- *sl*: leakage generator enable
- *st*: test capacitor enable
- *sm*: mask enable
- *sd0-sd3*: trim threshold dac
- *smx*: mux monitor mode (analog or trim threshold)