## The Electronics Challenge

- The Small ( $\sim$ 0.5 mm FWHM) charge footprint of the  $\mu$ Megas Detectors results in excellent position and double track resolution
- Results in a very large number of channels (order 10<sup>6</sup>)
- Two Functions of the Readout:
  - o Provide Precision measurement of charge and time at Trigger Level 1 accept
  - Provide in real time vector with ~1 mrad resolution to assist Trigger Level 1
- First task relatively easy to accomplish by highly multiplexed, data driven system
- Custom front end ASIC being under development

## BUT, How about Trigger? Need to process in Parallel at 40 MHz

## How can we take advantage of the 0.5 mm strip pitch?

Assume that we use ONLY one hit (the strip with the first arriving signal above a set threshold) from each 64-channel chip at each bunch crossing

### This way:

- ☐ We have a trigger system with granularity of 3.2 cm (64 channels x 0.5 mm) BUT
- ■With spatial resolution ~ 0.5 mm
- ■We now have to deal with ~30,000 channels and not 2 million

# But are we paying a price for this? i.e. efficiency loss?

Consider worst case at  $\eta$ = 2.4: Rate r = 10 kHz/cm<sup>2</sup>, strip length l = 50 cm, strip width w = 0.5 mm

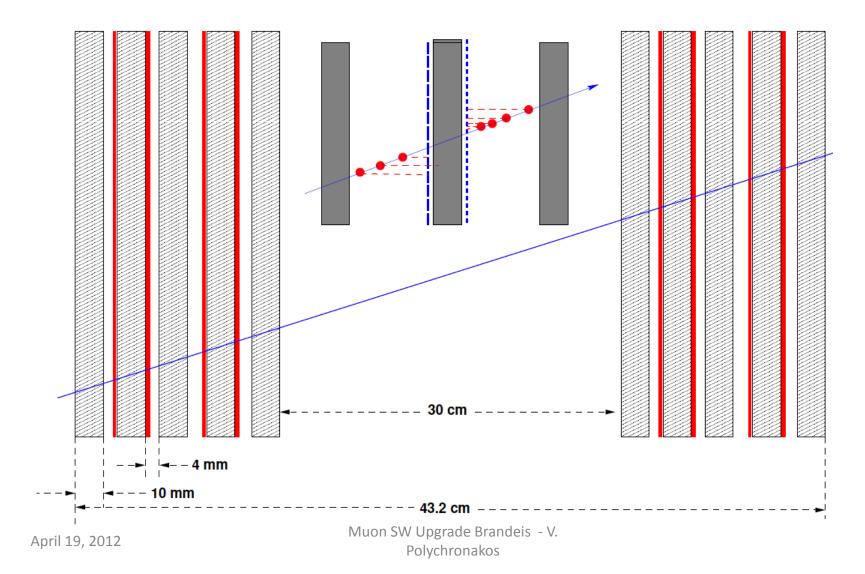
Occupancy/BC = rlwt =  $6.25 \times 10^{-4}$ 

	Probability per Front End IC [%]	
	Probability per Chip	Probability per Chip
# Hits	per Bunch Crossing	per 3 Bunch Crossings
0	96.1	88.7
1	3.8	10.6
>=2	0.1	0.6

Note: ONLY 12% of hits are from track segments (Results from CSC data at present Lumi.)

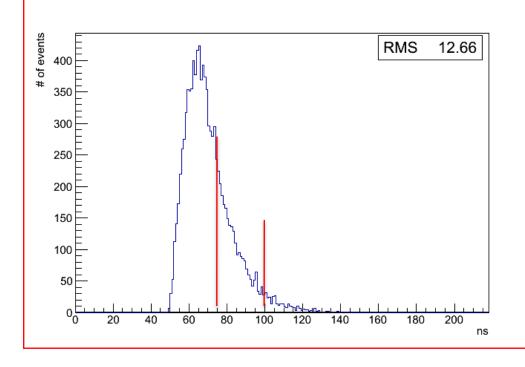
## Simulation with George Iakovididis And Theo. Alexopoulos

### Chamber arrangement used in the simulation

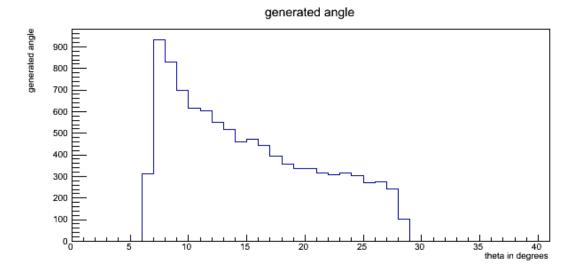


Earliest Arrival time Incident Angle = 20° Integration Time 50 ns

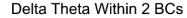
Earliest Peak above threshold of 1e

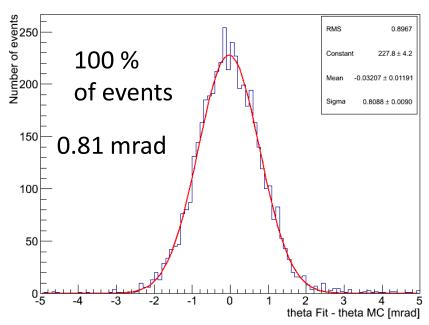


Small Wheel Angle Generation

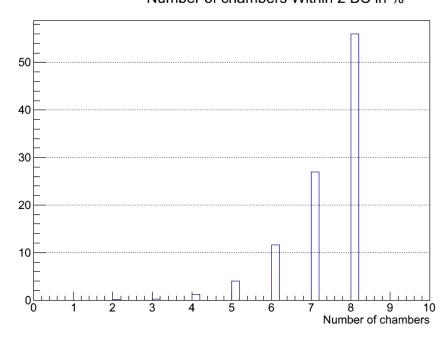


#### Rolling Window of 2 Bunch Crossings





Number of chambers Within 2 BC in %

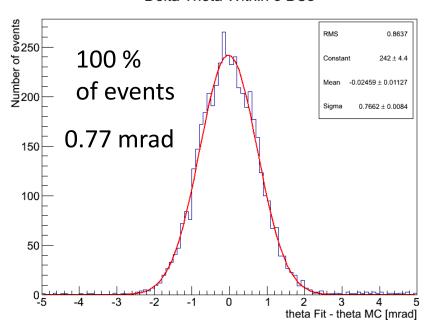


Track Segment Resolution with hits in a Rolling Window of 2 bunch crossings

Probability of n chambers in a Rolling Window of 2 bunch cossing

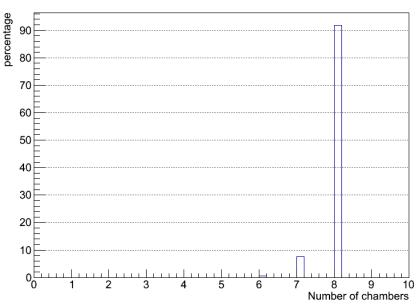
#### Rolling Window of 3 Bunch Crossings

Delta Theta Within 3 BCs



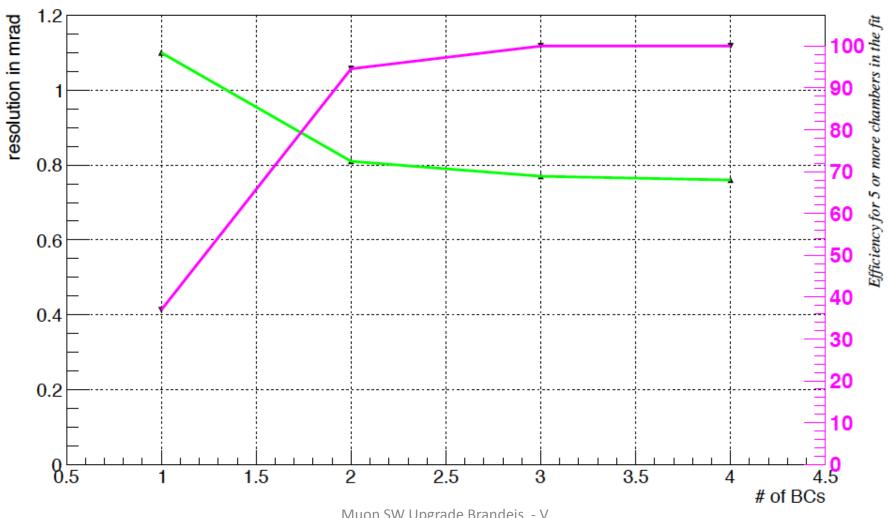
Track Segment Resolution with hits in a Rolling Window of 3 bunch crossings



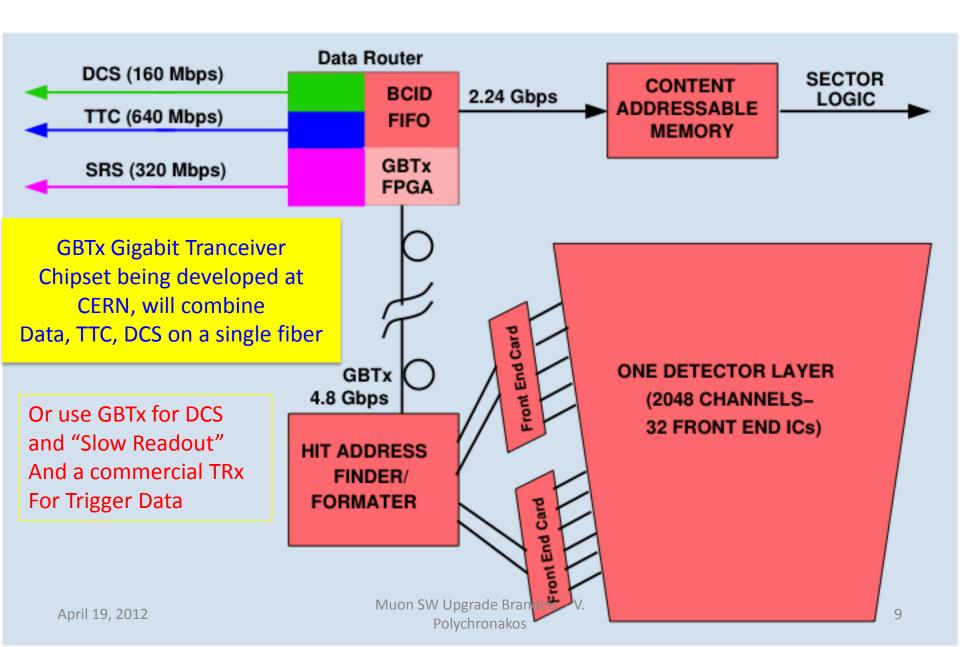


Probability of n chambers in a Rolling Window of 3 bunch crossings

### efficiency & resolution Versus BCs



## Trigger/DAQ Block Diagram



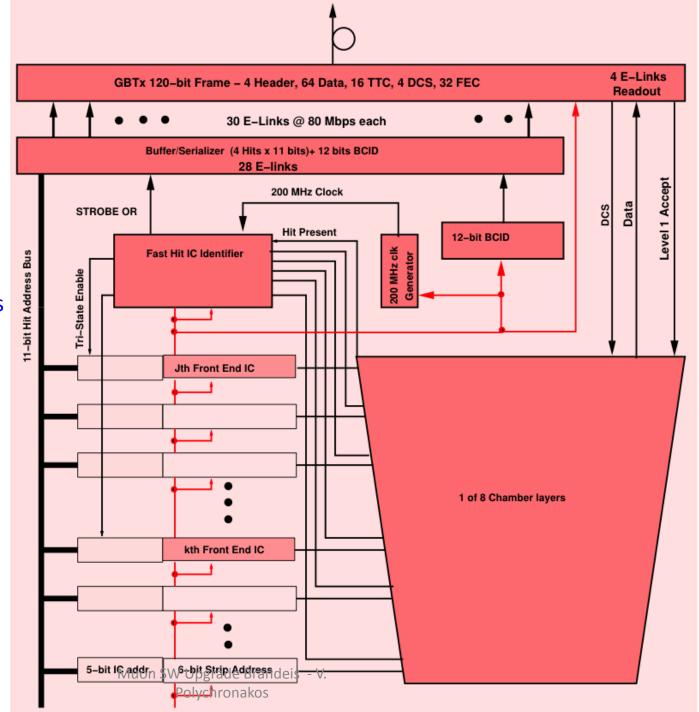
#### **On-Detector Card**

6 bit prompt strip address

5 bit IC address per plane

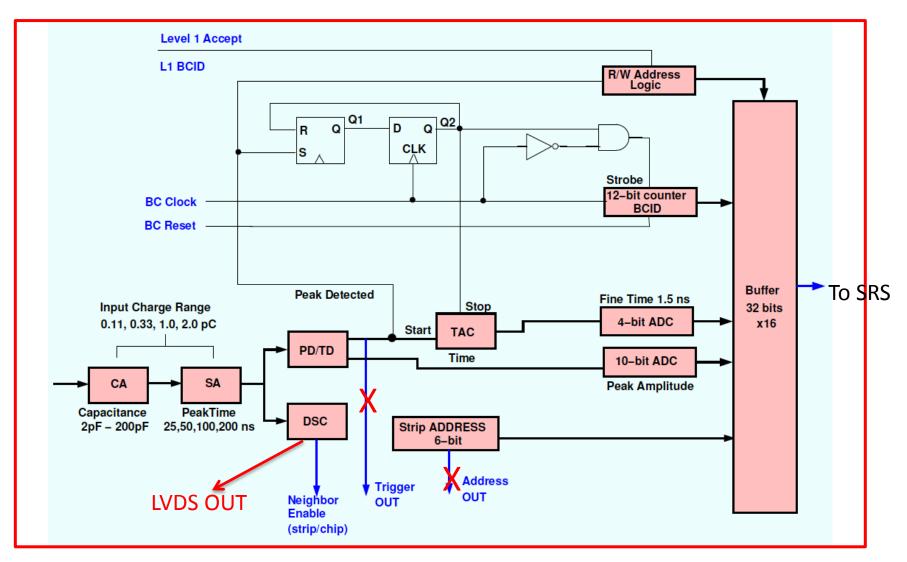
Up to 4 hits per plane transferred in 2 BC

Possibility to incorporate this function in Front End or a Custom Digital IC



## How does the a Mmegas System complements the Primary sTGC System

## **New Common Front End ASIC**





## Balance conflicting requirements

Micromegas

#### Very rare access, congested location, 1Mrad at innermost radius

- Minimum on-chamber complexity for reliability
  - But minimum cables to periphery
- Minimum on-chamber power dissipation
- Minimum on-chamber radiation tolerant electronics
- No Cables to Periphery
  - Just the front ends and fiber Drivers
  - But want programmable logic to future-proof the design Nothing Programmable

    No need for access
- Maximum access to electronics for repair

### Advantages of this solution

- Simple, no-extreme technology for links or logic
- Trigger generation is simple so its simulation is straight forward and therefore easy to verify.

#### sTGC trigger: strip logic: one layer of one 1/16th

ASD

ASD

ASDs

36

L. L&Piris 19, 201 March 2012

32

ToTD

on-chamber

TOT2Ds

18

Inner

Total:

strips

~1050

A band may bridge two ToTDs. Gaps in ASD allowed due to chamber boundaries TTC and DCS via Pad GBT BCID is pushed On-chamber cables: band[6:0] φ[3:0] with the data Pad trigger All signals are LVDS pairs: avg/max length 2.5m/5m ToTD to router: 18 twinax pairs TTC & Config Distrib bus sTGC Band select & o to ToTD bus: 3 x 10 twisted pairs on rim of small wheel twinax LVDS pair ASD length < 5m Selected band: suppress strips < ToTmin: 8 of up to 32 strips; ToTD Largest ToT is kept. 32 ASD One 125-bit word per BC  $\Rightarrow$  5.0.Gb/sec on-chamber hit 0 hit7 strip# ToT strip# ToT rsrvd # bits 12 BC clock ASD Outer Outer ToTD 32 ASD centroid finder 6.25 Gbit/s opt router on-chamber! and track lnk 8 layers extrapolator 3.6m on rim of small wheel flexible boundary to in USA15 →sector logic Middle 3 candidates per BC 6.25 Gbit/s centroid finder opt Middle router ≤8 and track electrical link Ink up to 8 layers extrapolator 80bits × 40MHz on rim of small wheel flexible boundary in USA15 2nd copy to Inner

6.25 Gbit/s

routers links
3
Muon SW Upgrade Brandeis - V.
sTGC Trigger Electropics

on rim of small wheel

Micromegas Strip addresses of 0.5 mm strips

router

≤8

opt

Ink

sTGC\_trigger\_stripLogic\_V04

~65 overlapping bands of strips per layer

Typically 20, but up to 32, strips in a band

centroid finder

and track

extrapolator

centroid finders

3 (for 8 layers)

in USA15

8 layers

**1**44

adjacent SL

## Summary

- Synchronous Trigger Data from Front End available in USA15 without any further on-detector processing
- No need for access during run
- Minimum Power, Services
- Common Front End (Only Trigger information different)
- Choice of how to use the trigger information
  - Provide redundant segment to Sector Logic
  - Combine information before segment → Segment from 16 planes
  - Possible to use Pad Logic to selectively read strips for full compatibility with sTGC