MMFE Related Questions

1. MMFE-8 Layout:

Q: When do you plan on going to layout for this board?

A: Any day. We are currently assembling documentation to solicit bids… It is anticipated there will be changes during layout, and there will need to be good communications with the designer…

Q: Can we schedule a review at the schematic stage? Doing so for all the on chamber boards can save a lot of time and expense in re-spins of these boards…

A: Yes, absolutely needs review, both after schematics and after layout. Just on little gotcha's that are invisible to the designer it can save a board spin…

2. miniSAS cables:

Q: Should we AC couple the E-Links Carrying L1 Data, Config, and TTC ?

A: No. This would cause many problems including protocol changes to HDLC or 8b10b, extra components, possible noise in the cable shields. The preferred solution is DC coupling, the twinax shield should be grounded at the detector end, with the NSW rim end (L1DDC), grounded via a capacitor [to prevent ground currents in the cable shields].

A: Note that the power arrives floating with the connection to the detector ground being at the Front End Board.

A: Philippe Farthouat also thought that DC coupling was OK.

A: Note that it looks like the drain wires in the connector are connected to the cable's shield and to the "GND" pins of the mini-SAS. Assuming that the cage is connected to the drain via the cable side connector, the cages should also have caps at the L1DDC end. Can someone please confirm these two assumptions, since our cable has been loaned to Rome.

Q: Should the ART cables be AC coupled?

A: This same solution should be used for all cables. All modules will be separately grounded by heavy copper braid to a single point ground. A single point ground must be defined for each independent segment, and for the entire NSW.

A: Note: we didn't get the shield ground modification into the MMFE1 we just built, but we are implementing it in the adapter…

Q: Which end should be open, should it be AC terminated?

A: It was originally surmised that the receive end should be open, but all the cables carry both transmit and receive components. Thus another scheme must be found… It is currently suggested to ground detector side. AC termination has been suggested, but may couple noise?

Q: How many E-Links do we need?

A: This is currently being calculated by Weismann

Q: What are all the capacitors for in the LVDS lines in your diagram below? I thoght we were DC coupling. Even if you did want to AC couple the LVDS lines, I think it has to be done at the receiving end so that the 100 ohm terminator is in a DC path with the LVDS driver. I believe the levels you will see in your circuit below go rail to rail, not LVDS, at least at low frequency.

A: That drawing is obsolete, all the R divides are DNP, and C's are now 0R0. These are inputs so these would have been AC coupled with the caps and DC balanced? This circuit is as suggested By Xilinx, in the event that DCI fails. Also note the R's… could be useful if we have level translation issues…

Q: What is the planned use of the MGT TX and RX? On the L1DDC side can we reserve these two pairs for a second data E-link? As I said, I expect more than one E-link will be needed from sTGC FEBs.

A: With the current configuration, the 26p mini SAS of the L1DDC card has 2 spare pairs on the receiver side. We can use them as a second "elink" (without the clock to the FE). Assuming this, we will be able to run only in 80 and 160Mb/s. This is because now we will connect 4 elinks to each GBTx group. Shall we proceed with this solution?

A: This has already been converted. Is it correct?

Q: Is there a reason that you have split the E-links over the two cables of the mini-SAS?

A: The cable is deigned to have RX on one cable and TX on the other. The connectors are flipped one end to the other. This polarizes the cable so that recive an transmit are always correct. I would like to keep that standard if possible.

Q: What is the planned use of the MGT?

A: The MGT is now gone

Q: Just checking, but are you assured that the "Sideband" pairs you've used for LVDS, are actually twisted pairs in the cable?

A: Yes, the sidebands appear to be more like coax cable or double twinax. I have not been able to get any data on them. They are used for "low speed" (as opposed to 10GbE) signaling such as SPI, so I think it will perform OK in the MHz region in a

configuration similar to the Xilinx sma connectors… The twinax we did measure. I am assured that if these low cost off the shelf cables do not work, we can get custom ones made. We should know if we are OK once the S6 FMC card is running… BTW I have run an S6-LX9 at 1GHz with differential coax and only minor issues due to layout…

3. Analog:

Q: The analog monitors are connected to Bank 15. I can't see where do they go from Bank 15.

Is there an ADC somewhere downstream?

A: Bank 15 contains the ADC. The ADC is built into the FPGA.

Q: I am wondering if you could route to the ADCs the PDO instead of the MO.

In VMM2 the PDO can be set either for the peak-detect output or as monitor-output (i.e identical to MO).

In this way we will also have the option of converting the peaks.

A: We can hook up the PDO instead. Or both or all three if needed (using an analog mux)

A: Hooking PDO and TDO without mux would be best. Second choice would be with a fast mux. Third choice only PDO. In any case there is no need to hook the MO.

A: The ADC is dual [differential] 1MHz 12 bit and uses an internal mux to sample channels. I can add an external mux to external + input, and the FPGA will then have more channels to choose from… I will ground the – input to AGND

4. MMFE-8 Internal Power Distribution:

Q: Why do you use so many inductors especially in the VCCO inputs?

A: #1--- great way to measure current. #2--- great way to break circuit for debug. #3--- With cap gives me an excellent low pass noise filter, way below DCDC ripple frequency, #4--- gives excellent bank to bank isolation –two inductors bank to bank, #5--- The ferrite beads are designed for this application.... Not just inductors...

Q: We have a CERN DCDC converter working with a small flat commercial coil. It could reduce the size. Or maybe we could just use the combo directly on the boards as you have suggested. How many sq. cm do you have devoted to power right now with the 8612 converter etc?

A: Just looking at layout now. Looks like 4x 8612 could fit in feast module

Q: What if we shrink the whole thing by putting the FEAST asic etc. directly on your board?

so the question is: how much room do you have? how many sq. cm. are you using for power now?

A: I'm not sure yet… just the coil and chip and some extra space is about 240mm^2 per channel… all on topside of board… There are 4 channels…

5. MMFE-8 Termination:

Q: Why do you use external termination and not the internal DIFF_TERM?

A: It was not clear to me that DIFF_TERM would work for the 1.2V IOSTANDARDs... so better to err on the cautious side...

6. LV Power Distribution:

A: On further reflection, perhaps a good place for a "ballast" resistor would be in series with the return leg of the distribution cable between front end board and distribution box. A small resistor, maybe 100 or so millions would equalize the return currents without burning too much power. I'm afraid putting one in series with the board to chamber ground might be problematic.

A: Not sure about the detector power wiring, I think routing should be coincident with Electronics power wiring.

A: Power and power return to the FEBs come from afar and are floating. The power return should be connected to the ground of the FEB

A: I am providing a 10 Ohm resistor between the detector ground pad and analog ground

A: There is no separate analog ground between VMM's.

7. Other Cables:

A: I am providing capacitive AC coupling capabilty for all cable grounds… miniSAS, HDMI, and Ethernet

A: Power Return is assumed to be ground.

8. Grounding:

Q: How small do you think we can get the potential difference between two boards separated by several meters by proper grounding? 0.1mv, 1mv, 10mv,....?

A: We should minimize and equalize the ground paths, then there is only an identical cumulative loss from a single point. This might be a “star” ground? Then we can look at things that delta this like EM effects, corrosion, vibration, etc, and try to mitigate these effects. I guess that if we have the same drop to the ADDC and other cards everything will be at the same potential.

Q: I’m not clear on what our tolerance for the IO is, but I guess we can stand 100mV, Maybe 300? More less? So I am not sure, I think things get better with a higher voltage supply, since there is less current?

A: The loss would be the current times the resistance of the cable, so at 42V, => 0.5A == 0.1V / R => R=0.2, which corresponds to 100 feet of 12ga wire. Note smaller DCDC’s give less margin. Suggest plan is to use redundant 12 ga wires…we are only going 6 feet best, 12 feet worst… So worst case drop is then 100mv * 12’/100’ = 12mV. Of course there are lots of other factors…

Q: How much DC current flow would that cause in a half dozen drain wires in a multi line cable?

A: 32 ga drain wires handle 0.5A ea and there are many in parallel, so no fried wires… Ohms for 32 ga drain wires is ~14 ohms per 100 feet, so 100 times higher resistance. I think very little current goes down the drain…Note the flat cable structure keeps drain wires from affecting each other, only providing an EM coupling effect for the twinax and “coax” which helps considerably dealing with high speed controlled impedance applications like this. 12mV /1 ohm = 12mA per wire worst case.

Q: And worse yet, what happens when the magnetic field of the toroid collapses?

A: My guess is that everything is better off grounded at both ends so that the wires and connected chips are better protected… but I don’t really know… has there been any dynamic field testing done? Do we have a rise time?

Q: On the other hand, AC coupling the drain/Gnd wires at one end only has no effect on the LVDS signal transmission, so I'm not seeing a problem with it. Also, this was done as standard practice for the muon MDT system, and probably many others in ATLAS as well. One more data point: we just did this on the NOvA detector which has approximately 15,000 LVDS data lines coupled in this manner.

A: I’m not an expert here, but I believe this is becoming standard practice in industry. I think disconnecting the ground with high speed impedance controlled signals can cause serious signal integrity effects at the resulting discontinuities, and this is another consideration. Note that it is typical, still, to use AC coupling on the signals

themselves. /however this causes other headaches such as DC balancing and ISI resulting in 8B10B and or HDLC.

Do you know what speed these other systems are operating at? I think we are talking a data rate for us at 200-400Mbps which is getting into GbE speeds…

I really don't like sticking my neck out, so I just suggest the zero ohm resistor approach, in case the worst happens.

The link I provided supplied a rule of thumb, of 25 yards? We are less than that so we should be good…

Q: Are the detectors isolated from the structure?

A: Yes.

Q: The detector reference (ground) should be tied directly to the FEB analog ground, optionally through ferrites, ~1K resistors, .1uF caps?

A: They should be tied directly to board ground of the VMMFE.

A: The HV ground will be decoupled from the LV ground with a small resistor in series, ~ 10 Ohms, as usual for all detectors.

A: Well, Bill, decoupling is necessary in order to prevent that LV currents (DC + AC) can return to the ground via the HV return, if this last is the lowest impedance path to ground. We have to assume that the return paths are not at zero resistance, due to the length of cables, so the LV current can partly flow toward the HV ground without decoupling. Concerning the wattage of the resistor, if we assume that the ground path resistance is of the order of 0. 1 ohm, and we place a 10 ohm resistor, we will have that 1/100 of the LV current can flow through this resistor, so per chamber it will be about 0.1W. Just as a rule of thumb.

A: Because we have to deal also with the DC component, an inductor should not be a good solution. For the fuse, its use can be matter of discussion for general protection of the converters, but if the LV system has the overvoltage trip, as the present ones have, it should be not necessary.

Q: FEB analog power and ground is tied to DC/DC with ferrites.

A: I don't understand the motivation for this. As Lorne pointed out, ferrites don't work in high B fields, but why do you want them anyway?

A: Simulation and measurements show the B field to be <3500 – 4500 Gauss max.

A: Ferrites are currently being tested and are passing with a BSat exceeding 4500 Gauss

A: Some Ferrites have failed.

A: EMI Ferrites help filter ripple currents produced by DCDC and other devices.

Q: FEB digital power and ground is tied to separate DC/DC without ferrites. A: Same as above.

Q: The individual detector panels should be isolated from each other?

A: To be discussed.

Q: As a practical matter, the point of load DC/DC converters on the MMFE will not be isolated... these do not exist in the size, rad hard, price that we need.

Q: DC/DC isolation will need to be accomplished at the facility level near the rim, perhaps on a per 16 MMFE card basis.

Q: Low voltage and high voltage distribution (and grounding) should be done in tandem, so as to prevent current loops.

A: Ok with me. Let's see how Agostino/Dan feel about it.

A: I agree on having HV and LV grounds to be routed in tandem, minimizing the loop surface, but this can be easily done if we can mix them in the same racks, which at the moment is not easy to plan. There is also a discussion on placing the HV in USA15 and not in the cavern.

Q: Faraday shields will not be required due to short analog path lengths, and nearby facility extrusions (which should be tied to detector reference ground in some manner) and lack of additional room...

A: Not required for MMFE-8, used elsewhere

General comment: These things are all to be discussed and sorted out in the Grounding Working Group telecons.