Xilinx Artix 7 - Micro Megas Front End - 8 VMM Card

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THE UNIVERSITY OF ARIZONA

Physics Department
0301-MMFE-8 A
6/17/2014
2:16:59 PM

Services / NRE

PCB1
ASSY_PCB_Layout
PCB layout / 5 boards

PCB2
ASSY_PCB_Man
PCB only

PCB3
ASSY_PCB_Assy
PCB assembly

Accessories

CBL1
CBL-miniSAS-36
miniSAS 4i 36 ckts

CBL2
CBL-miniSAS-36
miniSAS 4i 36 ckts

Title: *0301-MMFE-8_Title*		*University of Arizona* *1118 E 4th St* *Tucson, Arizona 85721* *billhart@email.arizona.edu*
Size: B	Engineer: William Hart	Revision: A
Date: 6/17/2014 Time: 2:16:59 PM	Sheet 1 of 24	
File: C:\Pjcts\AltProj\0301-MMFE 8\0301-MMFE 8-6-17-14\0301-MMFE 8-TitleSheet.SchDoc		

Bank 0:
Contains Configuration and Analog - Digital Converter functionality.
Bank Voltage is 2V5.

N25Q256A11EF840x is256Mb Quad SPI FLASH, used to configure the FPGA. XC7A200T requires 77,845,216b stream.

Since Flash does not typically run at 2V5, translators must be used.

All paired routing is 100 Ohm Differential and length matched TBD
All un-paired routing is 50 Ohm single ended.

JTAG

Diode is used to prevent any current backflow from a Parallel IV cable connection. Diode is probably no-longer required, Pullups are probably no longer required either

Use Digilent JTAG HS1,2 Programming Cable Part # 410-249P-KIT in place of installing JTAG SMT2 Surface-Mount Programming Module.

J9 — GND VREF, GND TMS, GND TCK, GND TDO, GND TDI, GND NC, GND NC — Xilinx Parallel IV Connector

D131 BAS16

RP1 4K7

SPI Flash ROM Signal / Pin Equivalences
C = Clock = Input
DQ0 = Serial Data In = Input
DQ1 = Serial Data Out = Output
S_N = CS = Input
For Quad, DQ pins are BiDirectional...

Per Impact Help:
Micron (Numonyx)
N25Q 3.3V (1) 32Mb – 256Mb Kintex™-7, Artix™-7
N25Q 1.8V (1) 32Mb – 256Mb Kintex-7,Virtex-7, Artix-7
1.For Numonyx N25Q: Top, Bottom, and Uniform block sectors are supported.

Configuration Flash

U10 n25q256a11ef840x

C2 0.22uF 0201 6V3

C3 4.7uF 0402 6V3

FPGA_CCLK

FPGA_SPI_CS#_1

Configuration Done

D129 LTST-C193TBKT-5A

Q1 DMG1012T-SOT523

R1025 49R9 0201

R1096 300R 0201

Place serial termination resistor close to the FPGA

Please Refer to XAPP586

U9G

TDI, TDO, TCK, TMS

FPGA_M0, FPGA_M1, FPGA_M2

FPGA_DONE, FPGA_INIT_B

FPGA_PROGRAM_B, FPGA_CONFIGBVS_25-33

R1033 24R9 0201

R1034 49R9 0201

R1047 49R9 0201

C39 0.001uF 0201 25V

VP_0, VN_0, VREFP0, VREFN0, DXP0, DXN0

FBG484
1.0_1.2_1.8_2.5
XC7A200T-2FBG484I

Connect Vrefp and Vrefn to ground when using internal reference

DX_P and DX_N are the Anode and Cathode of an internal [to the FPGA] temperature sensing diode.

Reconfigure Switch

R1117 4K87 0201

C1 4.7uF 0402 6V3

SW1 — SW_PB_SPST_4POS_SMT

Program Start

XADC SE Analog Mux for last 8 channels

U29 — MAX4781ETE

VCCADC

C432 0.01uF 0201 10V

TDO1, TDO2, TDO3, TDO4, TDO5, TDO6, TDO7, TDO8

MUXADDR0, MUXADDR1, MUXADDR2

XADC_AGND

AGND

Title:	0301-MMFE-8_Bank0
Size:	C
Engineer:	William Hart
Revision:	A
Date:	6/17/2014
Time:	2:16:59 PM
Sheet	2 of 24
File:	C:\Pjcts\AllProj\0301-MMFE_8\0301-MMFE_8-6-17-14\0301-MMFE_8_Bank0.SchDoc

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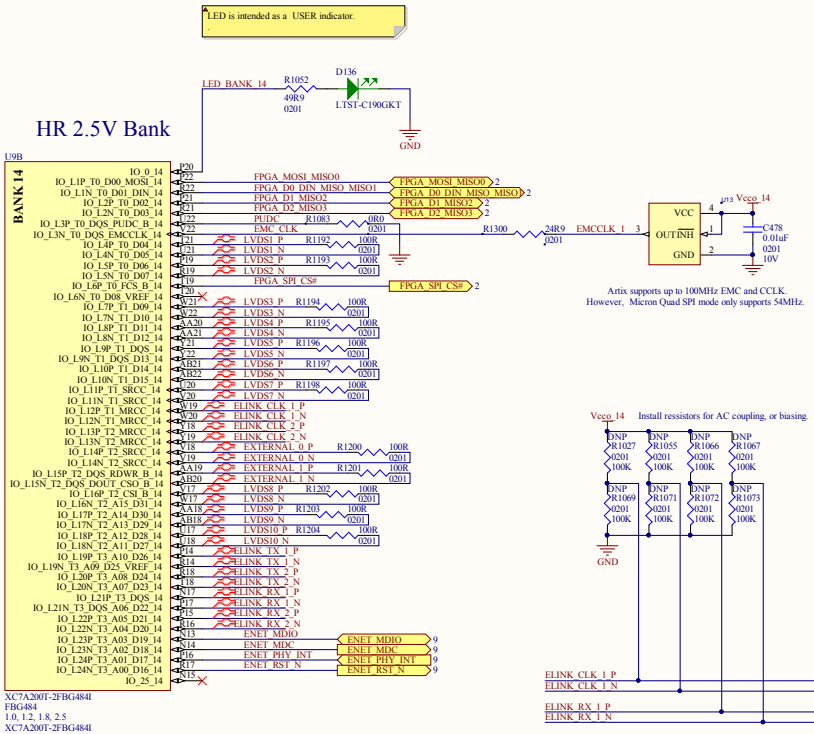
1118 E 4th St
Tucson, Arizona 85721
billhart@email.arizona.edu

HR Bank 14:
Sufficient 2.5V IO for Elink, 2x uHDMI, PHY, External IO.
Ethernet MD Interface:
Trace Impedence = 40 Ohms
Length match to < 385 mil
Spacing is 10 mil for short runs, 4 mils for parallel runs < 500 mils

All paired routing is 100 Ohm Differential and length matched TBD
All un-paired routing is 50 Ohm single ended.

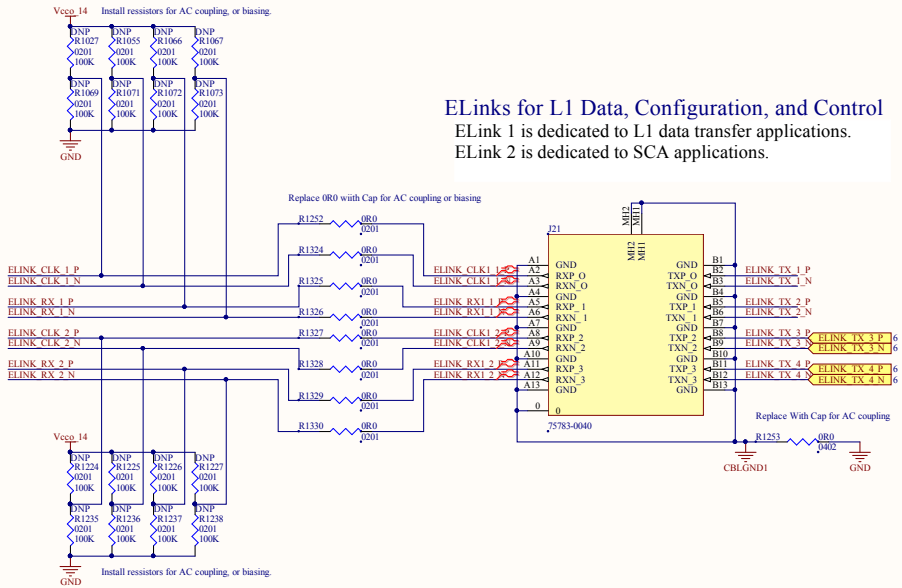
Bank Voltage is at 2.5V, not adjustible due to PHY.
Vref is handled internally by INTERNAL_VREF and pins are available for IO.
DCI is not available in HR banks.
It is unclear whether DIFF_TERM will work correctly.
All non-clock pairs may be pin-swapped as pairs within the bank.
Clock indicated nets are routed to clock input where possible.

HR 2.5V Bank

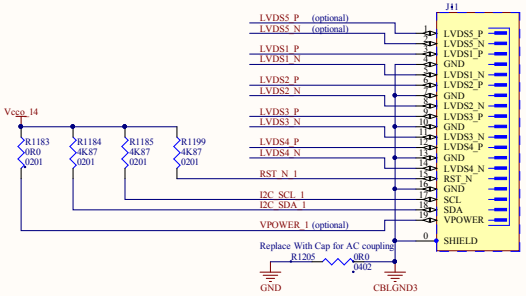


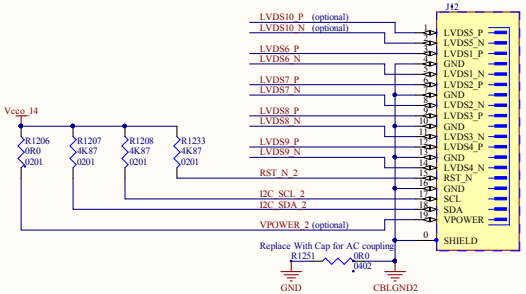
ELinks for L1 Data, Configuration, and Control

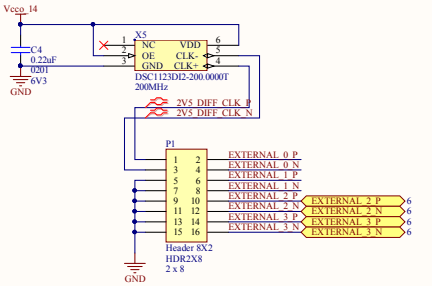
ELink 1 is dedicated to L1 data transfer applications.
ELink 2 is dedicated to SCA applications.



2V5 HDMI for SRS etc...

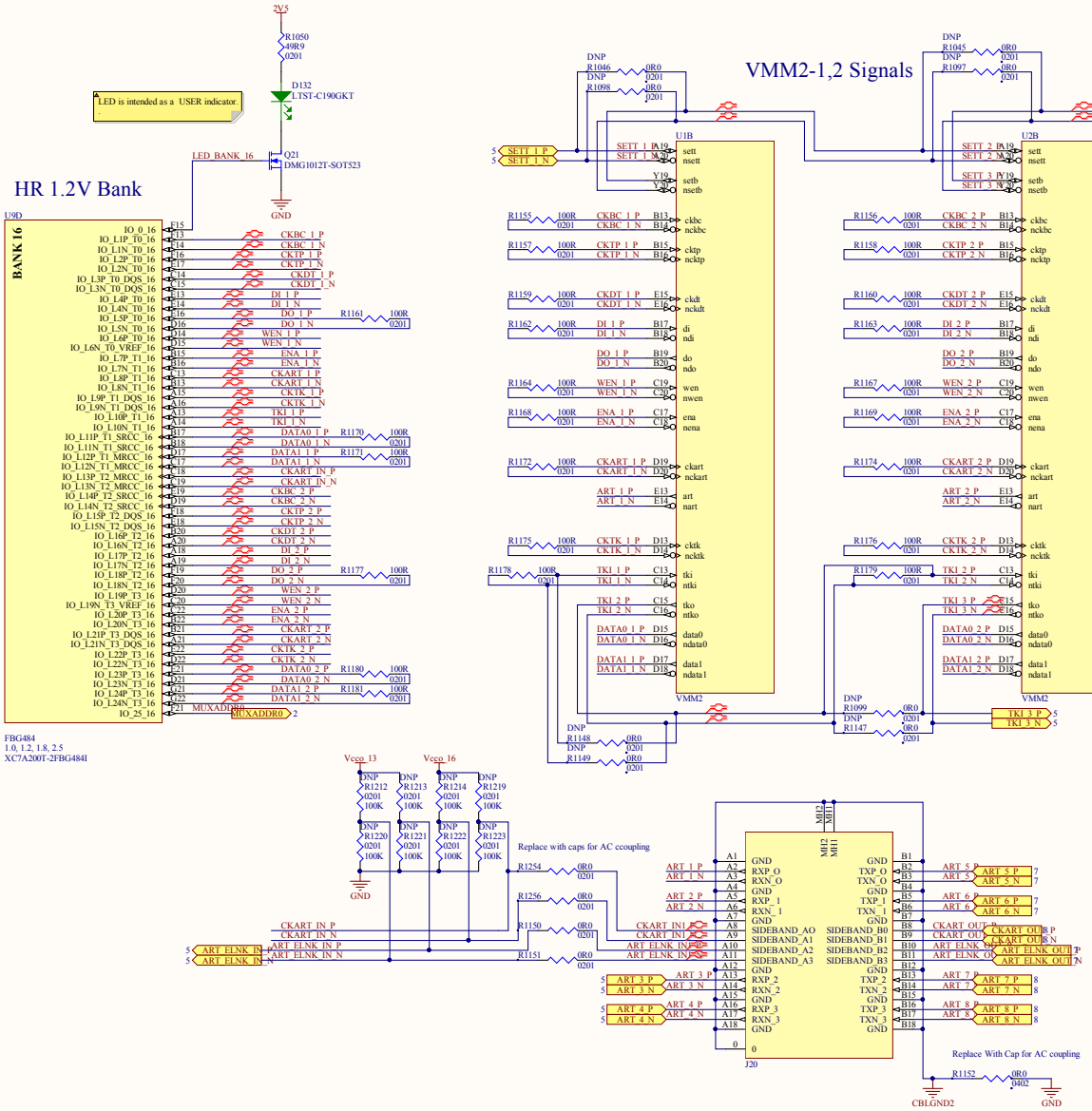






Title: 0301-MMFE-8_Bank16			University of Arizona 1118 E 4th St Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 6/17/2014	Time: 2:16:59 PM	Sheet 3 of 24	
File: C:\Pjcts\AllProj\0301-MMFE 8\0301-MMFE 8-6-17-14\0301-MMFE 8-Bank16.SchDoc			Drawn By: William Hart

HR Bank 16:
Sufficient 1.2V Differential IO for 2 VMM, Clock to / from ART.
8 Differential Analog Inputs
All paired routing is 100 Ohm Differential and length matched TBD
All un-paired routing is 50 Ohm single ended.
Bank Voltage is at 1.2V.
Vref is handled internally by INTERNAL_VREF and pins are available for IO.
DCI is not available in HR banks.
It is unclear whether DIFF_TERM will work correctly.
All non-clock pairs may be pin-swapped as pairs within the bank.
Clock indicated nets are routed to clock input where possible.



ART Data, Data Clock Out, Timing Clock In

Title: 0301-MMFE-8_Bank12			University of Arizona 1118 E 4th St Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	
Date: 6/17/2014	Time: 2:17:00 PM	Sheet 4 of 24	billhart@email.arizona.edu
File: C:\Pjcts\AllProj\0301-MMFE_8\0301-MMFE_8-6-17-14\0301-MMFE_8-Bank12.SchDoc			Drawn by: William Hart

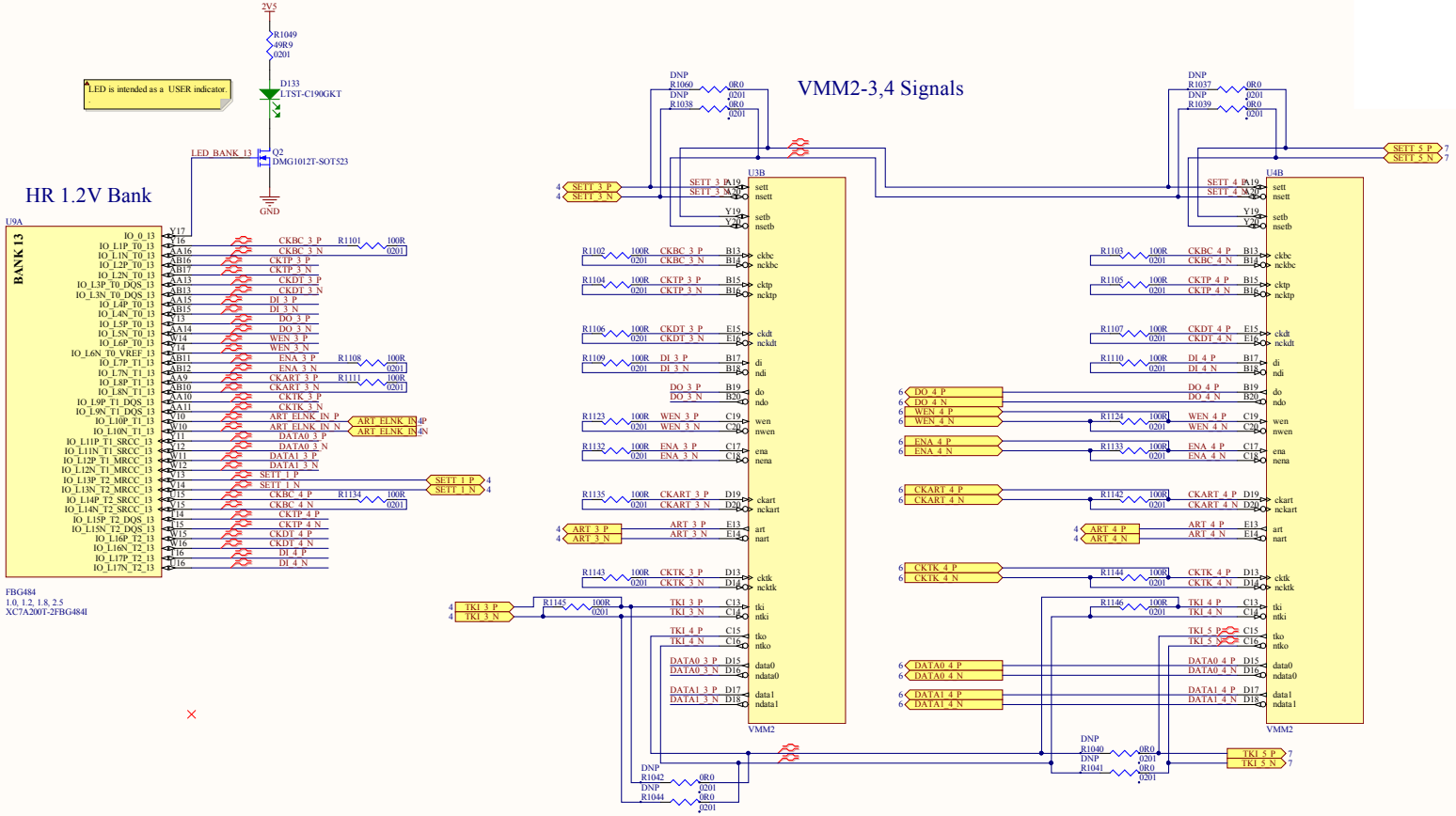
HR Bank 13:
Sufficient 1.2V Differential IO for 1.5 VMM.
All paired routing is 100 Ohm Differential and length matched TBD
All un-paired routing is 50 Ohm single ended.
Bank Voltage is at 1.2V.
Vref is handled internally by INTERNAL_VREF and pins are available for IO.
DCI is not available in HR banks.
It is unclear whether DIFF_TERM will work correctly.
All non-clock pairs may be pin-swapped as pairs within the bank.
Clock indicated nets are routed to clock input where possible.

sett: ch0 neighbor trigger
ckbc: BC clock (timestamp Gray-code counter advance)
cktp: test pulse clock
di: configuration data input
do: configuration data output
tki: token input (in analog mode)
tko: token output (in analog mode)

ena: acquisition start/stop
ena high, wen low: acquisition is enabled
internally enabled after 40ns from ena high
in two-phase (analog) mode is acquisition
in continuous (digital) mode is acquisition and readout
ena low, wen low: in two-phase mode is readout
ena pulse, wen high: global reset (acquisition and registers)

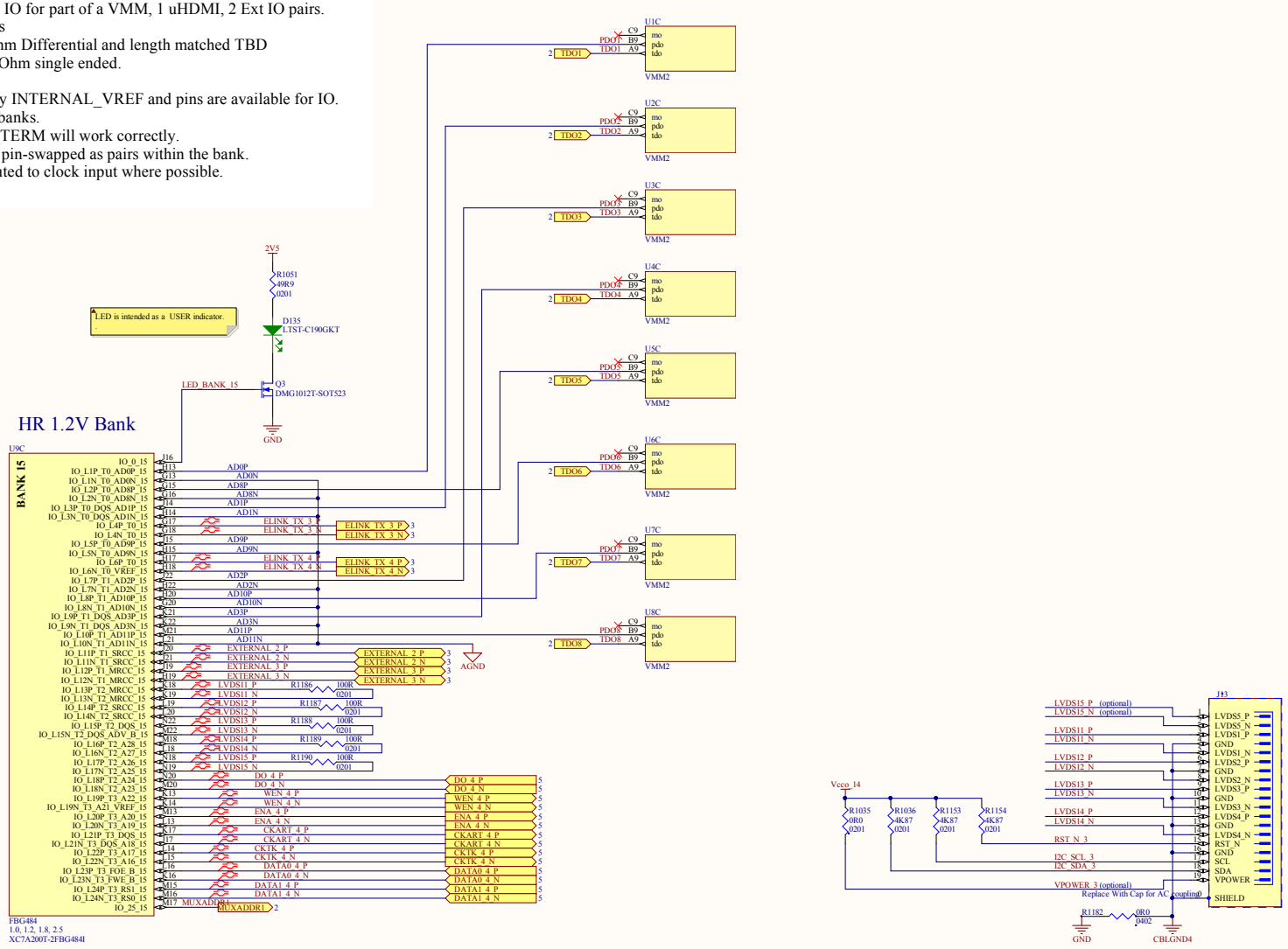
wen: configuration enable
wen high: configuration mode
wen pulse: acquisition reset (also resets BC counter)

cktk: token clock
data0: flag and first data line (flag and address in analog mode)
data1: second data line
ckart: ART clock
art: ART output
ckdt: configuration (data input), data output and 6-bit ADC clock
setb: ch63 neighbor trigger



Title: 0301-MMFE-8_Bank13			University of Arizona 1118 E 4th St Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 6/17/2014	Time: 2:17:00 PM	Sheet 5 of 24	
File: C:\Pjcts\AllProj\0301-MMFE_8\0301-MMFE_8-6-17-14\0301-MMFE_8_Bank13.SchDoc			Drawn by: William Hart

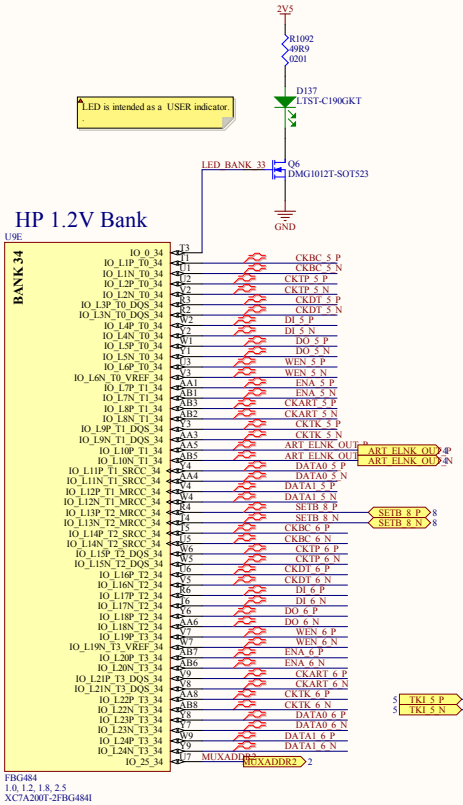
HR Bank 15:
Sufficient 1.2V Differential IO for part of a VMM, 1 uHDMI, 2 Ext IO pairs.
8 Differential Analog Inputs
All paired routing is 100 Ohm Differential and length matched TBD
All un-paired routing is 50 Ohm single ended.
Bank Voltage is at 1.2V.
Vref is handled internally by INTERNAL_VREF and pins are available for IO.
DCI is not available in HR banks.
It is unclear whether DIFF_TERM will work correctly.
All non-clock pairs may be pin-swapped as pairs within the bank.
Clock indicated nets are routed to clock input where possible.



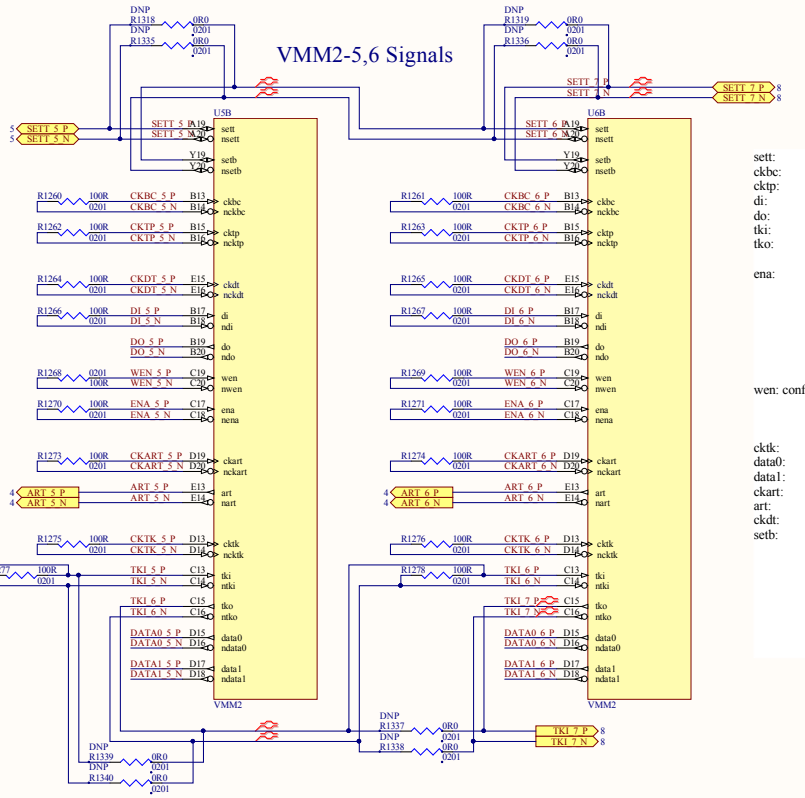
Title: 0301-MMFE-8_Bank15			University of Arizona 1118 E 4th St Tucson, Arizona 85721 billhart@email.arizona.edu
Size: C	Engineer: William Hart	Revision: A	
Date: 6/17/2014	Time: 2:17:00 PM	Sheet 6 of 24	
File: C:\Pjcts\AltProj\0301-MMFE 8\0301-MMFE 8-6-17-14\0301-MMFE 8-Bank15.SchDoc			Drawn By: William Hart

HR Bank 35:
Sufficient 1.2V Differential IO for 2 VMM's.
All paired routing is 100 Ohm Differential and length matched TBD
All un-paired routing is 50 Ohm single ended.
Bank Voltage is at 1.2V.
Vref is handled internally by INTERNAL_VREF and pins are available for IO.
DCI is available in HP banks.
It is unclear whether DIFF_TERM will work correctly.
All non-clock pairs may be pin-swapped as pairs within the bank.
Clock indicated nets are routed to clock input where possible.

HP 1.2V Bank



VMM2-5,6 Signals



sett: ch0 neighbor trigger
ckbc: BC clock (timestamp Gray-code counter advance)
cktp: test pulse clock
di: configuration data input
do: configuration data output
tki: token input (in analog mode)
tko: token output (in analog mode)

ena: acquisition start/stop
ena high, wen low: acquisition is enabled
internally enabled after 40ns from ena high
in two-phase (analog) mode is acquisition
in continuous (digital) mode is acquisition and readout
ena low, wen low: in two-phase mode is readout
ena pulse, wen high: global reset (acquisition and registers)

wen: configuration enable
wen high: configuration mode
wen pulse: acquisition reset (also resets BC counter)

cktk: token clock
data0: flag and first data line (flag and address in analog mode)
data1: second data line
ckart: ART clock
art: ART output
ckdt: configuration (data input), data output and 6 -bit ADC clock
setb: ch63 neighbor trigger

Title: 0301-MMFE-8_Bank33			University of Arizona 1118 E 4th St Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 6/17/2014	Time: 2:17:00 PM	Sheet 7 of 24	
File: C:\Pjcts\AllProj\0301-MMFE_8\0301-MMFE_8-6-17-14\0301-MMFE_8-Bank33.SchDoc			Drawn by: William Hart

HR Bank 34:
Sufficient 1.2V Differential IO for 2 VMM's.
All paired routing is 100 Ohm Differential and length matched TBD
All un-paired routing is 50 Ohm single ended.
Bank Voltage is at 1.2V.
Vref is handled internally by INTERNAL_VREF and pins are available for IO.
DCI is available in HP banks.
It is unclear whether DIFF_TERM will work correctly.
All non-clock pairs may be pin-swapped as pairs within the bank.
Clock indicated nets are routed to clock input where possible.

Board to Board neighbor connector is not needed

LED is intended as a USER indicator.

2V5
R1084 49R9 0201
D138 LTST-C190GKT
LED_BANK_34
Q7 DMG1012T-SOT523
GND

HP 1.2V Bank

U9F
BANK 35

IO_0_35	F4	
IO_L1P_T0_AD4P_35	G1	CKBC_7_P
IO_L1N_T0_AD4N_35	A1	CKBC_7_N
IO_L2P_T0_AD12P_35	B2	CKTP_7_P
IO_L2N_T0_AD12N_35	B1	CKTP_7_N
IO_L3P_T0_DQS_AD5P_35	E1	CKDT_7_P
IO_L3N_T0_DQS_AD5N_35	D1	CKDT_7_N
IO_L4P_T0_35	F2	DI_7_P
IO_L4N_T0_35	G2	DI_7_N
IO_L5P_T0_AD13P_35	D1	DO_7_P
IO_L5N_T0_AD13N_35	F1	DO_7_N
IO_L6P_T0_35	E3	WEN_7_P
IO_L6N_T0_VREF_35	E3	WEN_7_N
IO_L7P_T1_AD6P_35	E1	ENA_7_P
IO_L7N_T1_AD6N_35	F1	ENA_7_N
IO_L8P_T1_AD14P_35	H2	CKART_7_P
IO_L8N_T1_AD14N_35	G2	CKART_7_N
IO_L9P_T1_DQS_AD7P_35	F2	CKTK_7_P
IO_L9N_T1_DQS_AD7N_35	F2	CKTK_7_N
IO_L10P_T1_AD15P_35	J5	TKO_8_P
IO_L10N_T1_AD15N_35	J5	TKO_8_N
IO_L11P_T1_SRCC_35	H3	DATA0_7_P
IO_L11N_T1_SRCC_35	G3	DATA0_7_N
IO_L12P_T1_MRCC_35	J4	DATA1_7_P
IO_L12N_T1_MRCC_35	H4	DATA1_7_N
IO_L13P_T2_MRCC_35	K4	CKART_OUT_P
IO_L13N_T2_MRCC_35	K4	CKART_OUT_N
IO_L14P_T2_SRCC_35	K3	CKBC_8_P
IO_L14N_T2_SRCC_35	K3	CKBC_8_N
IO_L15P_T2_DQS_35	M1	CKTP_8_P
IO_L15N_T2_DQS_35	L1	CKTP_8_N
IO_L16P_T2_35	M3	CKDT_8_P
IO_L16N_T2_35	M2	CKDT_8_N
IO_L17P_T2_35	L6	DI_8_P
IO_L17N_T2_35	L6	DI_8_N
IO_L18P_T2_35	L5	DO_8_P
IO_L18N_T2_35	L4	DO_8_N
IO_L19P_T3_35	N4	WEN_8_P
IO_L19N_T3_VREF_35	N3	WEN_8_N
IO_L20P_T3_35	P1	ENA_8_P
IO_L20N_T3_35	P1	ENA_8_N
IO_L21P_T3_DQS_35	P5	CKART_8_P
IO_L21N_T3_DQS_35	P4	CKART_8_N
IO_L22P_T3_35	P2	CKTK_8_P
IO_L22N_T3_35	R2	CKTK_8_N
IO_L23P_T3_35	M6	DATA0_8_P
IO_L23N_T3_35	M5	DATA0_8_N
IO_L24P_T3_35	P6	DATA1_8_P
IO_L24N_T3_35	R5	DATA1_8_N
IO_25_35	L6	MUXADDR3

MUXADDR3 2

FBG484
1.0_1.2_1.8_2.5
XC7A200T-2FBG484I

VMM2-7,8 Signals

U7B VMM2 — U8B VMM2

SETT_7_P	A19	sett	SETT_8_P	A19	sett
SETT_7_N	A20	nsett	SETT_8_N	A20	nsett
	Y19	setb	SETB_8_P	Y19	setb
	Y20	nsetb	SETB_8_N	Y20	nsetb
CKBC_7_P	B13	ckbc	CKBC_8_P	B13	ckbc
CKBC_7_N	B14	nckbc	CKBC_8_N	B14	nckbc
CKTP_7_P	B15	cktp	CKTP_8_P	B15	cktp
CKTP_7_N	B16	ncktp	CKTP_8_N	B16	ncktp
CKDT_7_P	E15	ckdt	CKDT_8_P	E15	ckdt
CKDT_7_N	E16	nckdt	CKDT_8_N	E16	nckdt
DI_7_P	B17	di	DI_8_P	B17	di
DI_7_N	B18	ndi	DI_8_N	B18	ndi
DO_7_P	B19	do	DO_8_P	B19	do
DO_7_N	B20	ndo	DO_8_N	B20	ndo
WEN_7_P	C19	wen	WEN_8_P	C19	wen
WEN_7_N	C20	nwen	WEN_8_N	C20	nwen
ENA_7_P	C17	ena	ENA_8_P	C17	ena
ENA_7_N	C18	nena	ENA_8_N	C18	nena
CKART_7_P	D19	ckart	CKART_8_P	D19	ckart
CKART_7_N	D20	nckart	CKART_8_N	D20	nckart
ART_7_P	E13	art	ART_8_P	E13	art
ART_7_N	E14	nart	ART_8_N	E14	nart
CKTK_7_P	D13	cktk	CKTK_8_P	D13	cktk
CKTK_7_N	D14	ncktk	CKTK_8_N	D14	ncktk
TKI_7_P	C13	tki	TKI_8_P	C13	tki
TKI_7_N	C14	ntki	TKI_8_N	C14	ntki
TKI_8_P	C15	tko	TKO_8_P	C15	tko
TKI_8_N	C16	ntko	TKO_8_N	C16	ntko
DATA0_7_P	D15	data0	DATA0_8_P	D15	data0
DATA0_7_N	D16	ndata0	DATA0_8_N	D16	ndata0
DATA1_7_P	D17	data1	DATA1_8_P	D17	data1
DATA1_7_N	D18	ndata1	DATA1_8_N	D18	ndata1

DNP R1255 0R0 0201
DNP R1258 0R0 0201
DNP R1257 0R0 0201
DNP R1279 0R0 0201
DNP R1280 0R0 0201
DNP R1281 0R0 0201
DNP R1282 0R0 0201
DNP R1316 0R0 0201

R1209 100R 0201 CKBC_7_P — CKBC_7_N
R1210 100R 0201 CKBC_8_P — CKBC_8_N
R1215 100R 0201 CKTP_7_P — CKTP_7_N
R1216 100R 0201 CKTP_8_P — CKTP_8_N
R1217 100R 0201 CKDT_7_P — CKDT_7_N
R1218 100R 0201 CKDT_8_P — CKDT_8_N
R1239 100R 0201 DI_7_P — DI_7_N
R1240 100R 0201 DI_8_P — DI_8_N
R1241 100R 0201 WEN_7_P — WEN_7_N
R1242 100R 0201 WEN_8_P — WEN_8_N
R1243 100R 0201 ENA_7_P — ENA_7_N
R1244 100R 0201 ENA_8_P — ENA_8_N
R1245 100R 0201 CKART_7_P — CKART_7_N
R1246 100R 0201 CKART_8_P — CKART_8_N
R1247 100R 0201 CKTK_7_P — CKTK_7_N
R1248 100R 0201 CKTK_8_P — CKTK_8_N
R1240 0201 100R TKI_7_P — TKI_7_N
R1250 100R 0201 TKI_8_P — TKI_8_N

SETT_7_P, SETT_7_N
SETB_8_P, SETB_8_N
ART_7_P, ART_7_N
ART_8_P, ART_8_N
TKI_7_P, TKI_7_N

sett: ch0 neighbor trigger
ckbc: BC clock (timestamp Gray-code counter advance)
cktp: test pulse clock
di: configuration data input
do: configuration data output
tki: token input (in analog mode)
tko: token output (in analog mode)

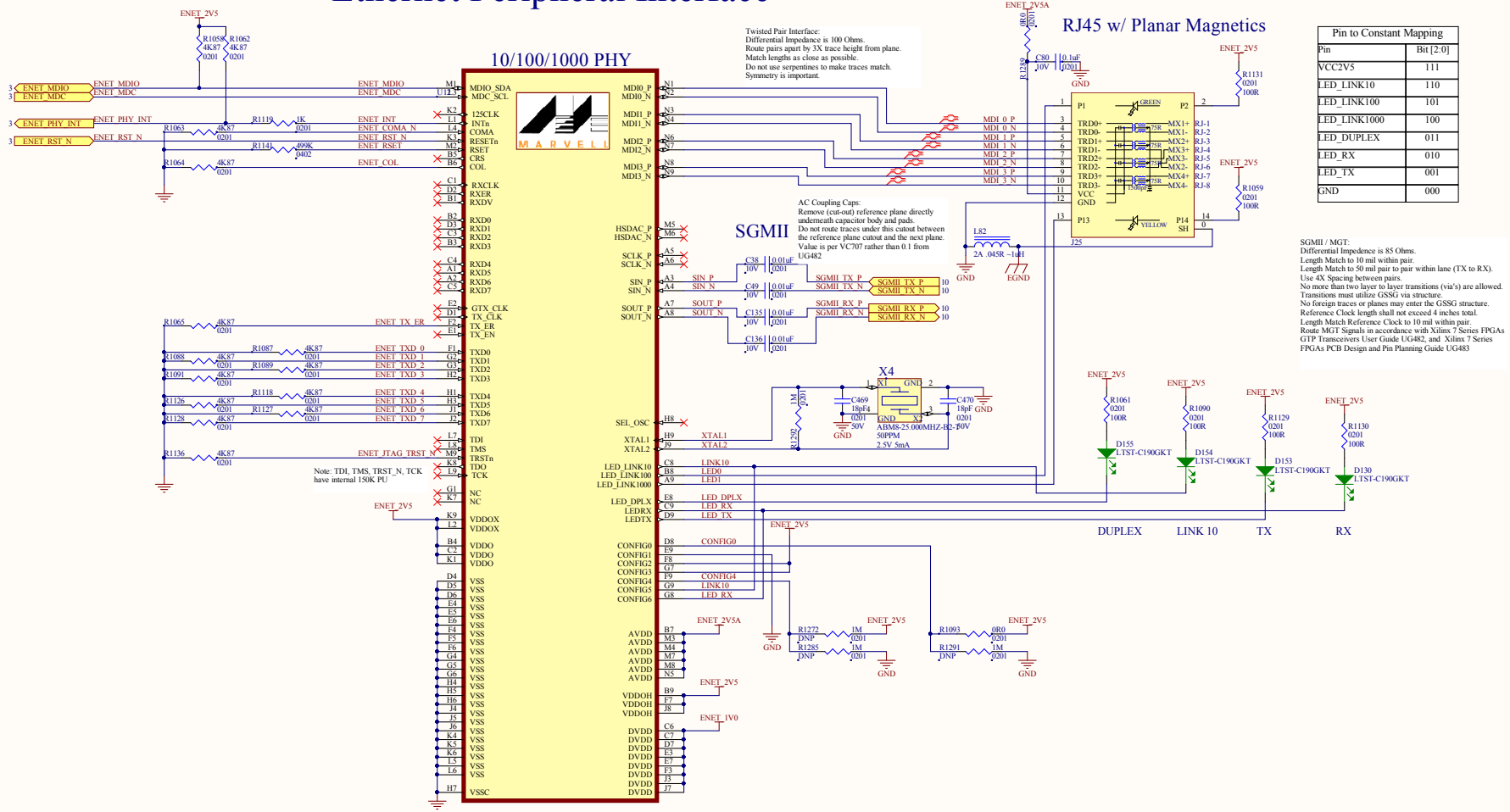
ena: acquisition start/stop
- ena high, wen low: acquisition is enabled
  - internally enabled after 40ns from ena high
  - in two-phase (analog) mode is acquisition
  - in continuous (digital) mode is acquisition and readout
- ena low, wen low: in two-phase mode is readout
- ena pulse, wen high: global reset (acquisition and registers)

wen: configuration enable
- wen high: configuration mode
- wen pulse: acquisition reset (also resets BC counter)

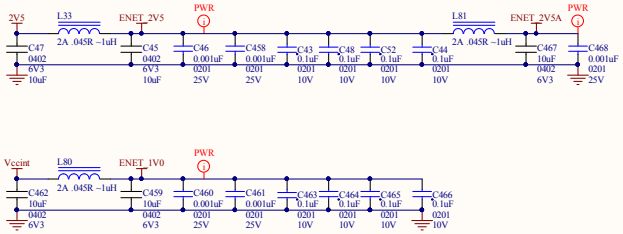
cktk: token clock
data0: flag and first data line (flag and address in analog mode)
data1: second data line
ckart: ART clock
art: ART output
ckdt: configuration (data input), data output and 6 - bit ADC clock
setb: ch63 neighbor trigger

Title: 0301-MMFE-8_Bank34			University of Arizona 1118 E 4th St Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 6/17/2014	Time: 2:17:00 PM	Sheet 8 of 24	
File: C:\Pjcts\AllProj\0301-MMFE_8\0301-MMFE_8-6-17-14\0301-MMFE_8-6-17-14.SchDoc			

Ethernet Peripheral Interface



Pin to Constant Mapping	
Pin	Bit [2:0]
VCC2V5	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
GND	000



Pin	Bit[2]	Bit[1]	Bit[0]		
CFG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	111	PHYAddr "00111". Don't advertise the PAUSE bit
CFG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	
CFG2	ANEG[3]	ANEG[2]	ANEG[1]	111	Auto-Neg en, advertise all caps; prefer slave. Auto crossover enabled. 125 CLK option disabled.
CFG3	ANEG[0]	ENA_XC	DIS_125	111	
CFG4	HWCFG_MD[2]	HWCFG_MD[1]	HWCFG_MD[0]	111	GMII to Cu mode. Fiber/copper auto-detect disabled. Sleep mode disabled.
CFG5	DIS_FC	DIS_SLEEP	HWCFG_MD[3]	111	
CFG6	SEL_BDT	INT_POL	75/50 OHM	010	MDC/MDIO selected. Active LOW interrupt 500hm SERDES option.

Title: 0301-MMFE-8_Ethernet			University of Arizona 1118 E 4th St Tucson, Arizona 85721
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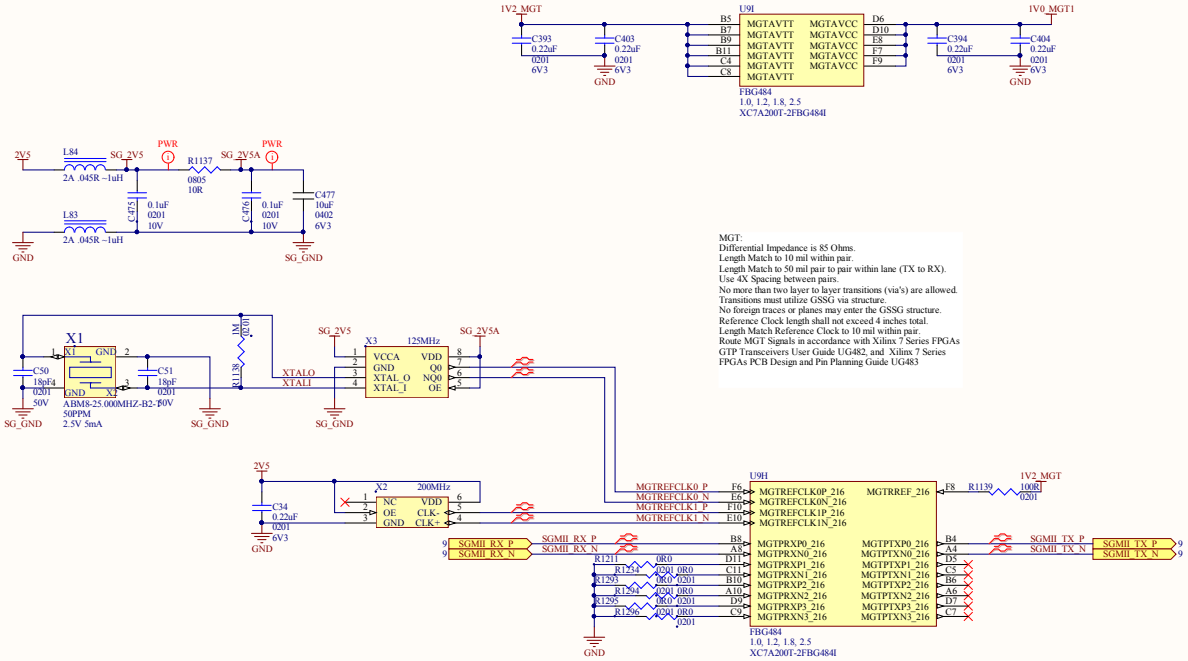
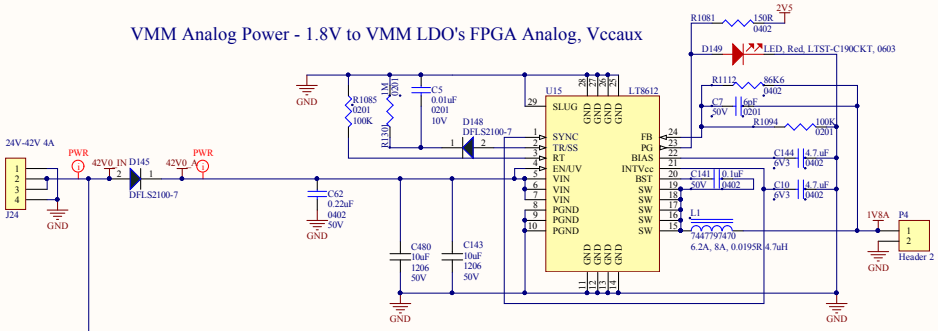
File: C:\Pjcts\AllProj\0301-MMFE 8\0301-MMFE 8-6-17-14\0301-MMFE-8_Ethernet.SchDoc			Drawn by: William Hart



Title: 0301-MMFE-8_MGT			University of Arizona 1118 E 4th St Tucson, Arizona 85721 billhart@email.arizona.edu
Size: C	Engineer: William Hart	Revision: A	
Date: 6/17/2014	Time: 2:17:01 PM	Sheet 10 of 24	
File: C:\Pjcts\AltProj\0301-MMFE 8\0301-MMFE 8-6-17-14\0301-MMFE 8-MGT.SchDoc		Drawn By: William Hart	

VMM Analog Power - 1.8V to VMM LDO's FPGA Analog, Vccaux

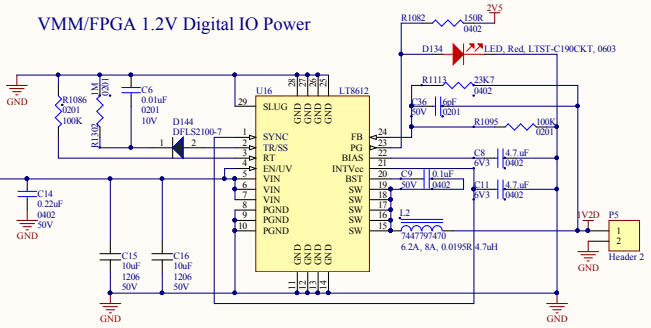


LT8612: R1(vout)=R2(gnd) x (Vout /0.970V -1)
1.0V => K=0.0309, R2=100K R1=3K09
1.2V => K=0.2371, R2=100K R1=23K7
1.5V => K=0.5464, R2=100K R1=54K6
1.8V => K=0.8557, R2=100K R1=85K6
2.5V=> K=1.5773, R2=100K R1=157K8

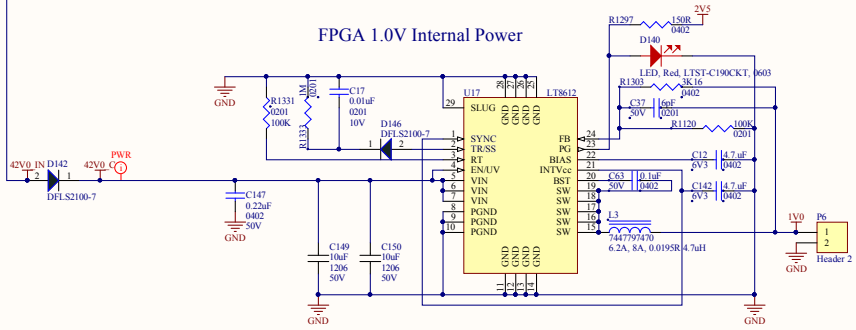
LT8612 Table 1.
SW Freq MHz vs RT Value kΩ

fsw	Rrt	fsw	Rrt
0.2	232	1.0	41.2
0.3	150	1.2	33.2
0.4	110	1.4	28.0
0.5	88.7	1.6	23.7
0.6	71.5	1.8	20.5
0.7	60.4	2.0	18.2
0.8	52.3	2.2	15.8

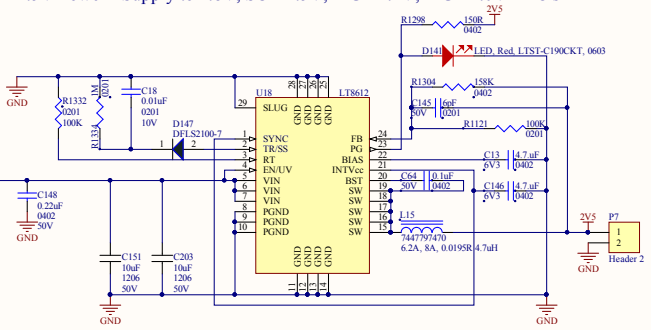
VMM/FPGA 1.2V Digital IO Power



FPGA 1.0V Internal Power



FPGA 2.5V Power - Supply to 1.8V, SCA 1.5V, MGT 1.2V, MGT 1.0V LDO's



When laying out power, it is recomended to route point to point with trace width sufficient to carry the required current. Then pours or splits can be instantiated, without fear of islands or choke points. This is especially crittical for FPGA power distribution.

VMM:
1.8Vanlg: Direct from LTM4619_1_A
Ianlg18 = 3.4A + losses

1.8Vdgtl: Direct from LTM4619_1_B
Idgtl18 = 1.2A + losses

8x 1.2Vanlg: From LTM4619_1_A via LT3080_1-8
Ianlg12 = .427A

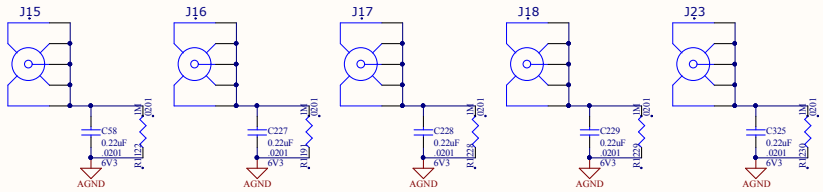
8x 1.2Vdgtl: From LTM4619_1_B via LT3080_9-16
Idgtl12 = .150A

FPGA:
1V: Direct from LTM4619_2_A
Iccint = 3.15A, Iccbram = .100A
1V MGT: From LTM4619_2_B via LT3080_17
Imgtavcc = 0.511A
1.2V: From LTM4619_2_B via LT3080_19, 20
Icco = .621A
1.2V MGT: From LTM4619_2_B via LT3080_18
Imgtavtt = .36A
1.8V: Direct from LTM4619_2_B or via LT3080_21
Iccaux = .32A
2.5V: If needed for LVDS Direct from LTM4619_2_B
Icco = .621A

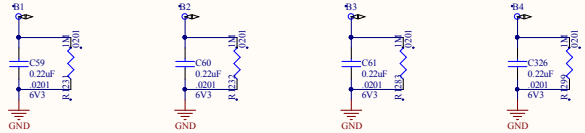
Iccauxq (Vaux Quiescent) = 7mA
1.8V LVCMOS25 or 33 = 2-24mA per pin

1.2V SSTL / HSTL 8mA per pin max

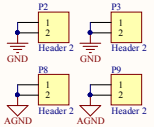
MMCX Coax Connectors for mounting and grounding Current location and usage is TBD



B1 ... B4
screw holes for mounting location is TBD

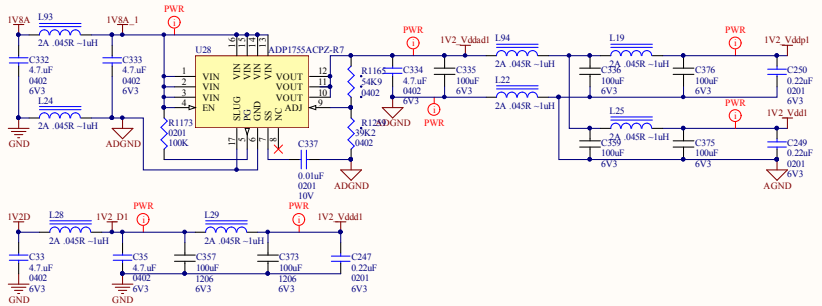


Ground Referance for Probes

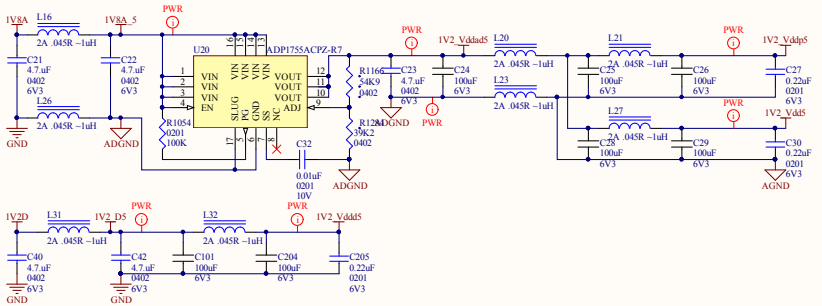


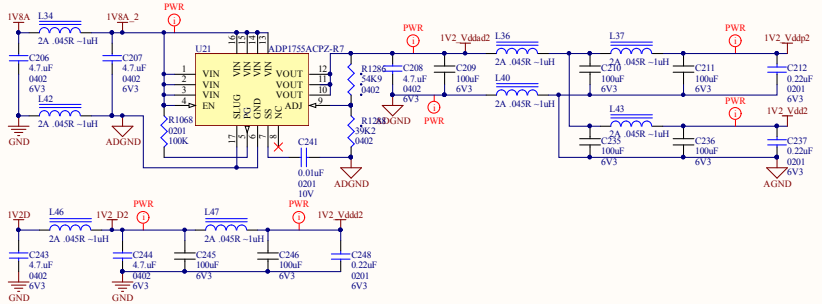
ESR:
DF = tan(phi) = ESR / Xc = 0.1 for CC
ESR = DF * Xc = DF / (2*pi*fC) = Xc / Q = tan(phi) * Xc
Z = (ESR^2 + (Xl-Xc)^2)^0.5
Fr = 1 / (2*pi*(L*C)^0.5)
Spec for Al and Film caps @100KHz
Spec for Al and Tant @120Hz
ESR = Rsdielc(0-3MHz) + Rsmetal(30-300MHz)
ESRf2 = ESRf1 * (f2/f1)^0.5
ESR calculations for ceramic caaps use DF of 10%, meas'd @ 120 Hz, used @ 1MHz = 0.005Ohms worst case.

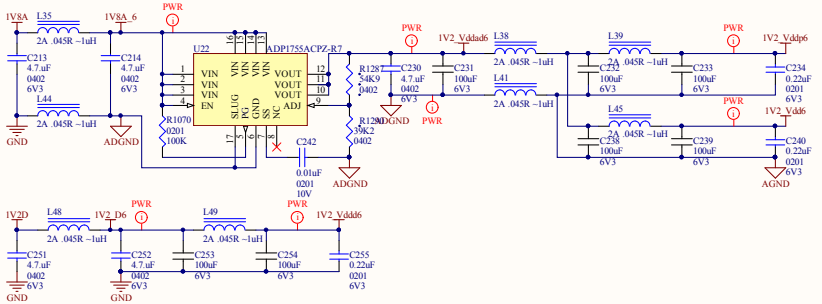
Title: 0301-MMFE-8_Power1			University of Arizona 1118 E 4th St Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 6/17/2014	Time: 2:17:01 PM	Sheet 11 of 24	
File: C:\Pjcts\AllProj\0301-MMFE 8\0301-MMFE 8-6-17-14\0301-MMFE 8_Power1.SchDoc			Drawn by: William Hart

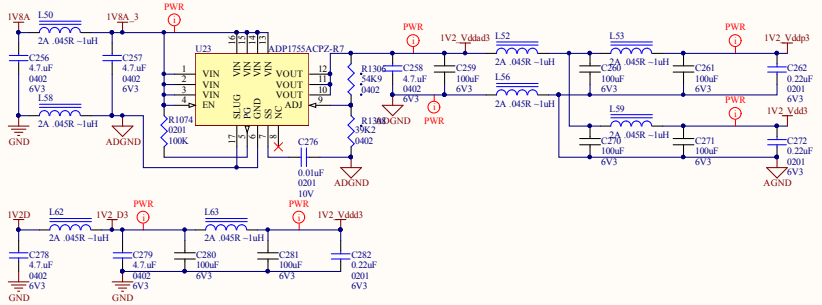


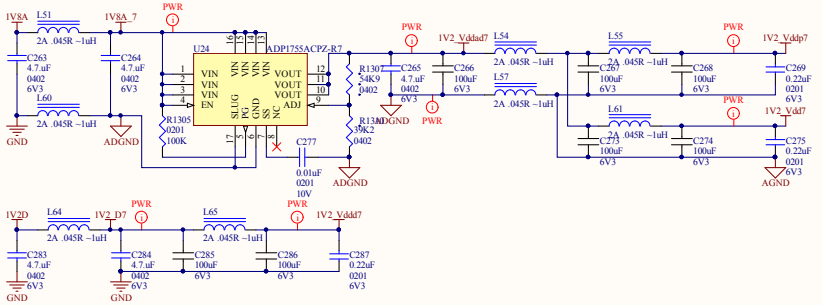
LT8640:
VOUT = 0.5 V × (1 + Rvout / Rgnd)
2 * VOUT = 1 + Rvout / Rgnd
(2 * VOUT) - 1 = Rvout / Rgnd
((2 * VOUT) - 1) * Rgnd = Rvout
Rgnd < 60K
Rgnd = 39.2K, VOUT = 1.0 => Rvout = 39.2K
Rgnd = 39.2K, VOUT = 1.2 => Rvout = 54.9K
Rgnd = 39.2K, VOUT = 1.5 => Rvout = 78.4K
Rgnd = 39.2K, VOUT = 1.8 => Rvout = 101.9K

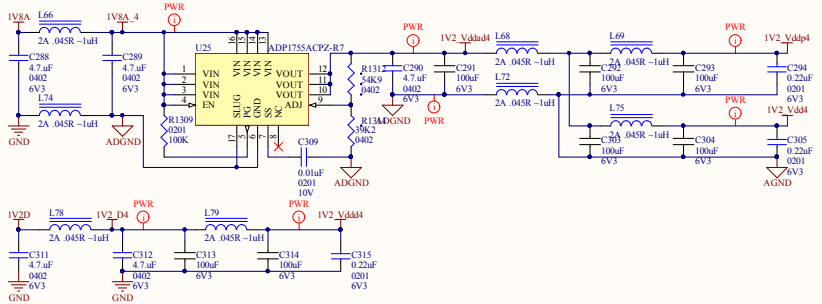


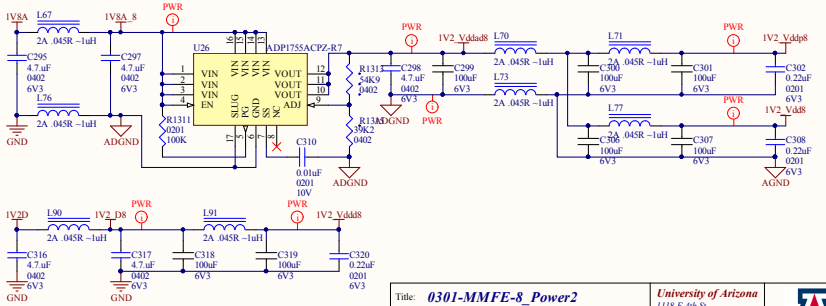




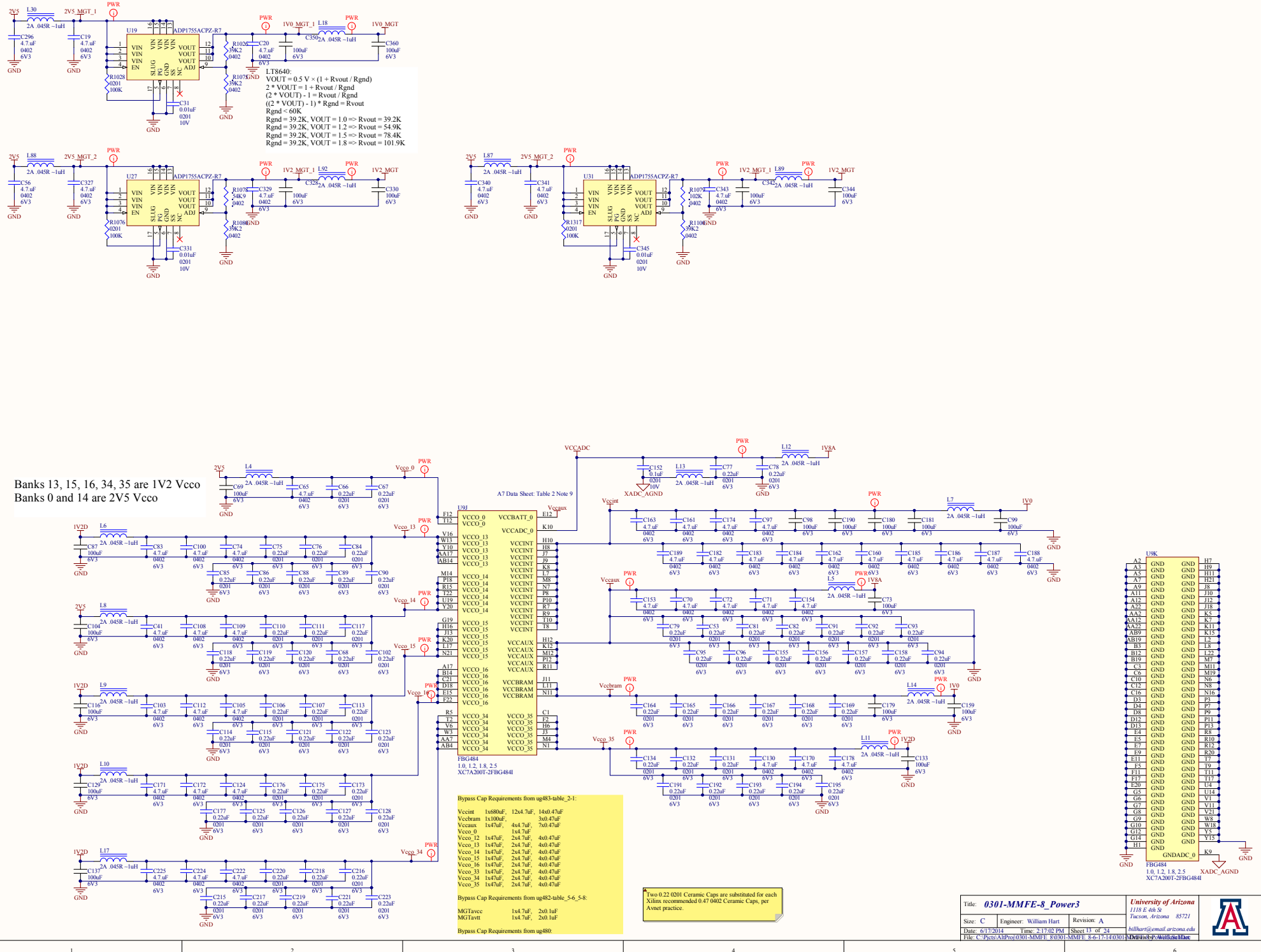








Title: 0301-MMFE-8_Power2			University of Arizona 1118 E 4th St Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 6/17/2014	Time: 2:17:01 PM	Sheet 12 of 24	
File: C:\Pjcts\AltProj\0301-MMFE 8\0301-MMFE 8-6-17-14\0301-MMFE 8-Power2.SchDoc			Drawn by: William Hart


2V5
L30
2A .045R ~1uH
2V5_MGT_1
PWR
U19
ADP1755ACPZ-R7
VIN
VOUT
ADJ
SLUG
PG
GND
NC
EN
C296
4.7 uF
0402
6V3
C19
R1028
0201
100K
R1026
39K2
0402
R1075
C20
C31
0.01uF
0201
10V
1V0_MGT_1
L18
2A .045R ~1uH
C350
100uF
6V3
1V0_MGT
C360
LT8640:
VOUT = 0.5 V × (1 + Rvout / Rgnd)
2 * VOUT = 1 + Rvout / Rgnd
(2 * VOUT) - 1 = Rvout / Rgnd
((2 * VOUT) - 1) * Rgnd = Rvout
Rgnd < 60K
Rgnd = 39.2K, VOUT = 1.0 => Rvout = 39.2K
Rgnd = 39.2K, VOUT = 1.2 => Rvout = 54.9K
Rgnd = 39.2K, VOUT = 1.5 => Rvout = 78.4K
Rgnd = 39.2K, VOUT = 1.8 => Rvout = 101.9K
L88
2V5_MGT_2
U27
R1076
R1078
54K9
R1080
C329
C328
1V2_MGT_1
L92
1V2_MGT
C330
C327
C56
C331
L87
U31
R1317
R1079
102K
R1106
C343
C342
C344
C340
C341
C345
Banks 13, 15, 16, 34, 35 are 1V2 Vcco
Banks 0 and 14 are 2V5 Vcco
L4
Vcco_0
C69
C65
C66
C67
A7 Data Sheet: Table 2 Note 9
U9J
VCCO_0
VCCBATT_0
VCCADC_0
VCCINT
VCCAUX
VCCBRAM
VCCO_13
VCCO_14
VCCO_15
VCCO_16
VCCO_34
VCCO_35
FBG484
1.0, 1.2, 1.8, 2.5
XC7A200T-2FBG484I
VCCADC
XADC_AGND
C152
0.1uF
10V
L13
C77
C78
L12
1V8A
Vccint
Vccaux
Vccbram
L7
1V0
L5
L14
L11
1V2D
C163
C161
C174
C97
C98
C190
C180
C181
C99
C189
C182
C183
C184
C162
C160
C185
C186
C187
C188
C153
C70
C72
C71
C154
C73
C79
C53
C81
C82
C91
C92
C93
C95
C96
C155
C156
C157
C158
C94
C164
C165
C166
C167
C168
C169
C179
C159
C134
C132
C131
C130
C170
C178
C133
C191
C192
C193
C194
C195
U9K
GNDADC_0
XADC_AGND
Bypass Cap Requirements from ug483-table_2-1:
Vccint 1x680uF, 12x4.7uF, 14x0.47uF
Vccbram 1x100uF, 3x0.47uF
Vccaux 1x47uF, 4x4.7uF, 7x0.47uF
Vcco_0 1x4.7uF
Vcco_12 1x47uF, 2x4.7uF, 4x0.47uF
Vcco_13 1x47uF, 2x4.7uF, 4x0.47uF
Vcco_14 1x47uF, 2x4.7uF, 4x0.47uF
Vcco_15 1x47uF, 2x4.7uF, 4x0.47uF
Vcco_16 1x47uF, 2x4.7uF, 4x0.47uF
Vcco_33 1x47uF, 2x4.7uF, 4x0.47uF
Vcco_34 1x47uF, 2x4.7uF, 4x0.47uF
Vcco_35 1x47uF, 2x4.7uF, 4x0.47uF
Bypass Cap Requirements from ug482-table_5-6_5-8:
MGTavcc 1x4.7uF, 2x0.1uF
MGTavtt 1x4.7uF, 2x0.1uF
Bypass Cap Requirements from ug480:
Two 0.22 0201 Ceramic Caps are substituted for each Xilinx recommended 0.47 0402 Ceramic Caps, per Avnet practice.
Title: 0301-MMFE-8_Power3
Size: C
Engineer: William Hart
Revision: A
Date: 6/17/2014
Time: 2:17:02 PM
Sheet 13 of 24
File: C:\Pjcts\AlhProj\0301-MMFE 8\0301-MMFE 8-6-17-14\0301-MMFE 8-Drivers-Power3.SchDoc
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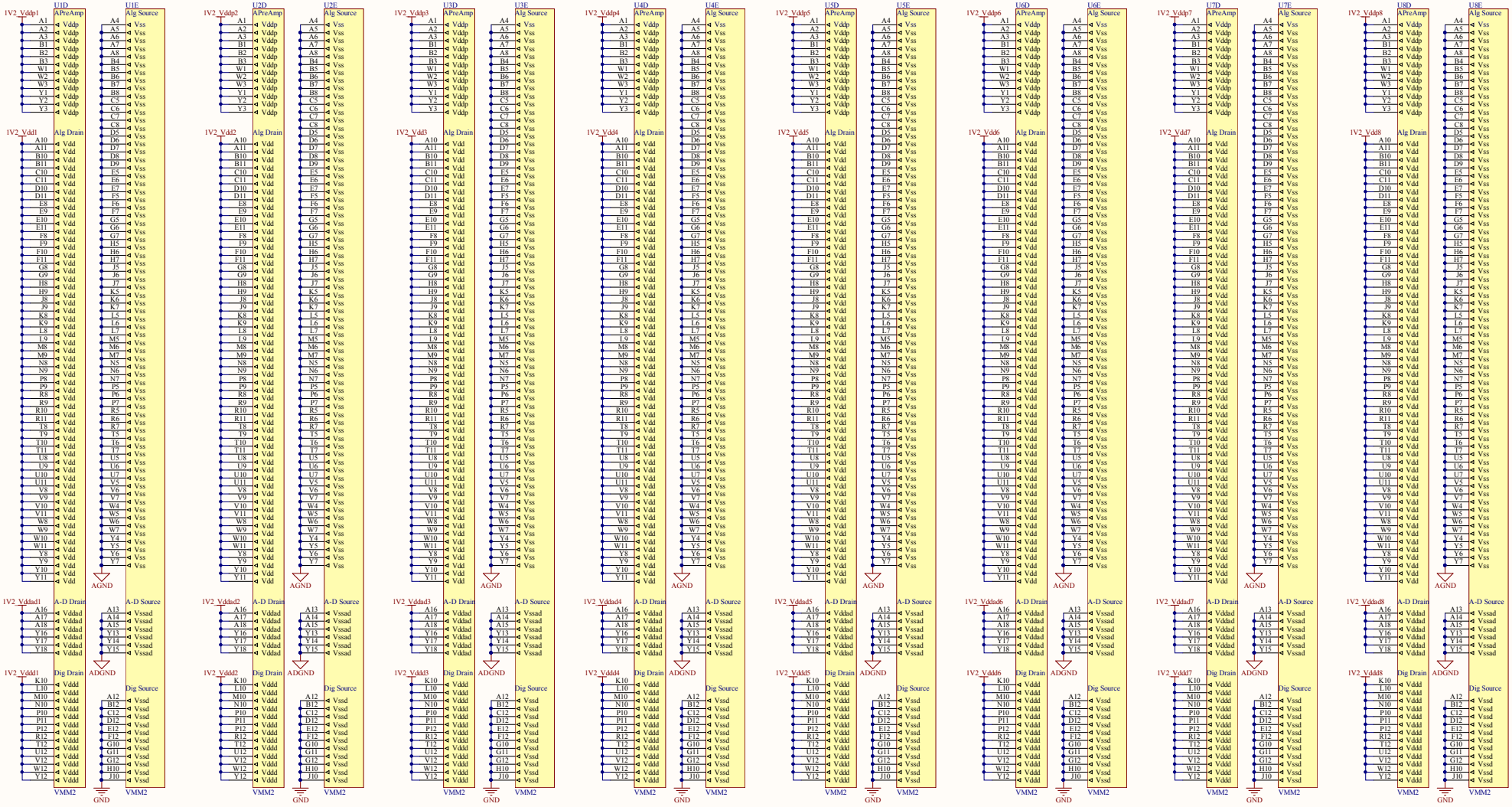
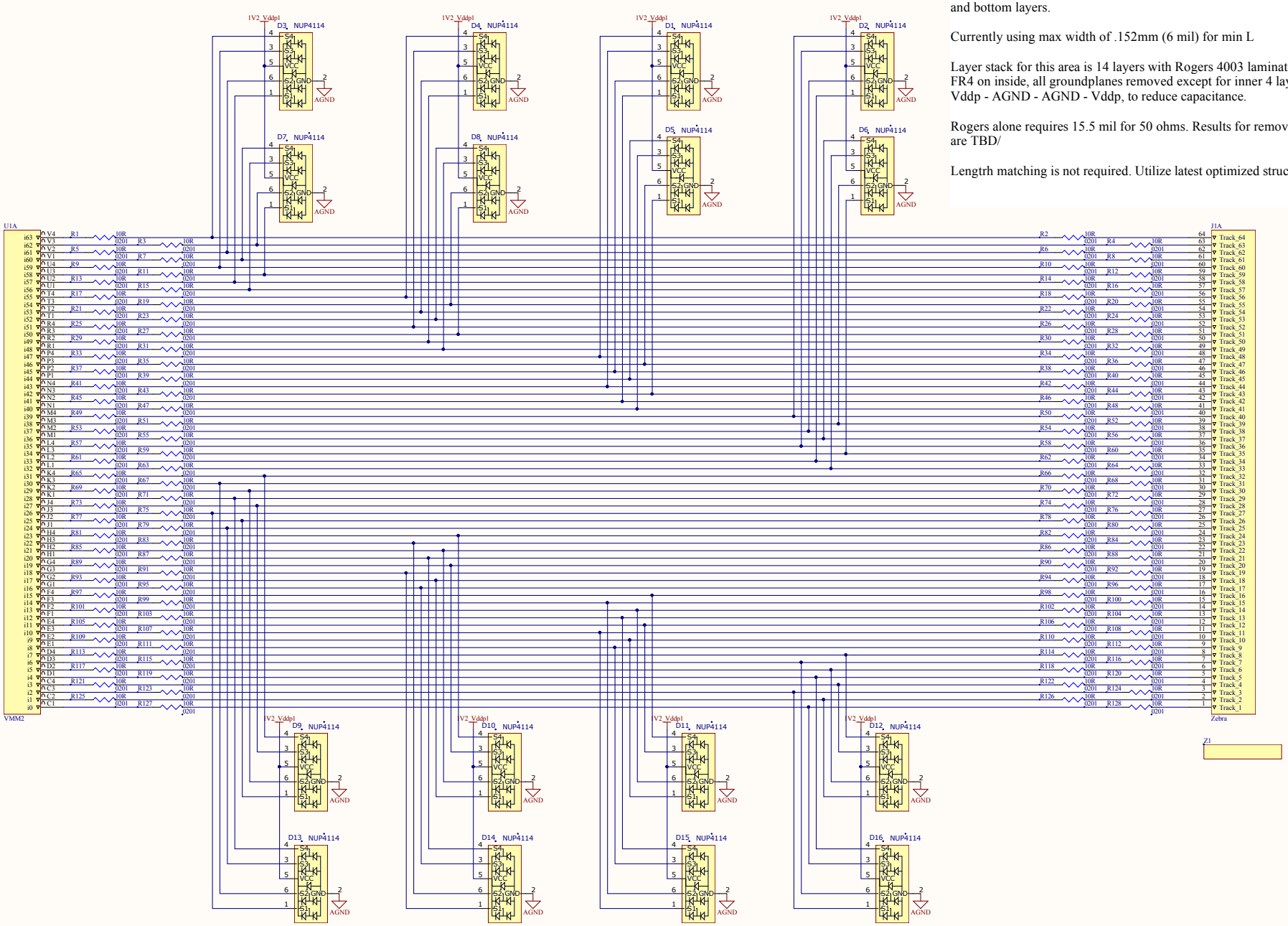
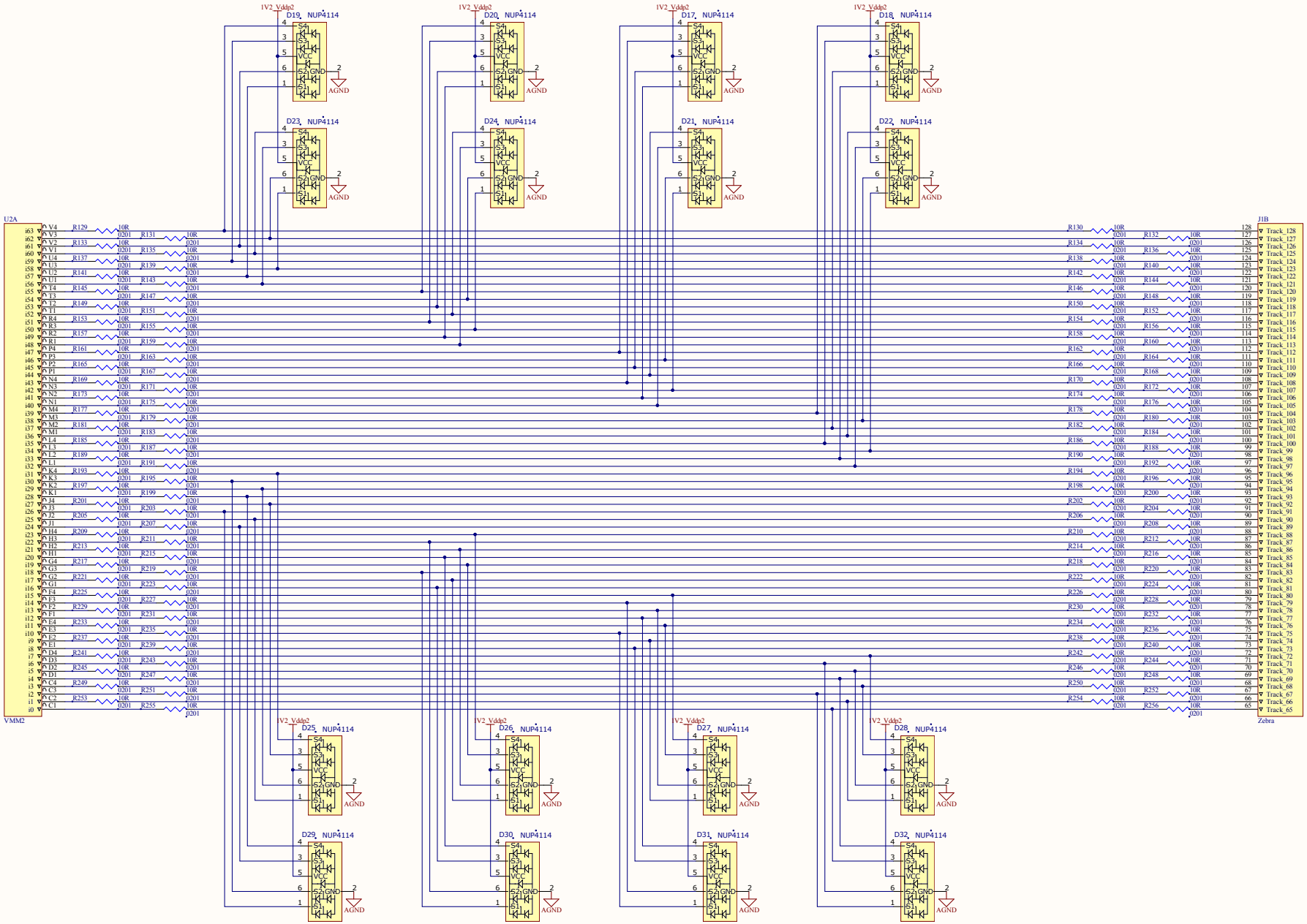
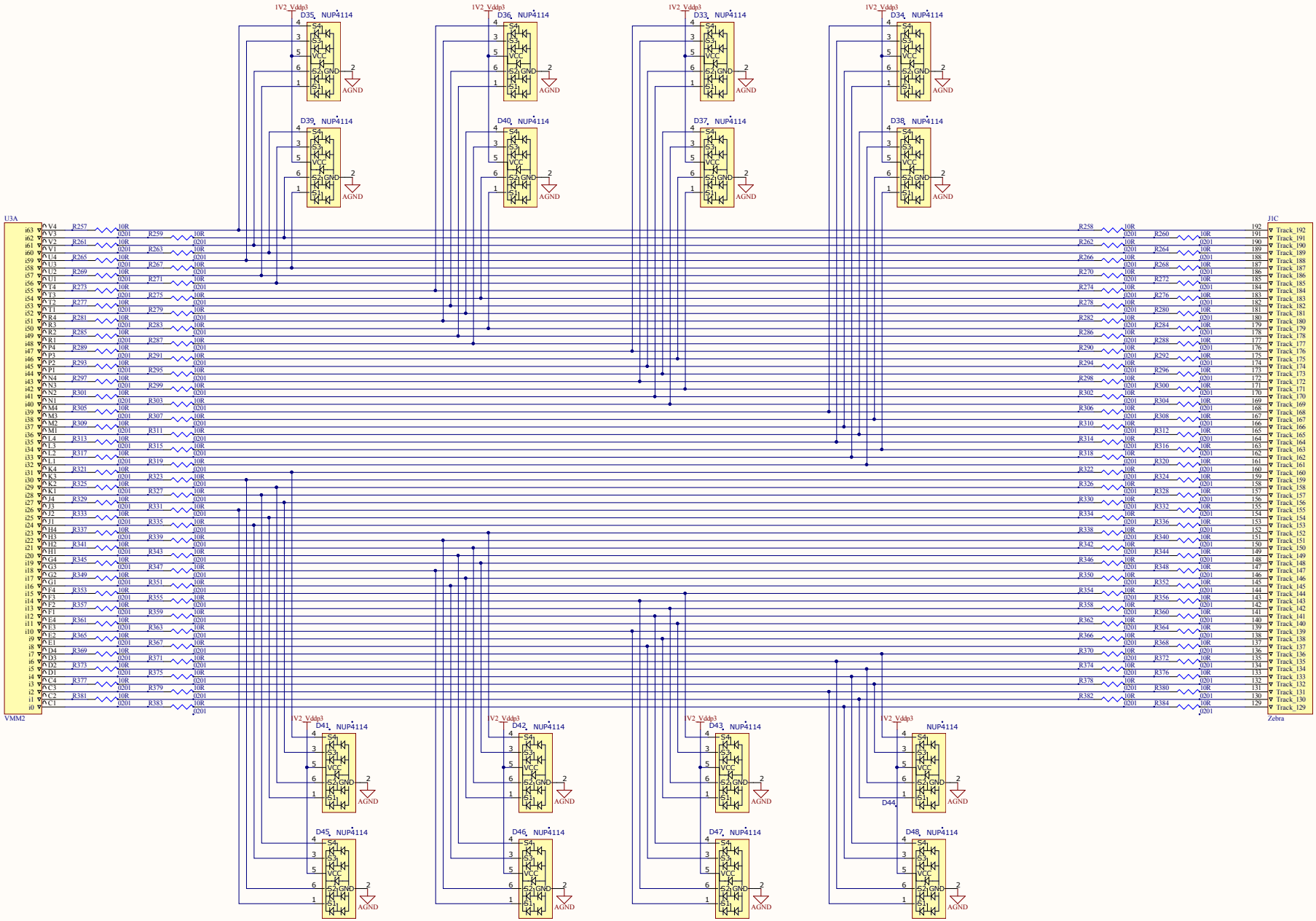


Title: 0301-MMFE-8_Power4			University of Arizona 1118 E 4th St Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 6/17/2014	Time: 2:17:02 PM	Sheet 14 of 24	
File: C:\Pjcts\AltProj\0301-MMFE_8\0301-MMFE_8-6-17-14\0301-MMFE_8-Power4.SchDoc		Drawn By: William Hart	

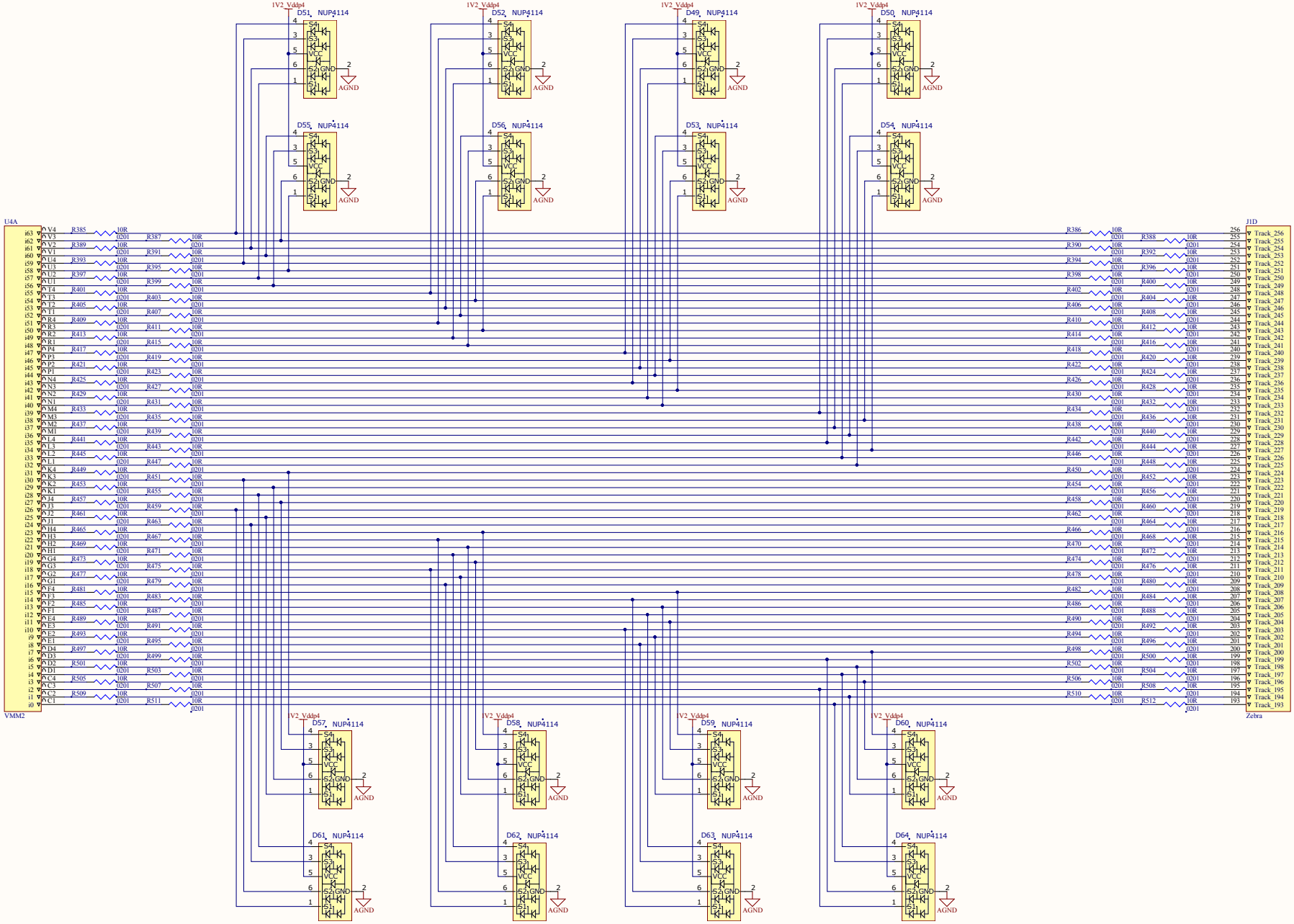

Analog Input Routing:
Traces from input connectors (Zaxis, Zebra, etc) are routed alternately to top and bottom layers.
Currently using max width of .152mm (6 mil) for min L
Layer stack for this area is 14 layers with Rogers 4003 laminate on outside, FR4 on inside, all groundplanes removed except for inner 4 layes which are Vddp - AGND - AGND - Vddp, to reduce capacitance.
Rogers alone requires 15.5 mil for 50 ohms. Results for removed ground layers are TBD/
Lengtrh matching is not required. Utilize latest optimized structures.
U1A
VMM2
J1A
Zebra
Z1
1V2_Vddp1
V2_Vddp1
D1 NUP4114
D2 NUP4114
D3 NUP4114
D4 NUP4114
D5 NUP4114
D6 NUP4114
D7 NUP4114
D8 NUP4114
D9 NUP4114
D10 NUP4114
D11 NUP4114
D12 NUP4114
D13 NUP4114
D14 NUP4114
D15 NUP4114
D16 NUP4114
AGND
Title: 0301-MMFE-8_Analog1
University of Arizona
1118 E 4th St
Tucson, Arizona 85721
billhart@email.arizona.edu
Size: C
Engineer: William Hart
Revision: A
Date: 6/17/2014
Time: 2:17:02 PM
Sheet 15 of 23
File: C:\Pjcts\AllProj\0301-MMFE 8\0301-MMFE 8-6-17-14\0301-MMFE 8-Analog1.SchDoc
Drawn by:



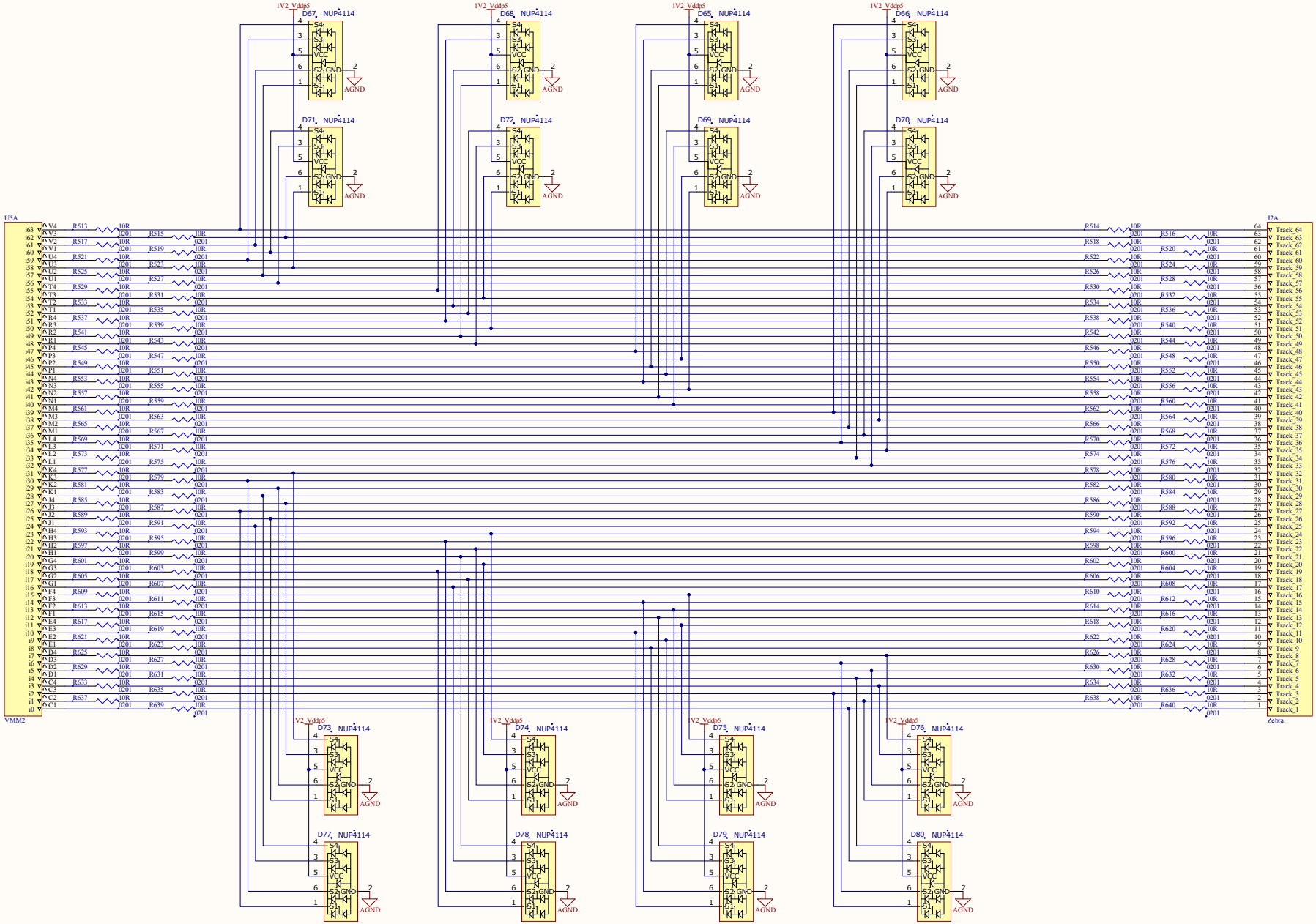
Title: 0301-MMFE-8_Analog2			University of Arizona 1118 E 4th St Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 6/17/2014	Time: 2:17:03 PM	Sheet 16 of 24	
File: C:\Pjcts\AltProj\0301-MMFE 8\0301-MMFE 8-6-17-14\0301-MMFE 8-Drivers by Analog2.SchDoc			



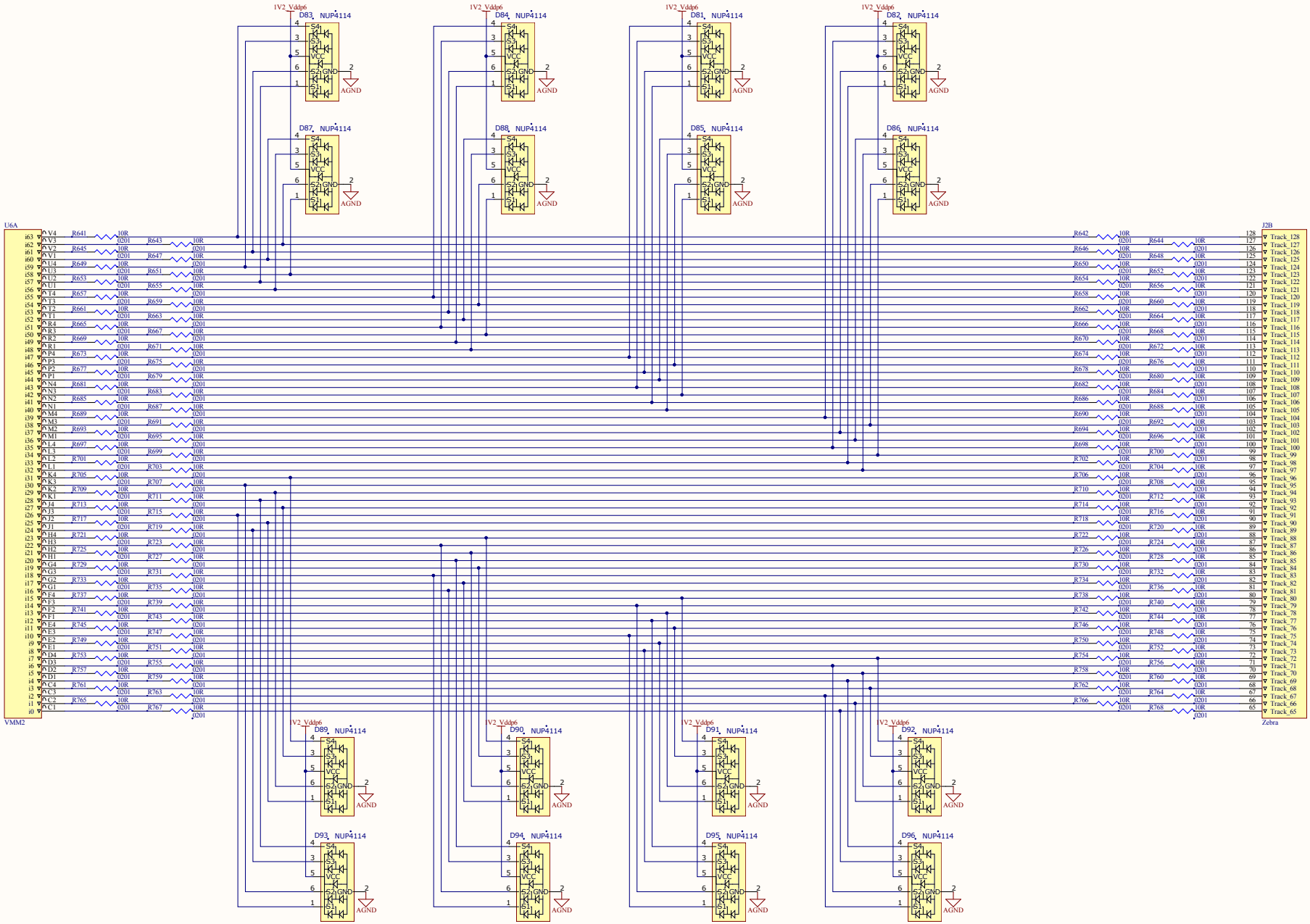
Title: 0301-MMFE-8_Analog3			University of Arizona 1118 E 4th St Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 6/17/2014	Time: 2:17:03 PM	Sheet 17 of 24	
File: C:\Pjcts\AllProj\0301-MMFE 8\0301-MMFE 8-6-17-14\0301-MMFE 8-Drivers by Analog.SchDoc			Drawn by: William Hart



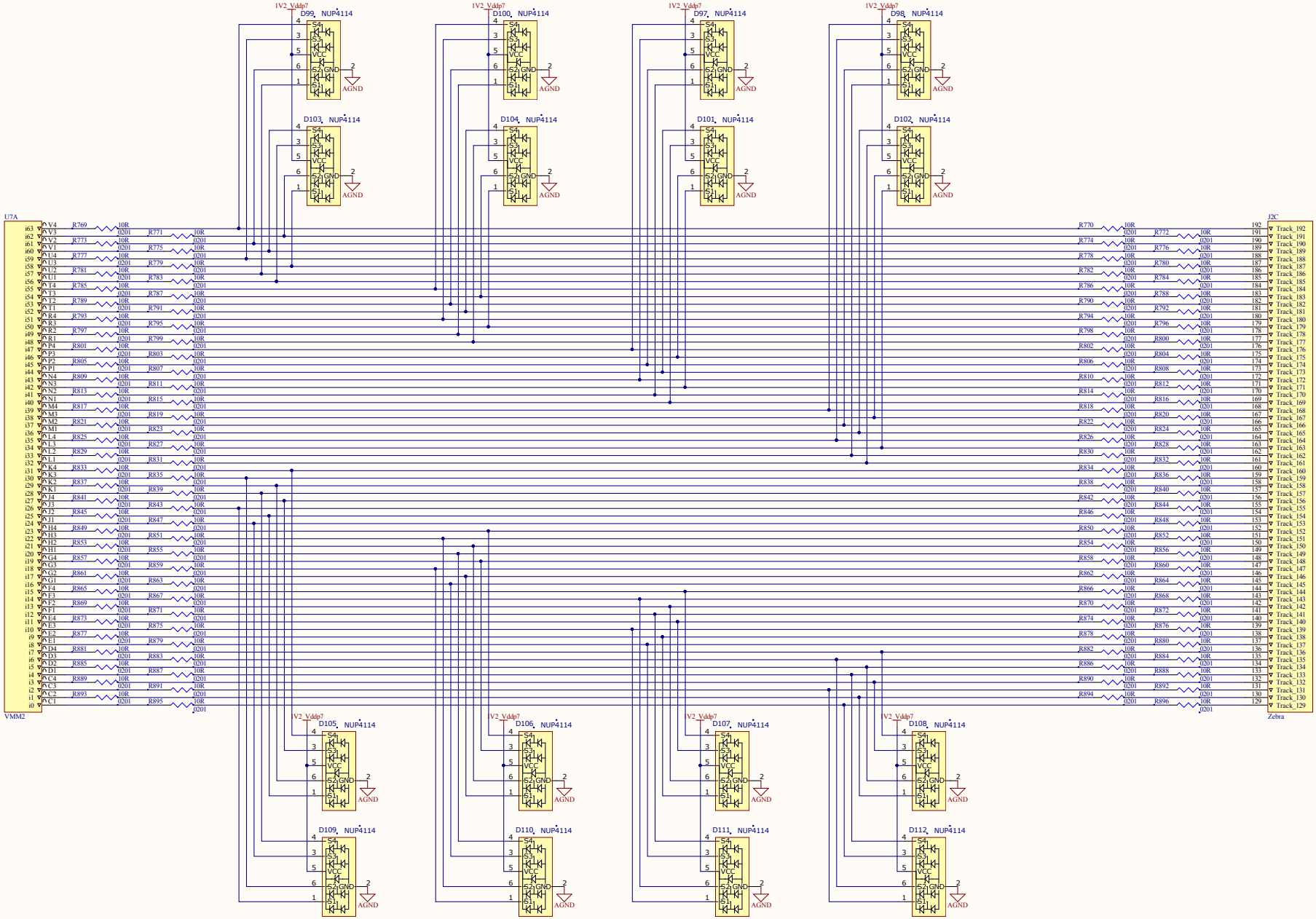
Title: 0301-MMFE-8_Analog4			University of Arizona 1118 E 4th St Tucson, Arizona 85721 billhart@email.arizona.edu
Size: C	Engineer: William Hart	Revision: A	
Date: 6/17/2014	Time: 2:17:03 PM	Sheet 18 of 24	
File: C:\Pjcts\AllProj\0301-MMFE 8\0301-MMFE 8-6-17-14\0301-MMFE 8-Analog4.SchDoc		Drawn by: William Hart	



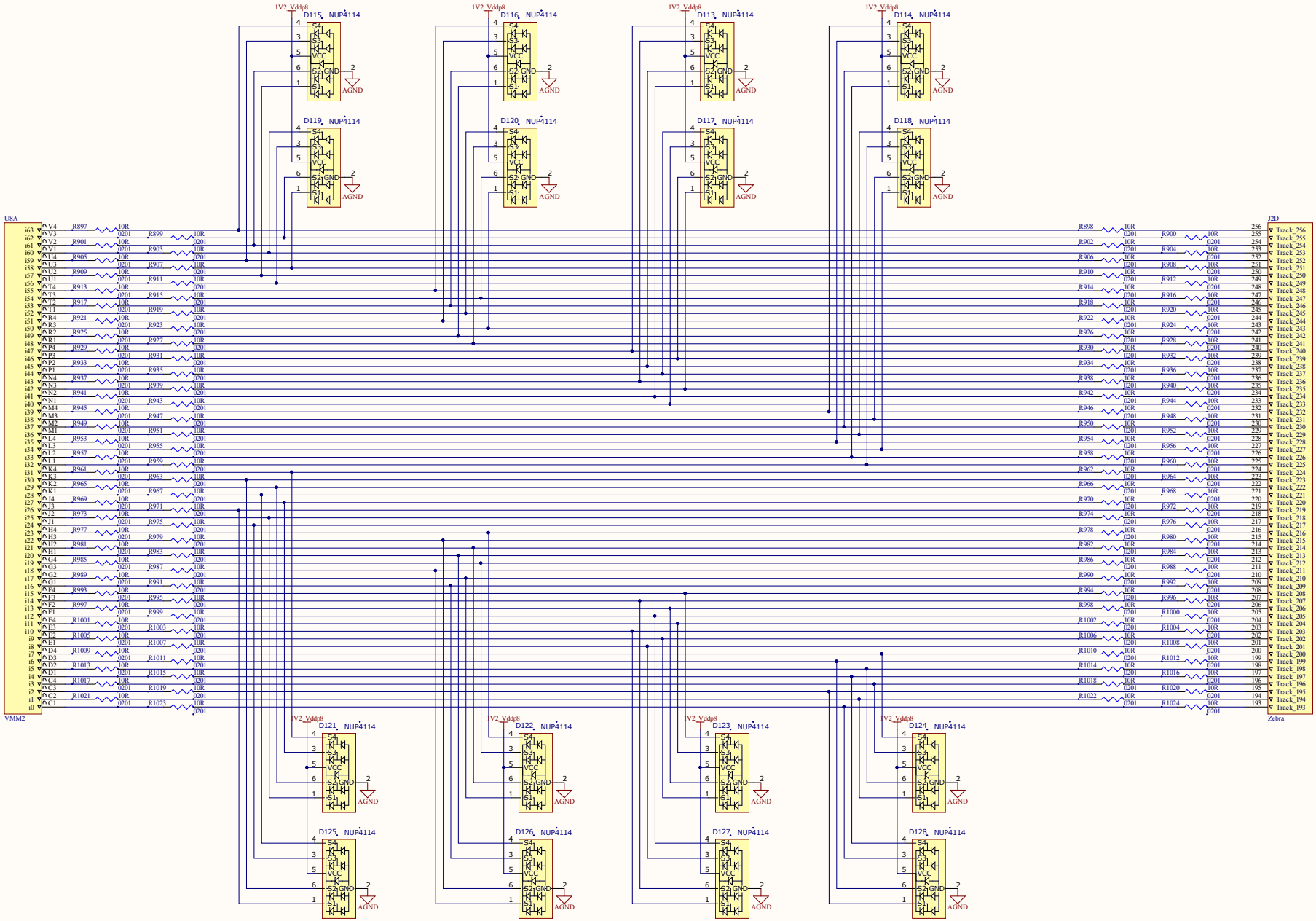
Title: 0301-MMFE-8_Analog5			University of Arizona 1118 E 4th St Tucson, Arizona 85721 billhart@email.arizona.edu
Size: C	Engineer: William Hart	Revision: A	
Date: 6/17/2014	Time: 2:17:04 PM	Sheet 19 of 24	
File: C:\Pjcts\AllProj\0301-MMFE 8\0301-MMFE 8-6-17-14\0301-MMFE 8-Analog5.SchDoc		Drawn by: William Hart	



Title: 0301-MMFE-8_Analog6			University of Arizona 1118 E 4th St Tucson, Arizona 85721 billhart@email.arizona.edu
Size: C	Engineer: William Hart	Revision: A	
Date: 6/17/2014	Time: 2:17:04 PM	Sheet 20 of 24	
File: C:\Pjcts\AllProj\0301-MMFE 8\0301-MMFE 8-6-17-14\0301-MMFE 8-Drivers by Analog.SchDoc			Drawn By:

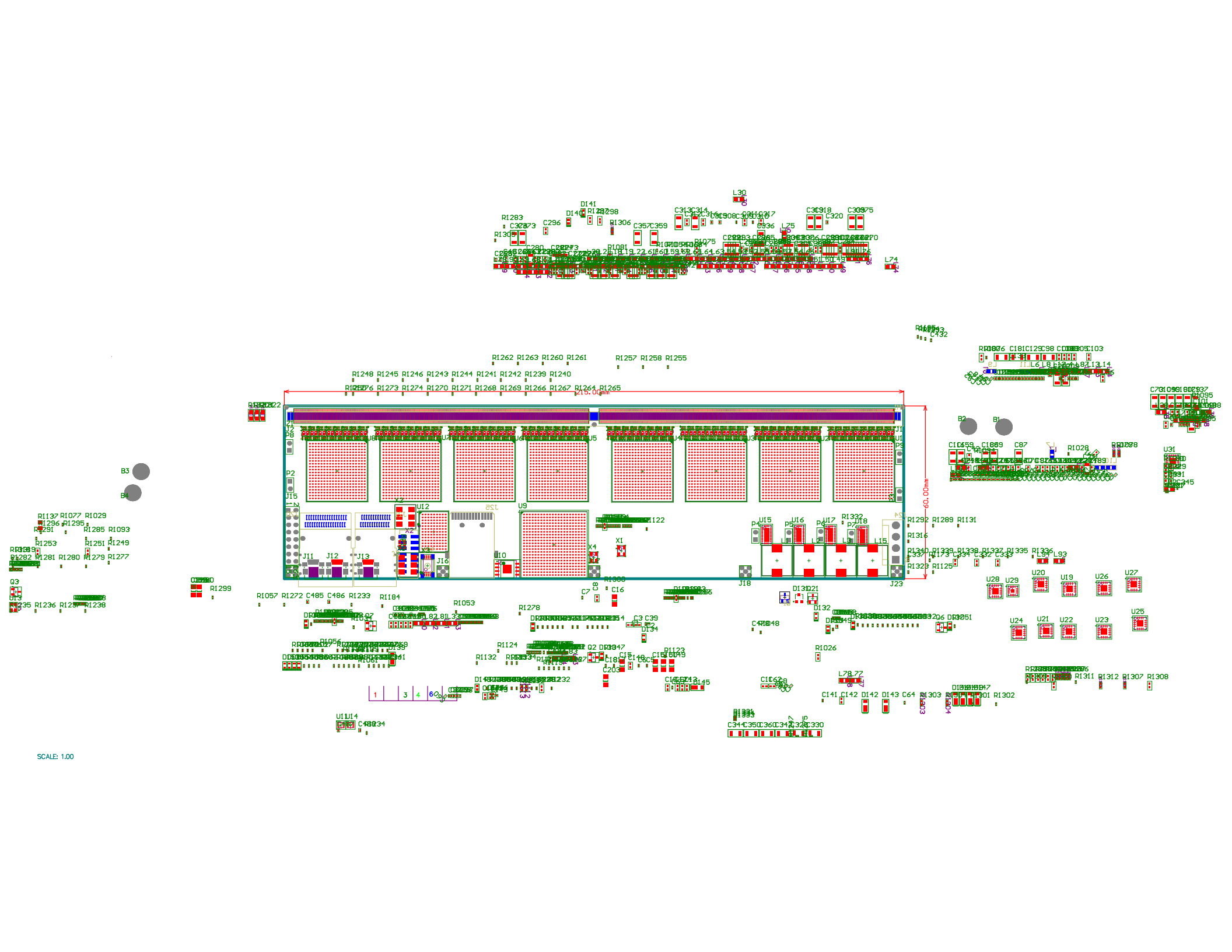


Title: 0301-MMFE-8_Analog7			University of Arizona 1118 E 4th St Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 6/17/2014	Time: 2:17:04 PM	Sheet 21 of 24	
File: C:\Pjcts\AllProj\0301-MMFE 8\0301-MMFE 8-6-17-14\0301-MMFE 8-Analog7.SchDoc			Drawn by: William Hart



Title: 0301-MMFE-8_Analog8			University of Arizona 1118 E 4th St Tucson, Arizona 85721 billhart@email.arizona.edu
Size: C	Engineer: William Hart	Revision: A	
Date: 6/17/2014	Time: 2:17:05 PM	Sheet 22 of 24	
File: C:\Pjcts\AllProj\0301-MMFE 8\0301-MMFE 8-6-17-14\0301-MMFE 8-Analog8.SchDoc		Drawn By: William Hart	

Title: 0301-MMFE-8_VMM_tp			University of Arizona 1118 E 4th St Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 6/17/2014	Time: 2:17:05 PM	Sheet 23 of 24	
File: C:\Pjcts\AlProj\0301-MMFE_8\0301-MMFE_8-6-17-14\0301-MMFE_8-VMM_tp.SchDoc		Drawn by: William Hart	


215.00mm
60.00mm
SCALE: 1.00