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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Sheet 1 - Contents

Sheet 2 - Block Diagram

Sheet 3 - Ethernet Main

Sheet 4 - Ethernet Extras

Sheet 5 - USB

Sheet 6 - DDR

Sheet 7 - Flash

Sheet 8 - Clocks

Sheet 9 - Analog Interfaces

Sheet 10 - ADCs

Sheet 11 - DACS for Board 1

Sheet 12 - DACS for Board 2

Sheet 13 - Connections to TPC 1

Sheet 14 - Connections to TPC 2

Sheet 15 - Connections to FEC

Sheet 16 - FEC Grounds

Sheet 17 - Microcontroller

Sheet 18 - MicroController Power

Sheet 19 - Test Points and LEDs

Sheet 20 - Programming

Sheet 21 - Power Supplies

Sheet 22 - Power Supplies 2

Sheet 23 - Decoupling for FPGA

COMPANY: University of Arizona

TITLE: C-Card Schematic

DRAWN: J. Steinberg	DATED: 6/14/2010
CHECKED: <Checked By>	DATED: <Checked Date>
QUALITY CONTROL: <QC By>	DATED: <QC Date>
RELEASED: <Released By>	DATED: <Release Date>

CODE:	SIZE:	DRAWING NO:	REV:
<Code>	C	PCB-0220-BD	A

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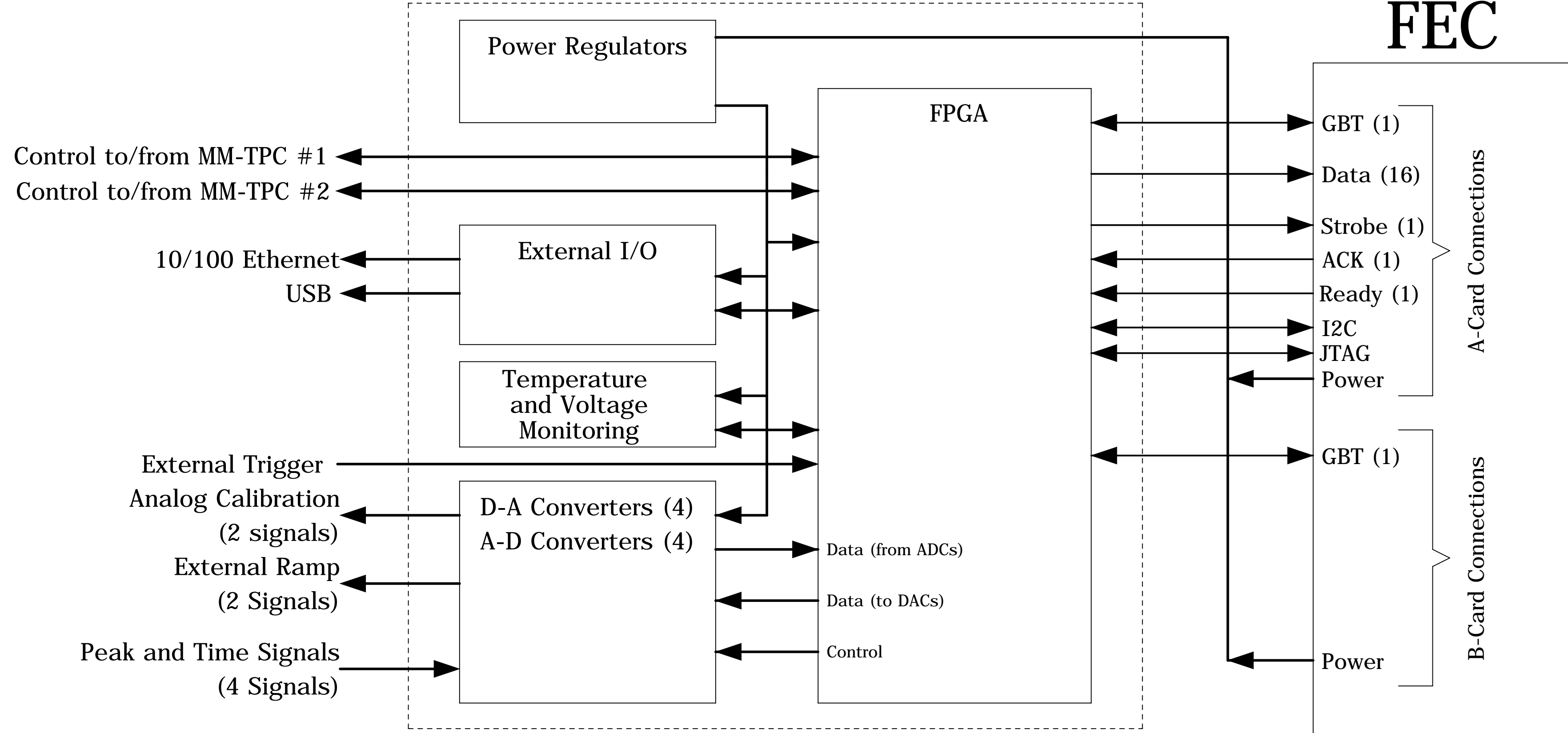
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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

# C-Card

# FEC



COMPANY: **University of Arizona**

TITLE: **C-Card Schematic Block Diagram**

DRAWN: J. Steinberg	DATED: 6/14/2010
CHECKED: <Checked By>	DATED: <Checked Date>
QUALITY CONTROL: <QC By>	DATED: <QC Date>
RELEASED: <Released By>	DATED: <Release Date>

CODE:	SIZE: <b>C</b>	DRAWING NO: <b>PCB-0220-BD</b>	REV: <b>A</b>
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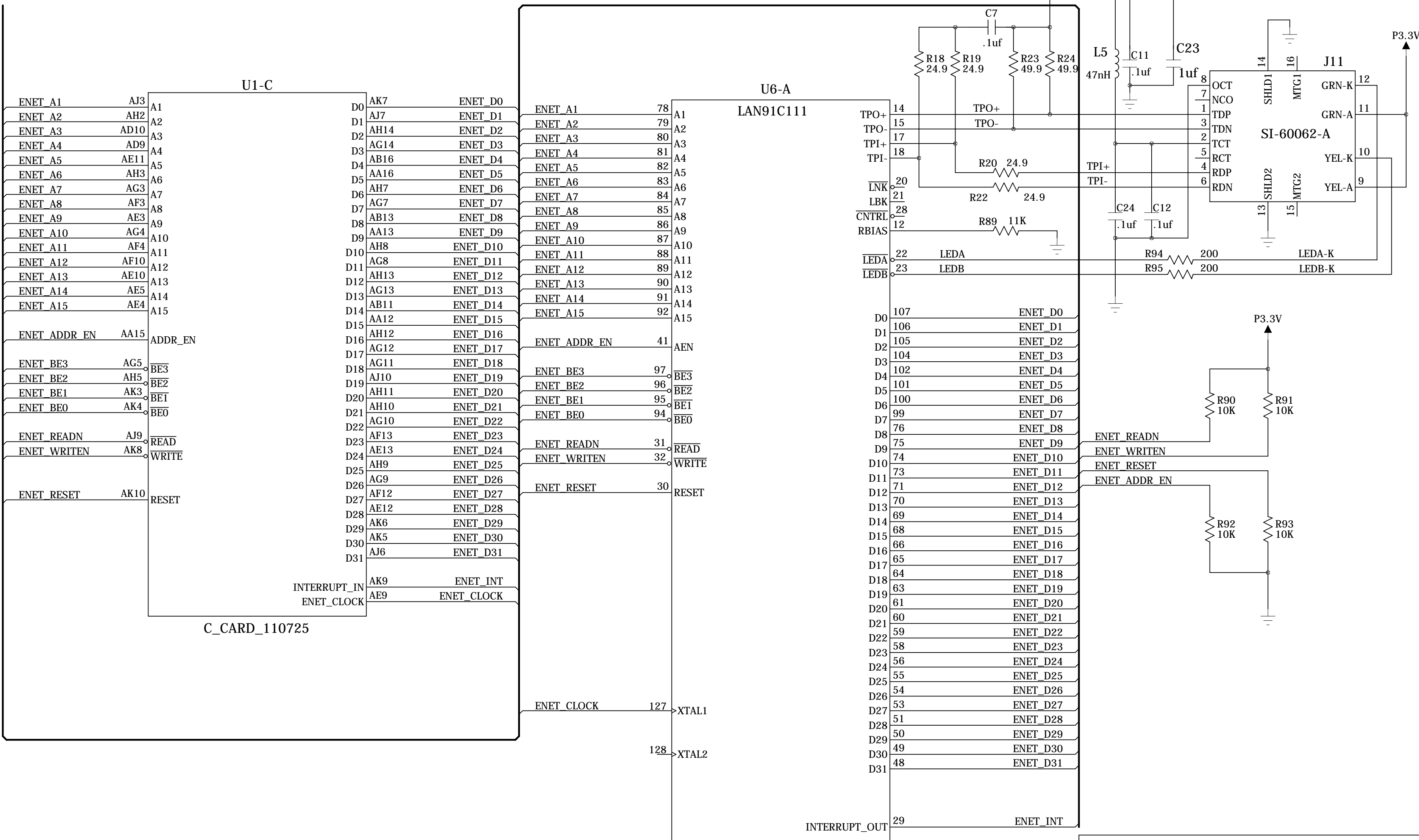
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COMPANY: University of Arizona			
TITLE: C-Card Schematic Ethernet Interface			
DRAWN: J. Steinberg	DATED: 6/14/2010	CODE: <Code>	SIZE: C
CHECKED: <Checked By>	DATED: <Checked Date>	DRAWING NO: PCB-0220-BD	REV: A
QUALITY CONTROL: <QC By>	DATED: <QC Date>	SHEET: 3 of 26	
RELEASED: <Released By>	DATED: <Release Date>		

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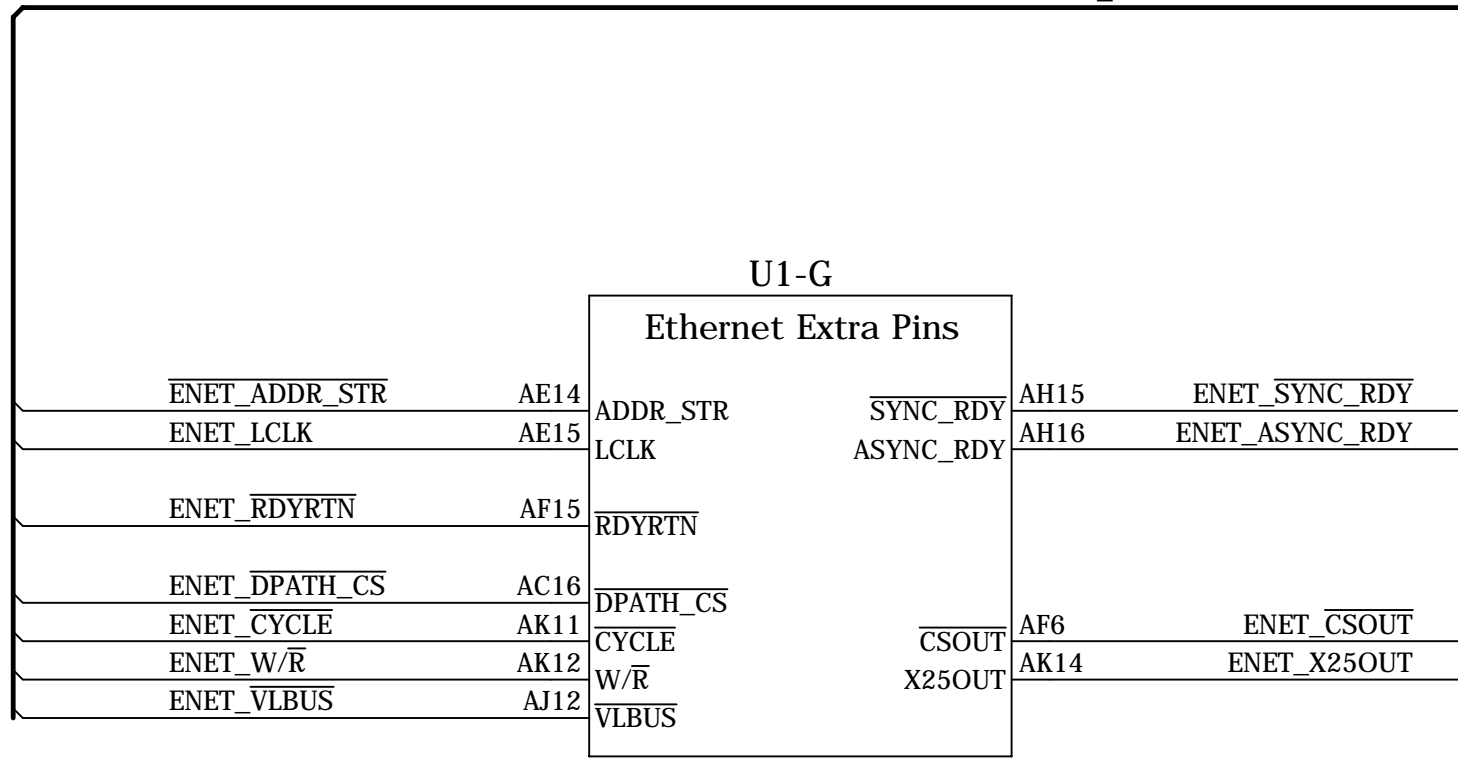
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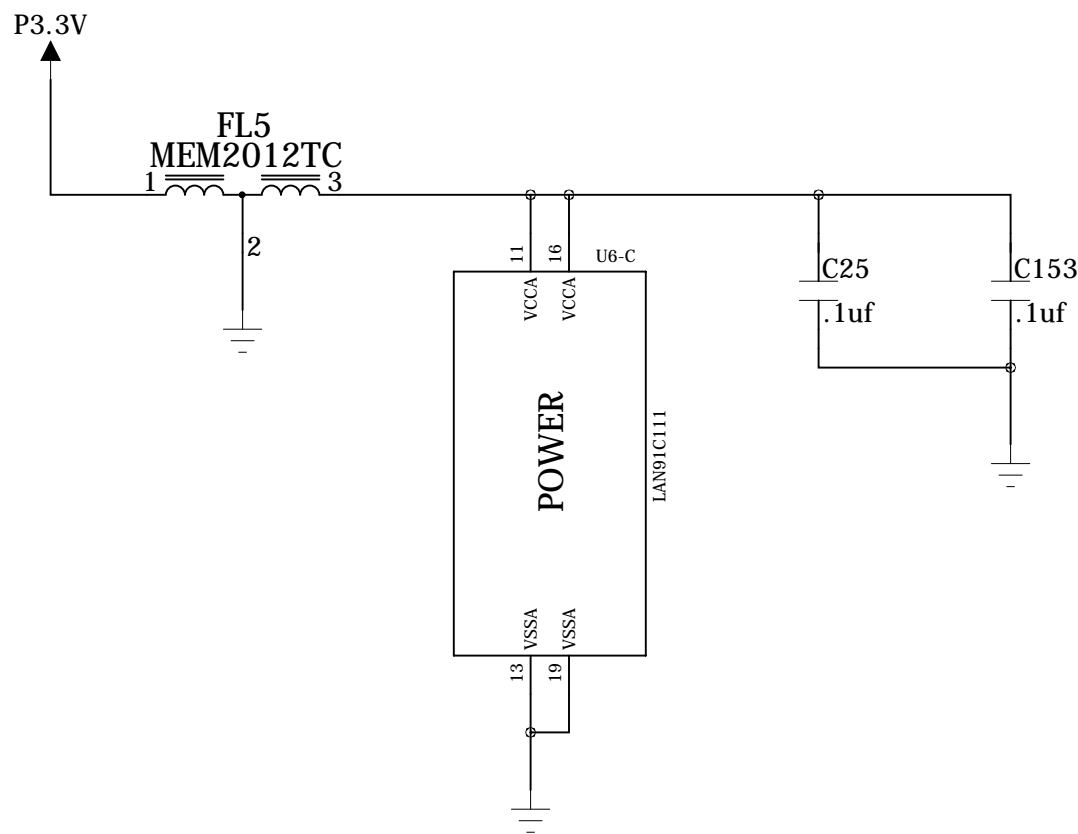
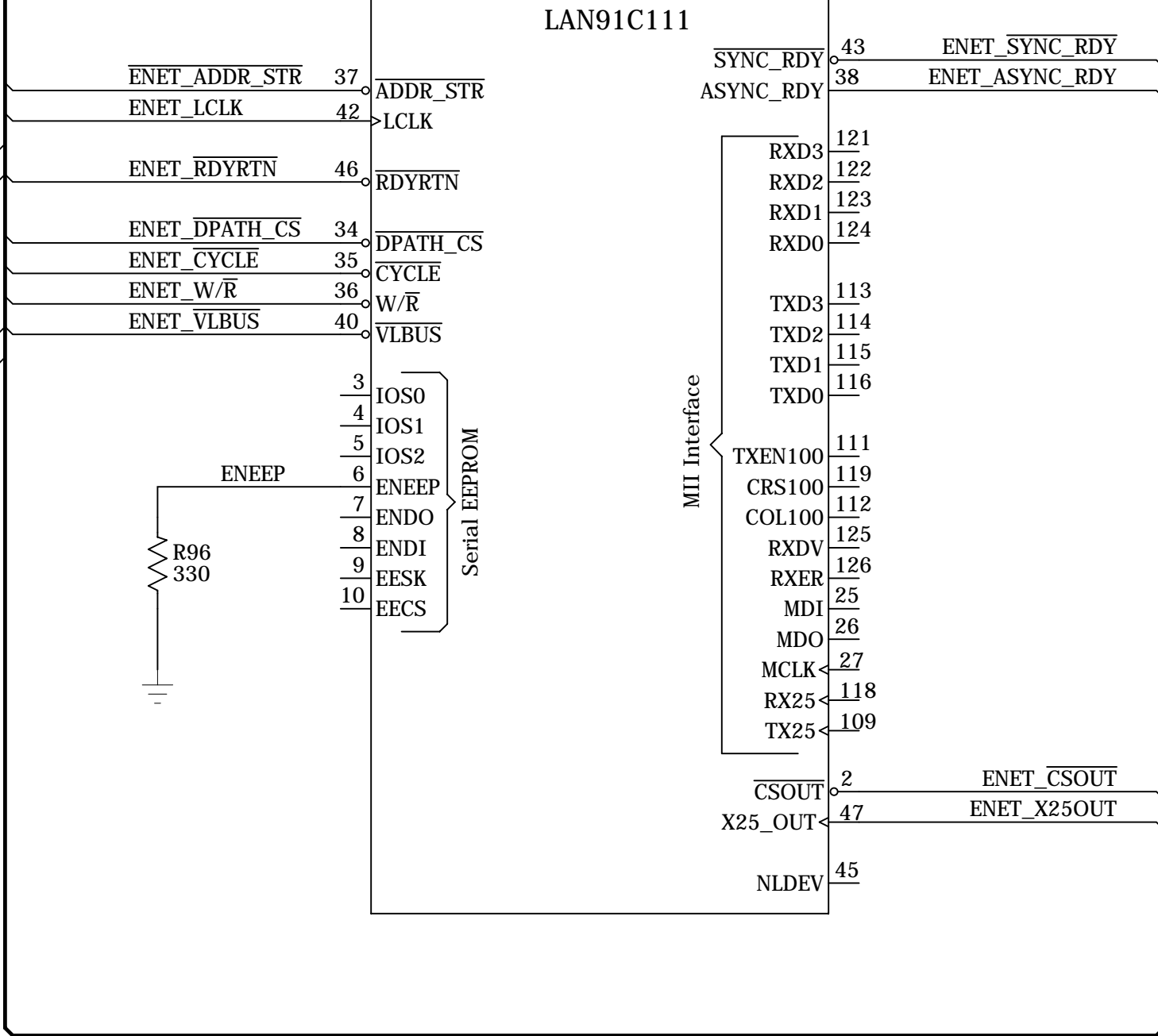
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LTR	ECO NO:	APPROVED:	DATE:

ETHERNET\_EXTRAS



C\_CARD\_110725

U6-B



COMPANY: University of Arizona

TITLE: C-Card Schematic

DRAWN: J. Steinberg	DATED: 6/14/2010
CHECKED: <Checked By>	DATED: <Checked Date>
QUALITY CONTROL: <QC By>	DATED: <QC Date>
RELEASED: <Released By>	DATED: <Release Date>

CODE: <Code>	SIZE: C	DRAWING NO: PCB-0220-BD	REV: A
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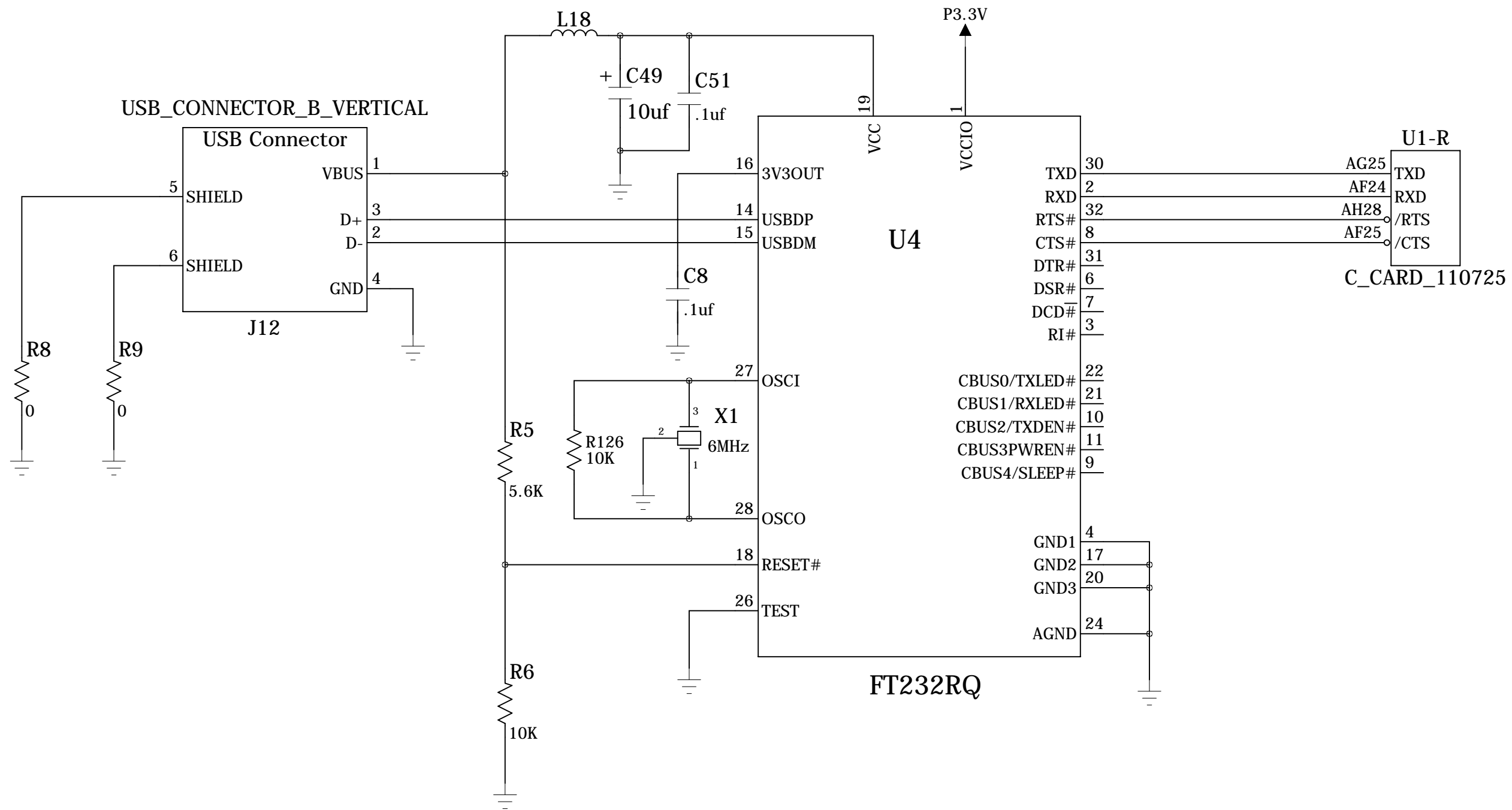
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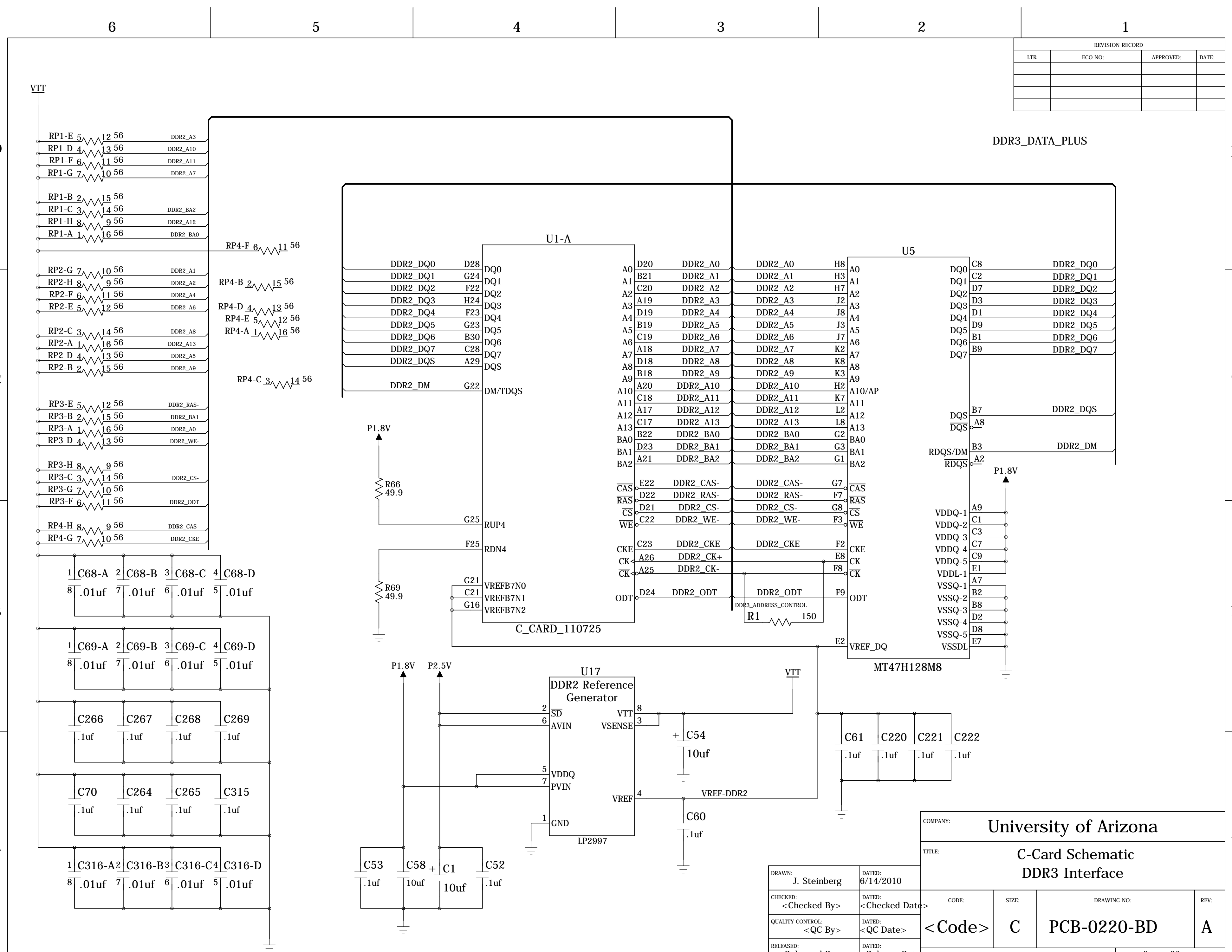
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LTR	ECO NO:	APPROVED:	DATE:



COMPANY:				University of Arizona			
TITLE:				C-Card Schematic			
DRAWN:	J. Steinberg	DATED:	6/14/2010	CODE:	SIZE:	DRAWING NO:	REV:
CHECKED:	<Checked By>	DATED:	<Checked Date>	<Code>	C	PCB-0220-BD	A
QUALITY CONTROL:	<QC By>	DATED:	<QC Date>				
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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



COMPANY: University of Arizona			
TITLE: C-Card Schematic DDR3 Interface			
DRAWN: J. Steinberg	DATED: 6/14/2010	CODE:	SIZE:
CHECKED: <Checked By>	DATED: <Checked Date>	<Code>	C
QUALITY CONTROL: <QC By>	DATED: <QC Date>	DRAWING NO: PCB-0220-BD	
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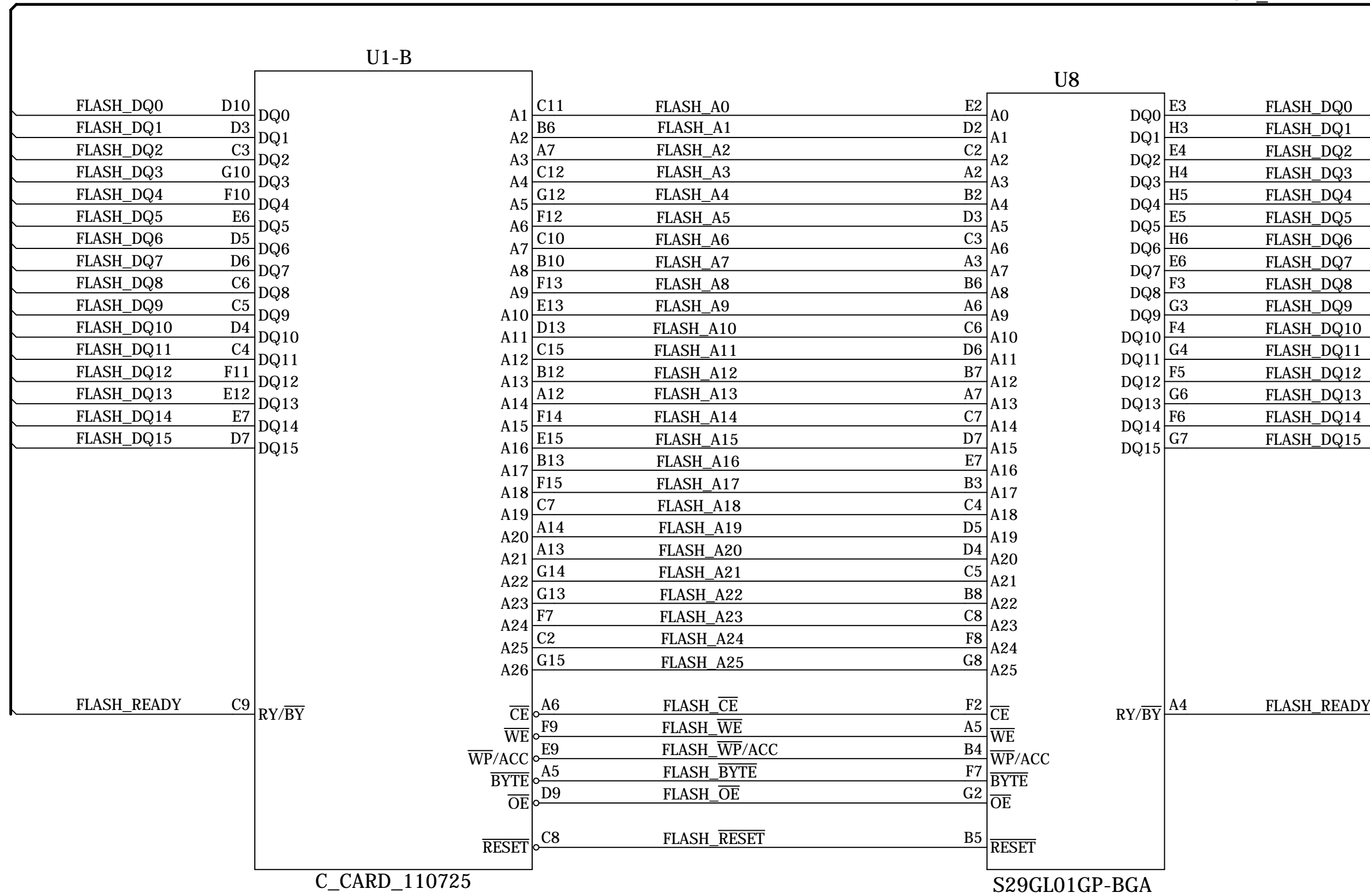
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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

FLASH DATA



COMPANY: University of Arizona			
TITLE: C-Card Schematic Flash Interface			
DRAWN: J. Steinberg	DATED: 6/14/2010	CODE:	REV: A
CHECKED: <Checked By>	DATED: <Checked Date>	SIZE: C	DRAWING NO: PCB-0220-BD
QUALITY CONTROL: <QC By>	DATED: <QC Date>	SHEET: 7 of 26	
RELEASED: <Released By>	DATED: <Release Date>		

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REVISION RECORD

LTR	ECO NO:	APPROVED:	DATE:

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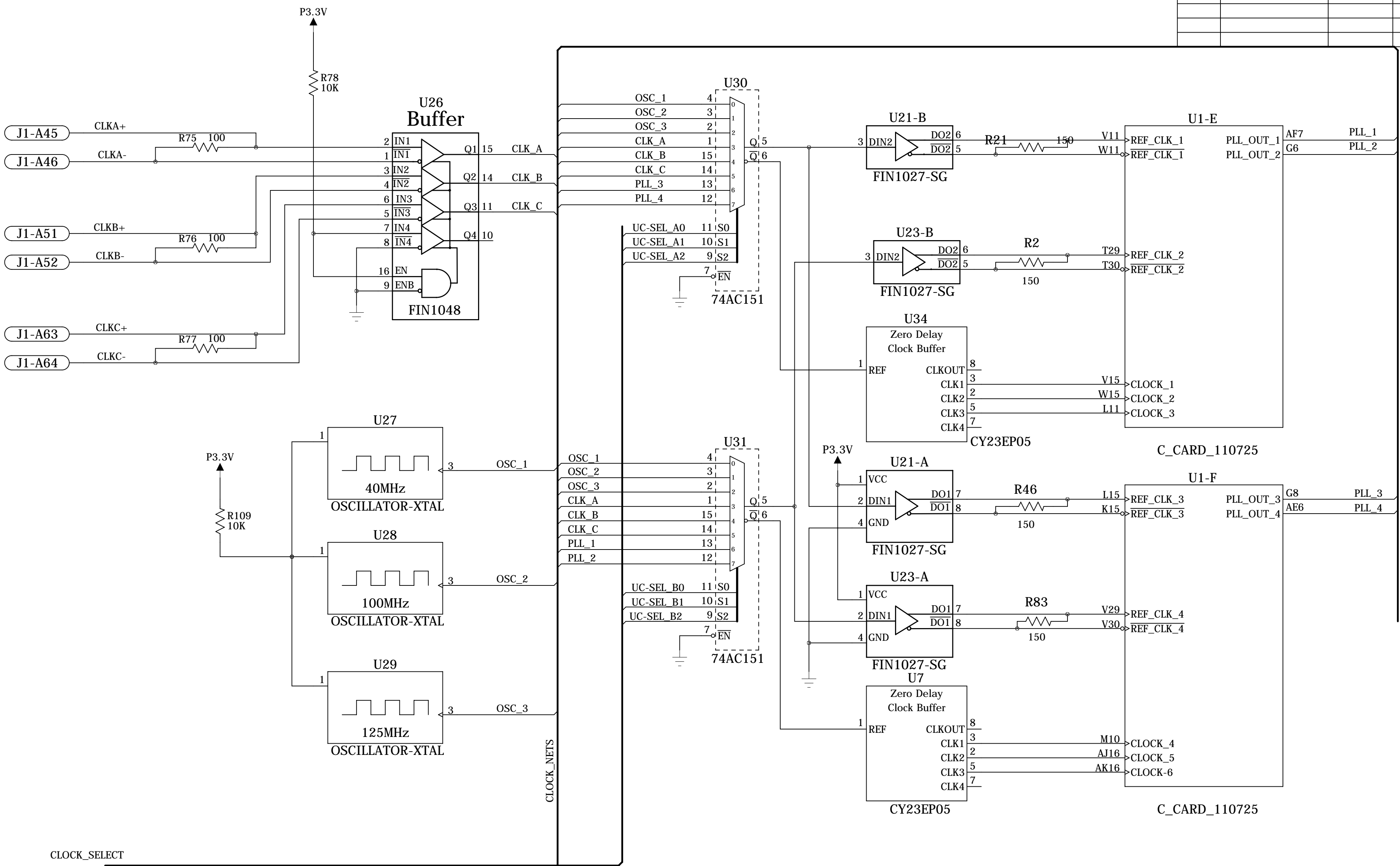
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COMPANY: University of Arizona			
TITLE: C-Card Schematic Clocks			
DRAWN: J. Steinberg	DATED: 6/14/2010	CODE: <Code>	SIZE: C
CHECKED: <Checked By>	DATED: <Checked Date>	DRAWING NO: PCB-0220-BD	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	REV: A	
RELEASED: <Released By>	DATED: <Release Date>	SHEET: 8 of 26	



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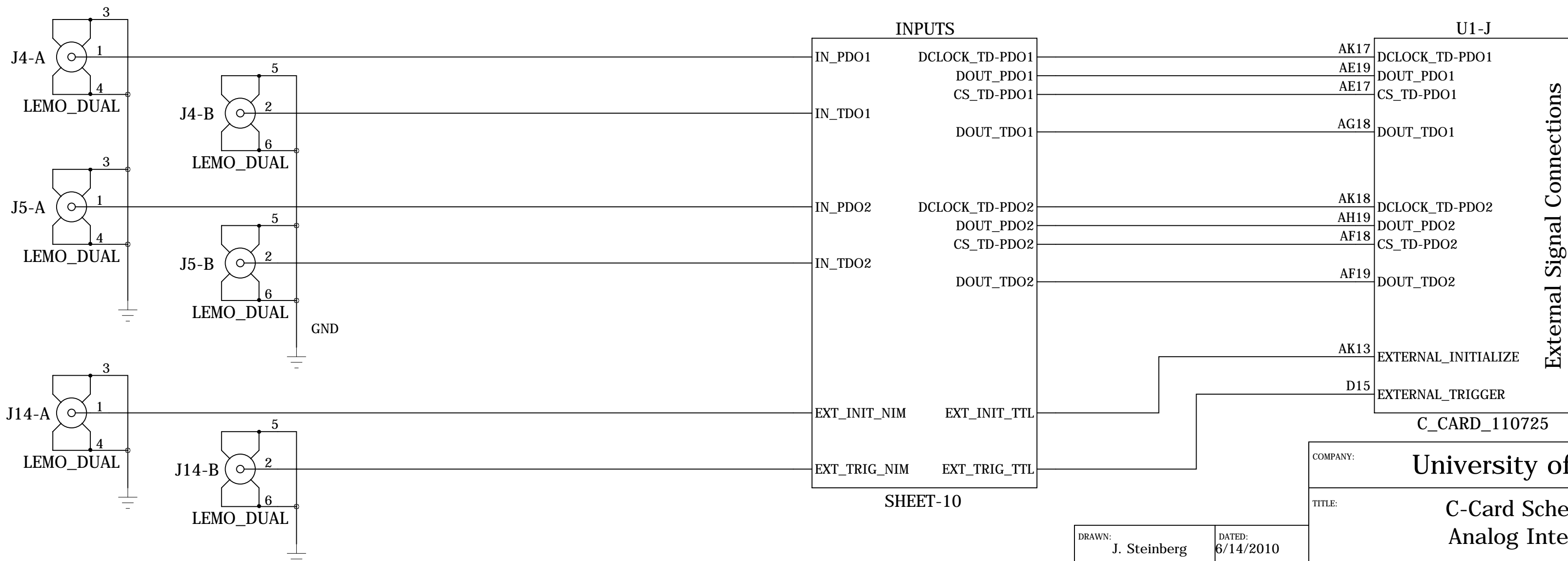
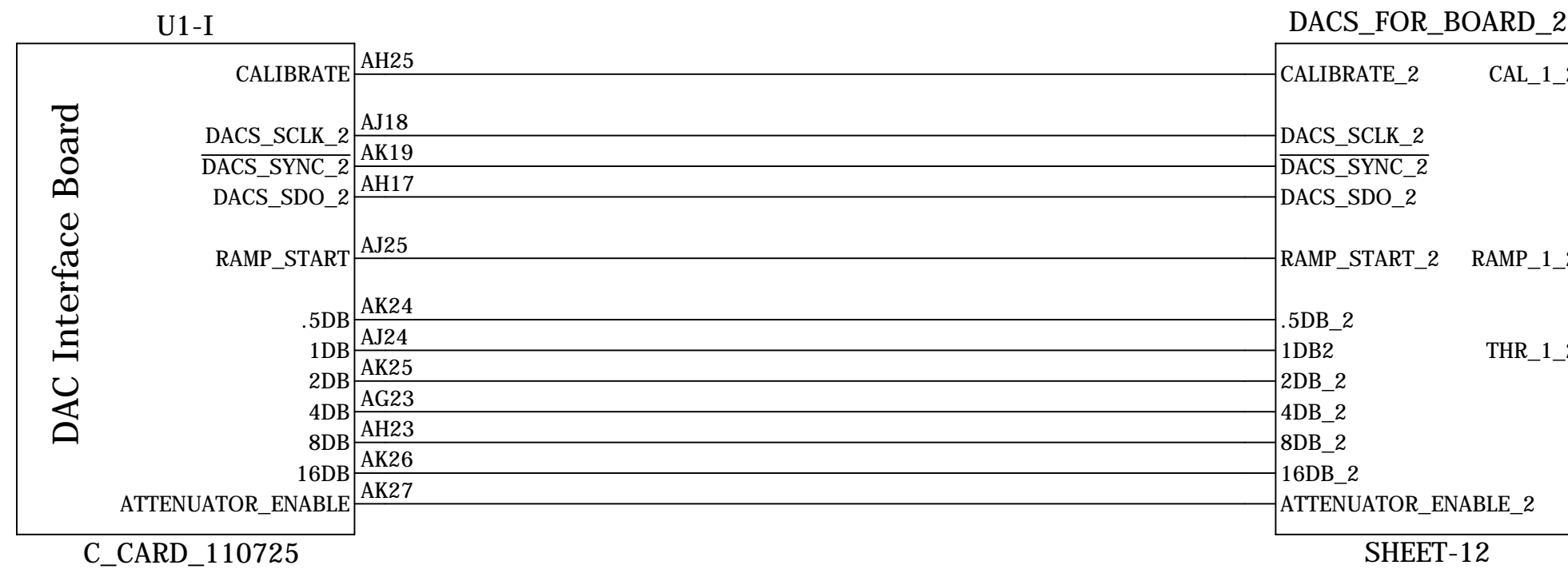
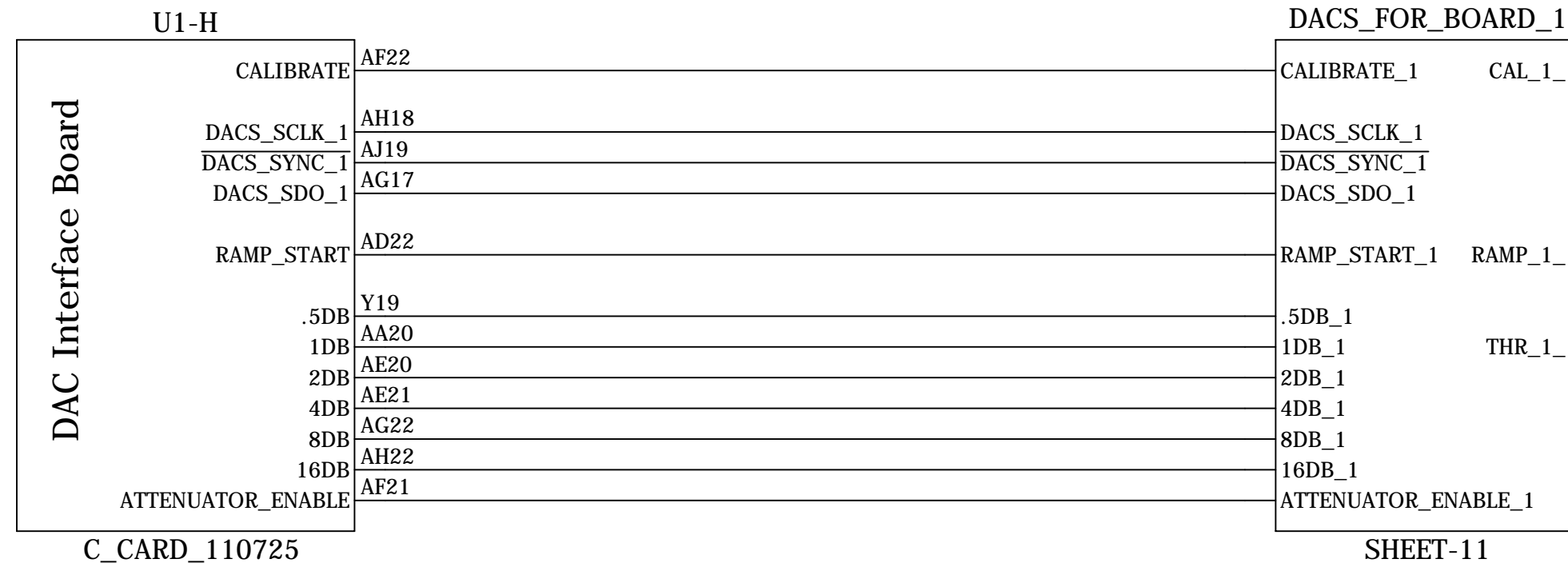
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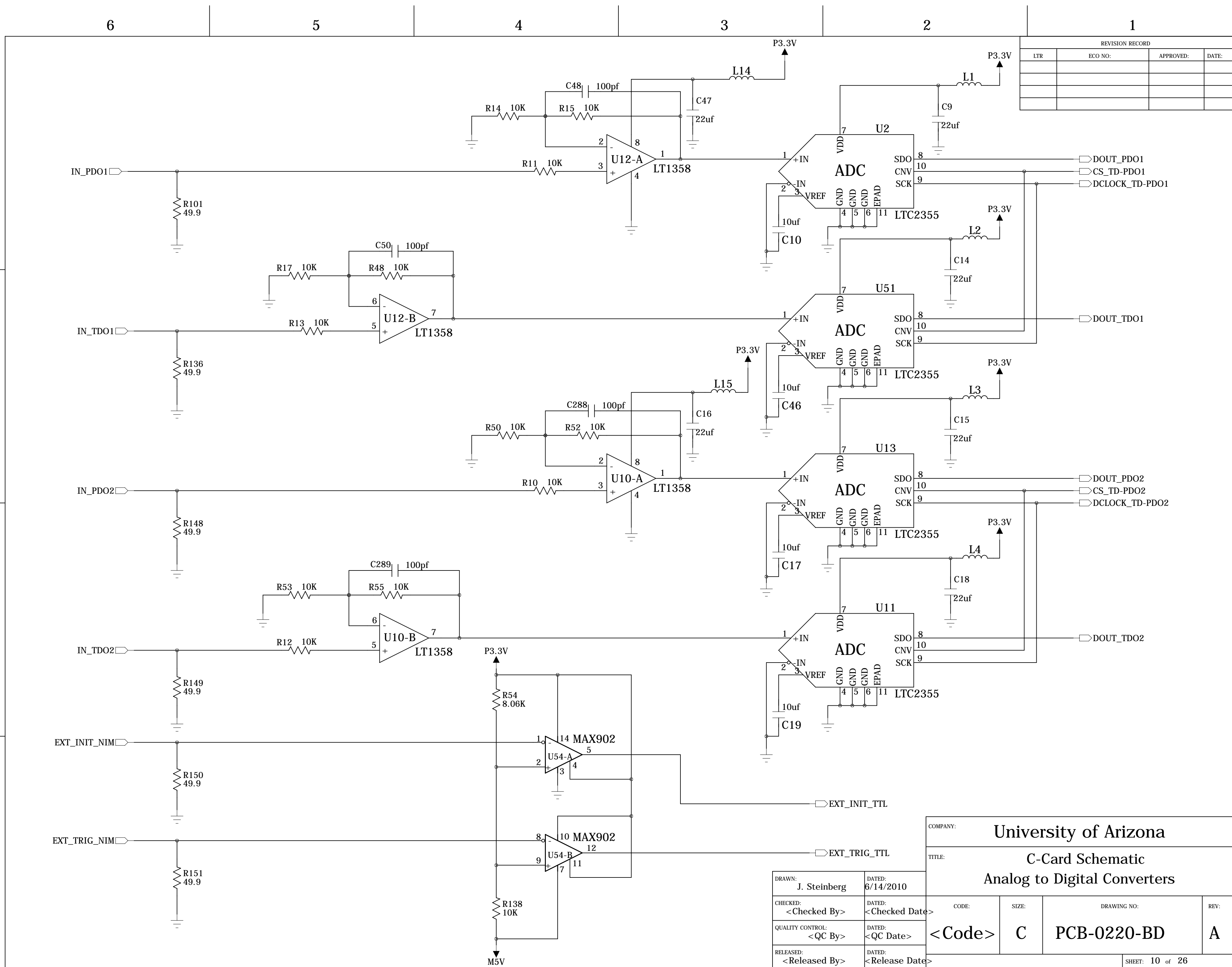
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COMPANY: <b>University of Arizona</b>			
TITLE: <b>C-Card Schematic Analog Interface</b>			
CODE: <b>&lt;Code&gt;</b>	SIZE: <b>C</b>	DRAWING NO: <b>PCB-0220-BD</b>	REV: <b>A</b>

DRAWN: <b>J. Steinberg</b>	DATED: <b>6/14/2010</b>
CHECKED: <b>&lt;Checked By&gt;</b>	DATED: <b>&lt;Checked Date&gt;</b>
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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

COMPANY: **University of Arizona**

TITLE: **C-Card Schematic  
Analog to Digital Converters**

DRAWN: J. Steinberg	DATED: 6/14/2010
CHECKED: <Checked By>	DATED: <Checked Date>
QUALITY CONTROL: <QC By>	DATED: <QC Date>
RELEASED: <Released By>	DATED: <Release Date>

CODE: <b>&lt;Code&gt;</b>	SIZE: <b>C</b>	DRAWING NO: <b>PCB-0220-BD</b>	REV: <b>A</b>
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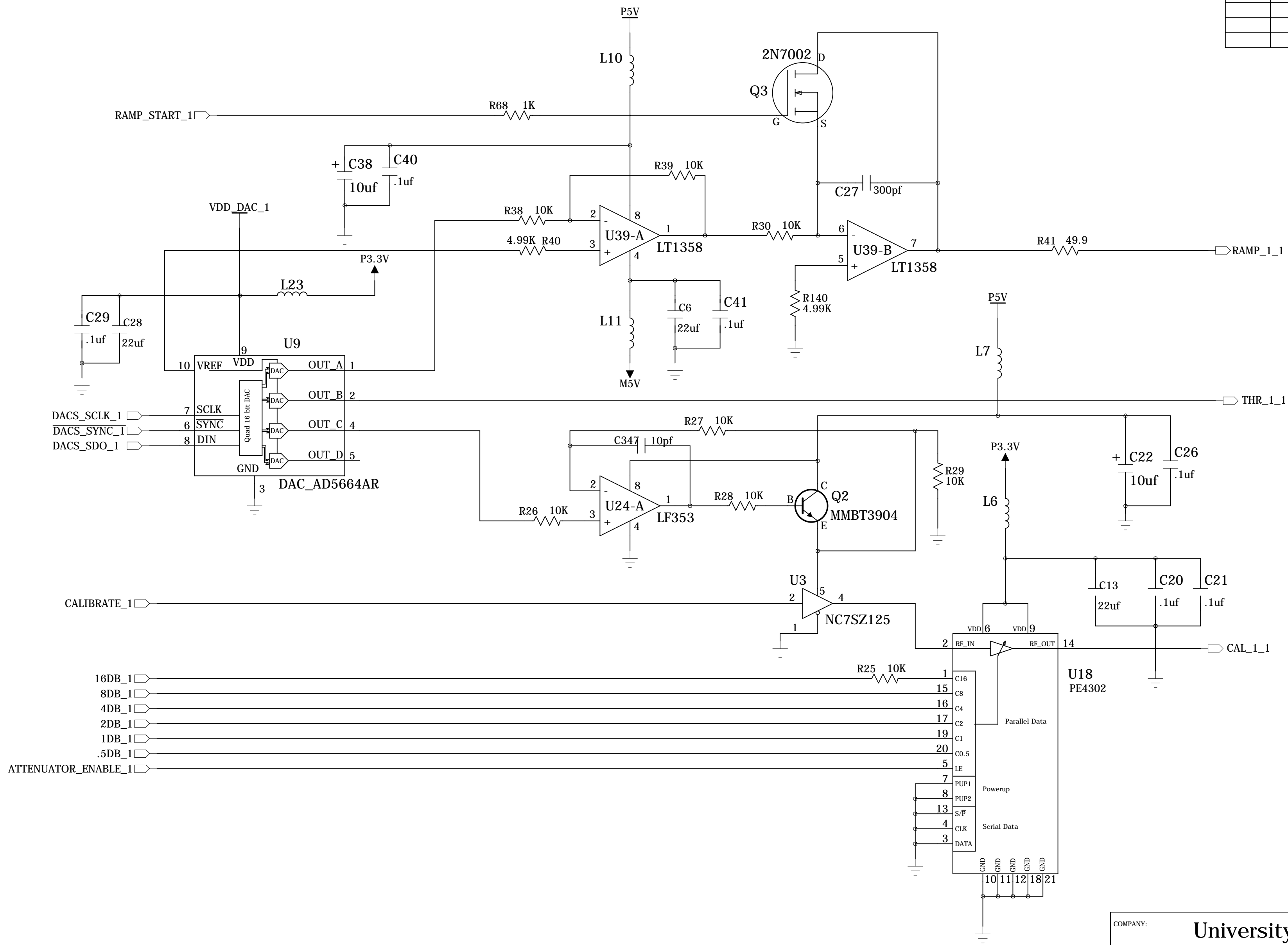
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DRAWN: J. Steinberg	DATED: 6/14/2010
CHECKED: <Checked By>	DATED: <Checked Date>
QUALITY CONTROL: <QC By>	DATED: <QC Date>
RELEASED: <Released By>	DATED: <Release Date>

COMPANY: <b>University of Arizona</b>			
TITLE: <b>C-Card Schematic Digital to Analog Converters</b>			
CODE: <b>&lt;Code&gt;</b>	SIZE: <b>C</b>	DRAWING NO: <b>PCB-0220-BD</b>	REV: <b>A</b>

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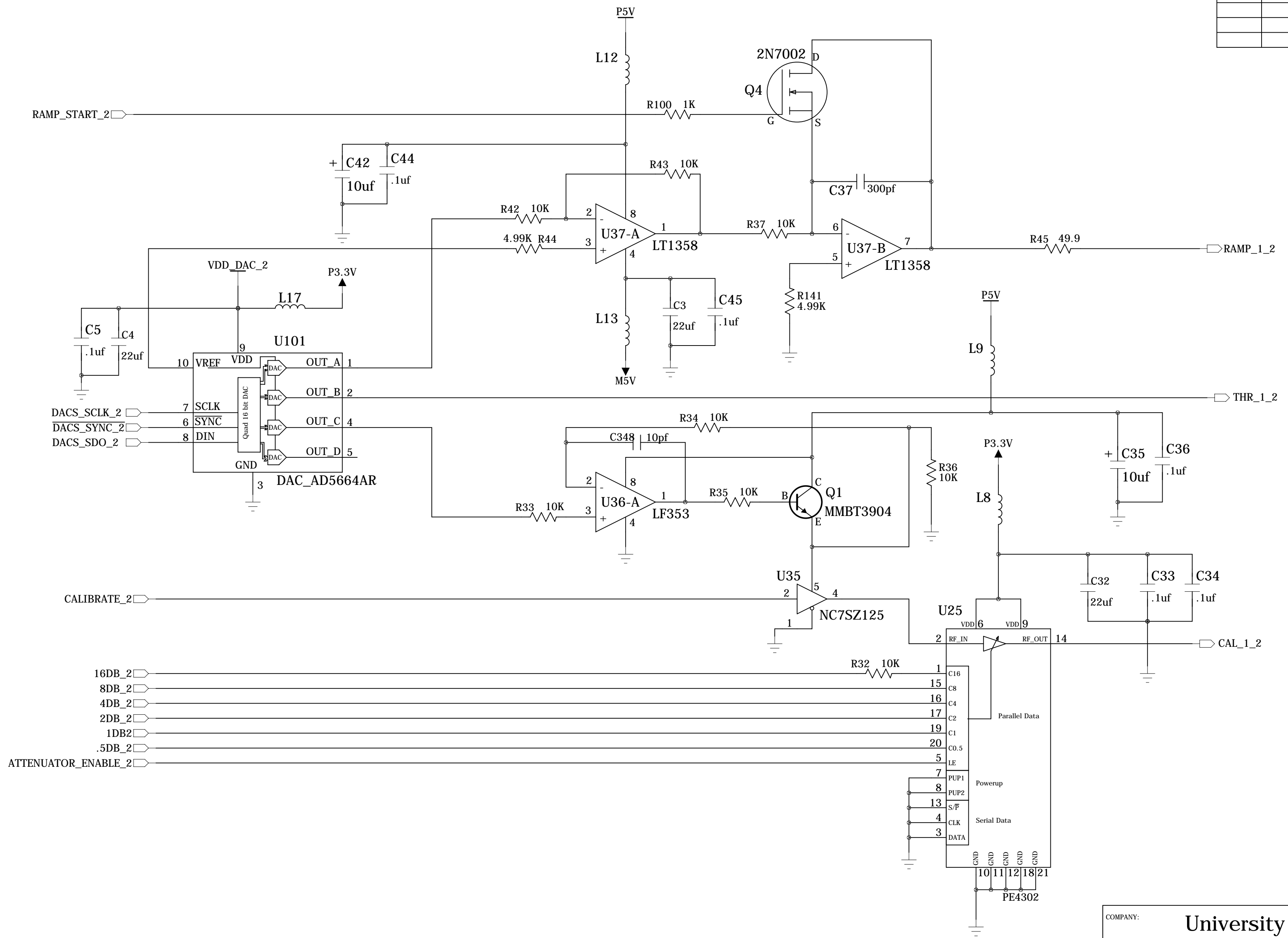
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DRAWN: J. Steinberg	DATED: 6/14/2010
CHECKED: <Checked By>	DATED: <Checked Date>
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COMPANY: <b>University of Arizona</b>			
TITLE: <b>C-Card Schematic Digital to Analog Converters</b>			
CODE: <b>&lt;Code&gt;</b>	SIZE: <b>C</b>	DRAWING NO: <b>PCB-0220-BD</b>	REV: <b>A</b>
SHEET: 12 of 26			

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REVISION RECORD			
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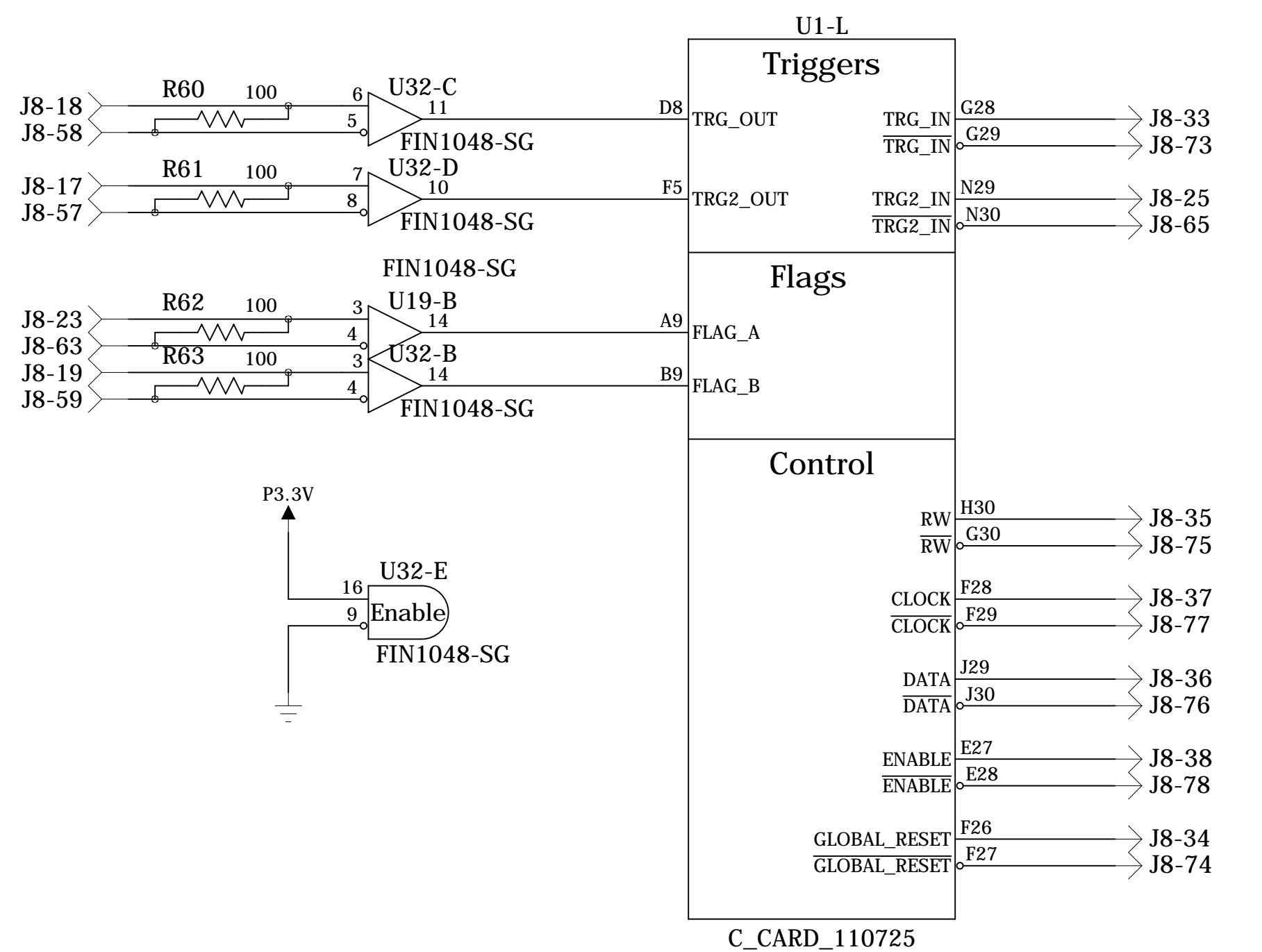
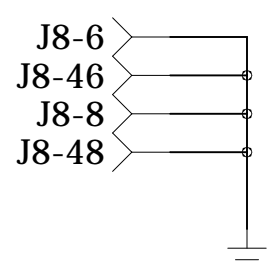
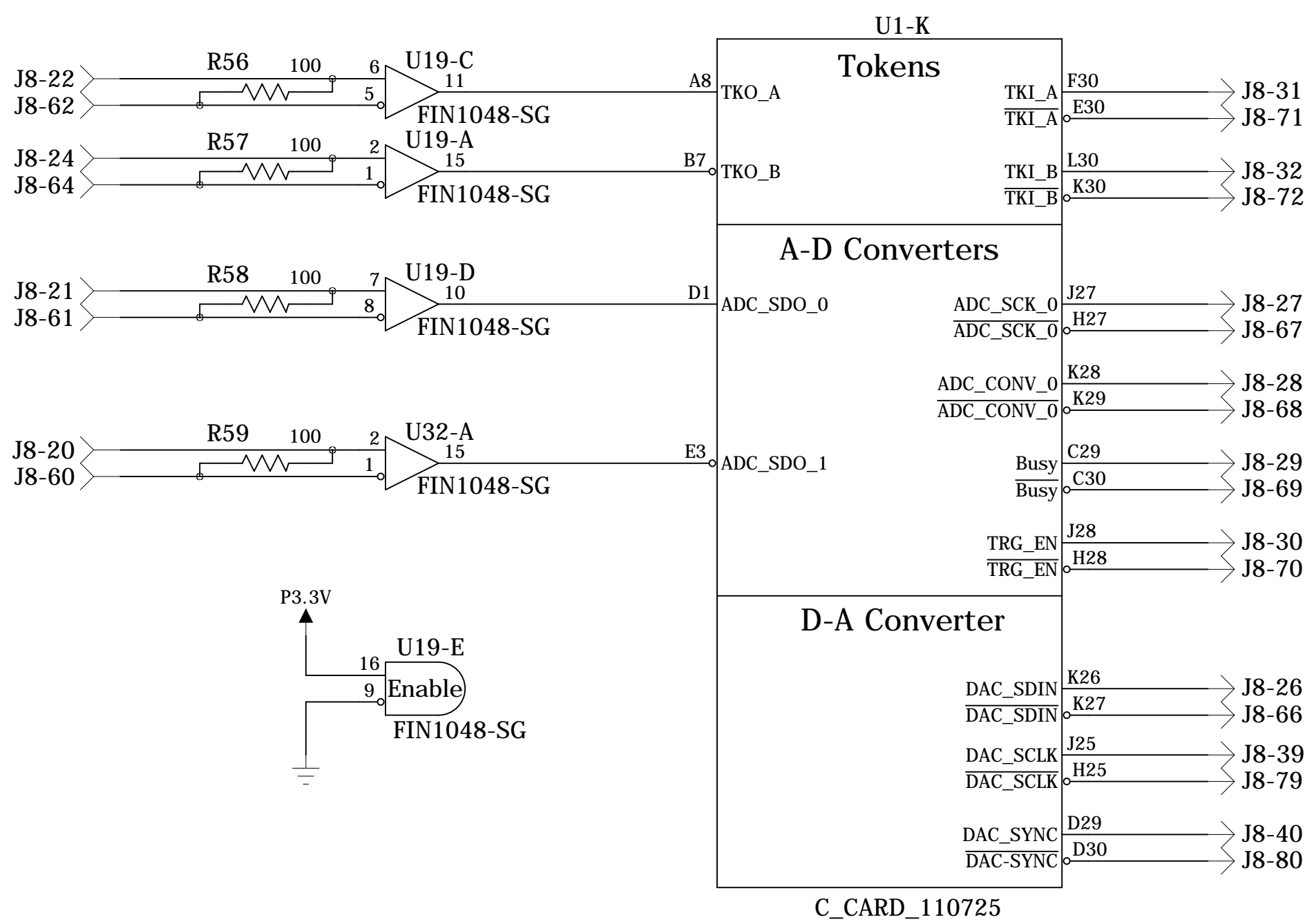
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DRAWN: J. Steinberg	DATED: 6/14/2010
CHECKED: <Checked By>	DATED: <Checked Date>
QUALITY CONTROL: <QC By>	DATED: <QC Date>
RELEASED: <Released By>	DATED: <Release Date>

COMPANY: <b>University of Arizona</b>			
TITLE: <b>C-Card Schematic Connections to MM-TPC</b>			
CODE: <b>&lt;Code&gt;</b>	SIZE: <b>C</b>	DRAWING NO: <b>PCB-0220-BD</b>	REV: <b>A</b>
SHEET: 13 of 26			

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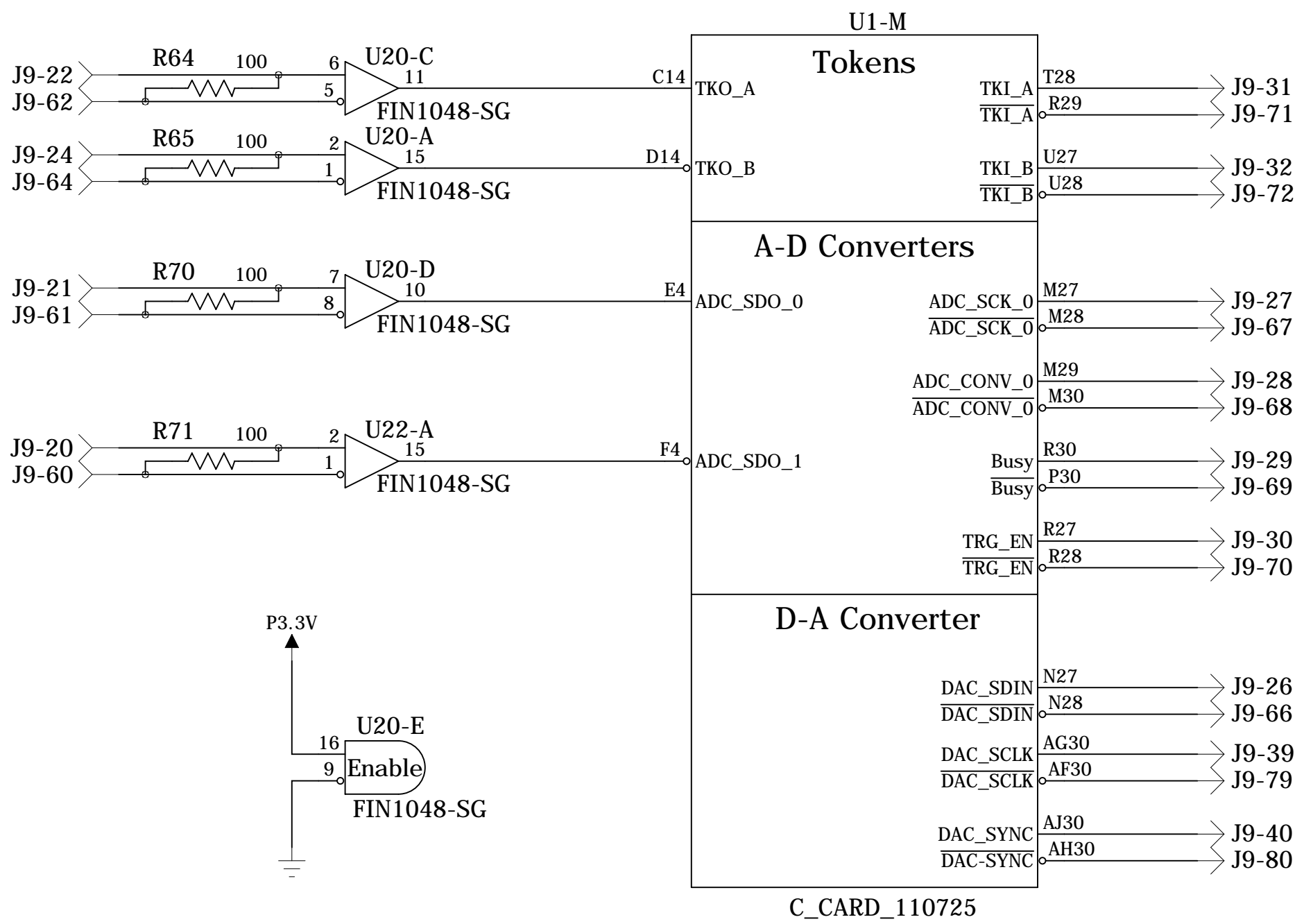
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LTR	ECO NO:	APPROVED:	DATE:

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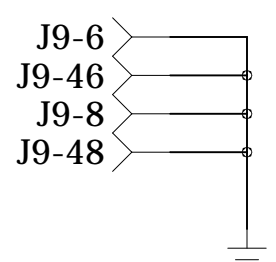
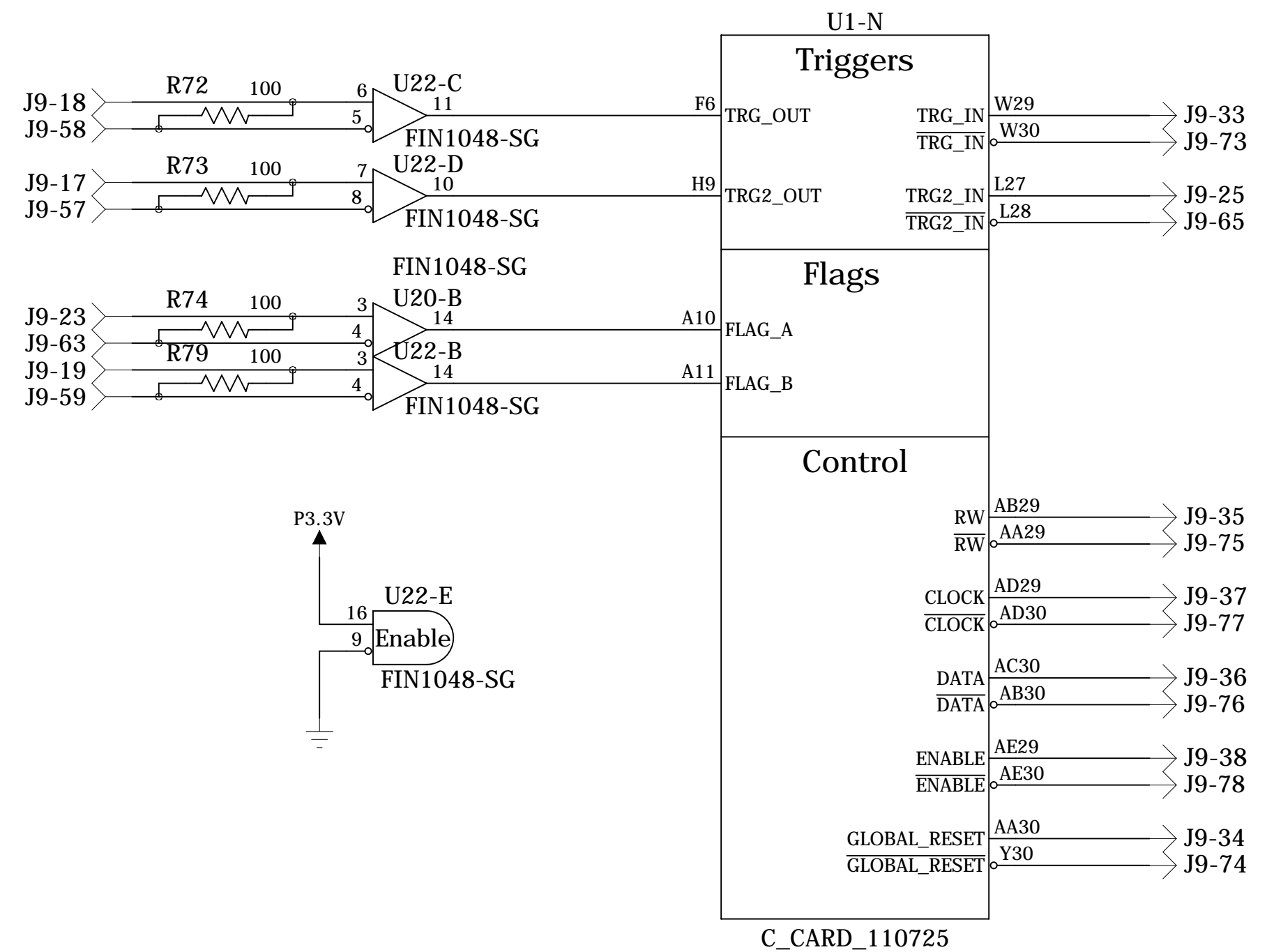
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COMPANY: <b>University of Arizona</b>			
TITLE: <b>C-Card Schematic Connections to MM-TPC</b>			
DRAWN: <b>J. Steinberg</b>	DATED: <b>6/14/2010</b>	CODE: <b>&lt;Code&gt;</b>	SIZE: <b>C</b>
CHECKED: <b>&lt;Checked By&gt;</b>	DATED: <b>&lt;Checked Date&gt;</b>	DRAWING NO: <b>PCB-0220-BD</b>	
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REVISION RECORD			
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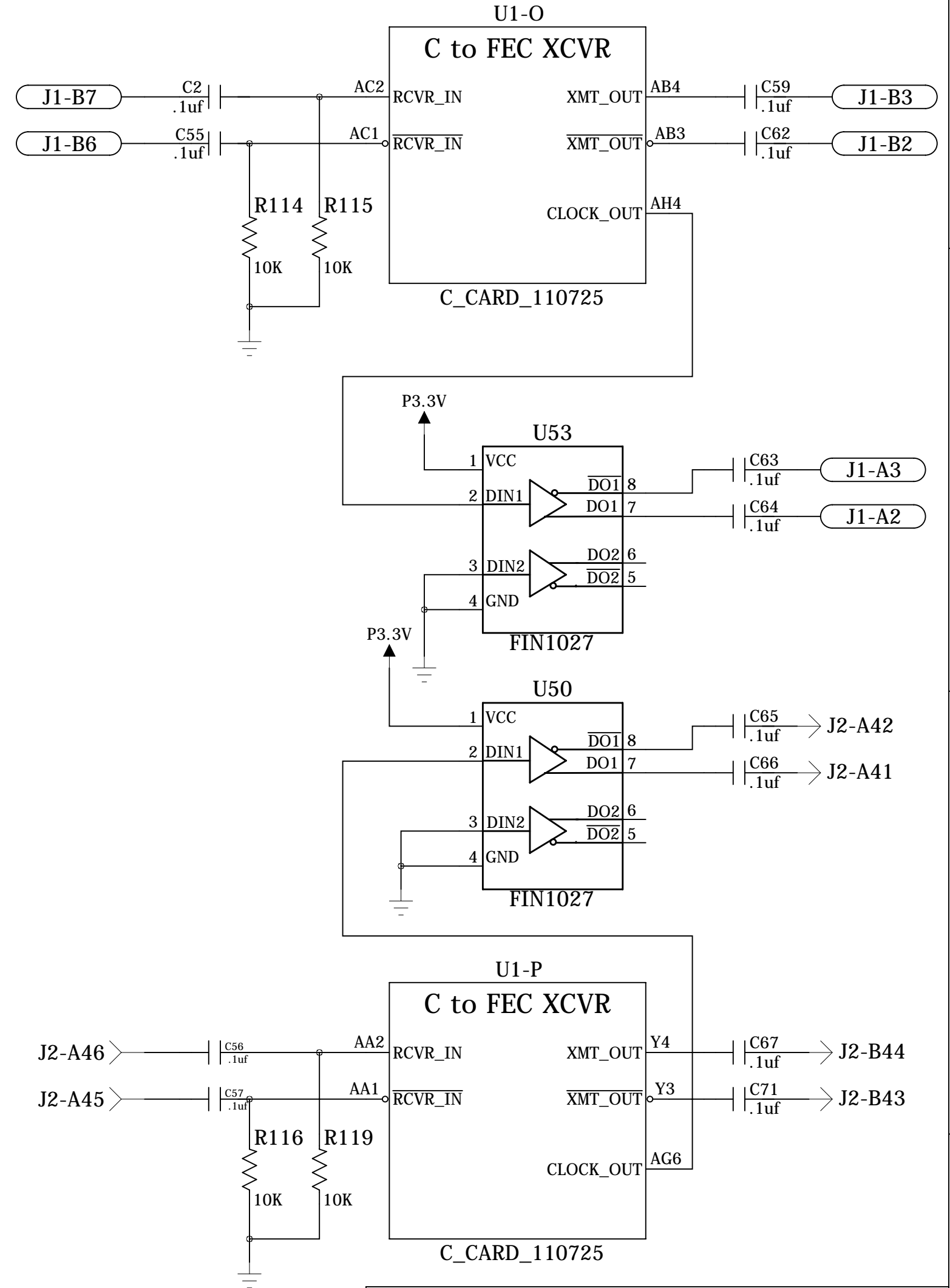
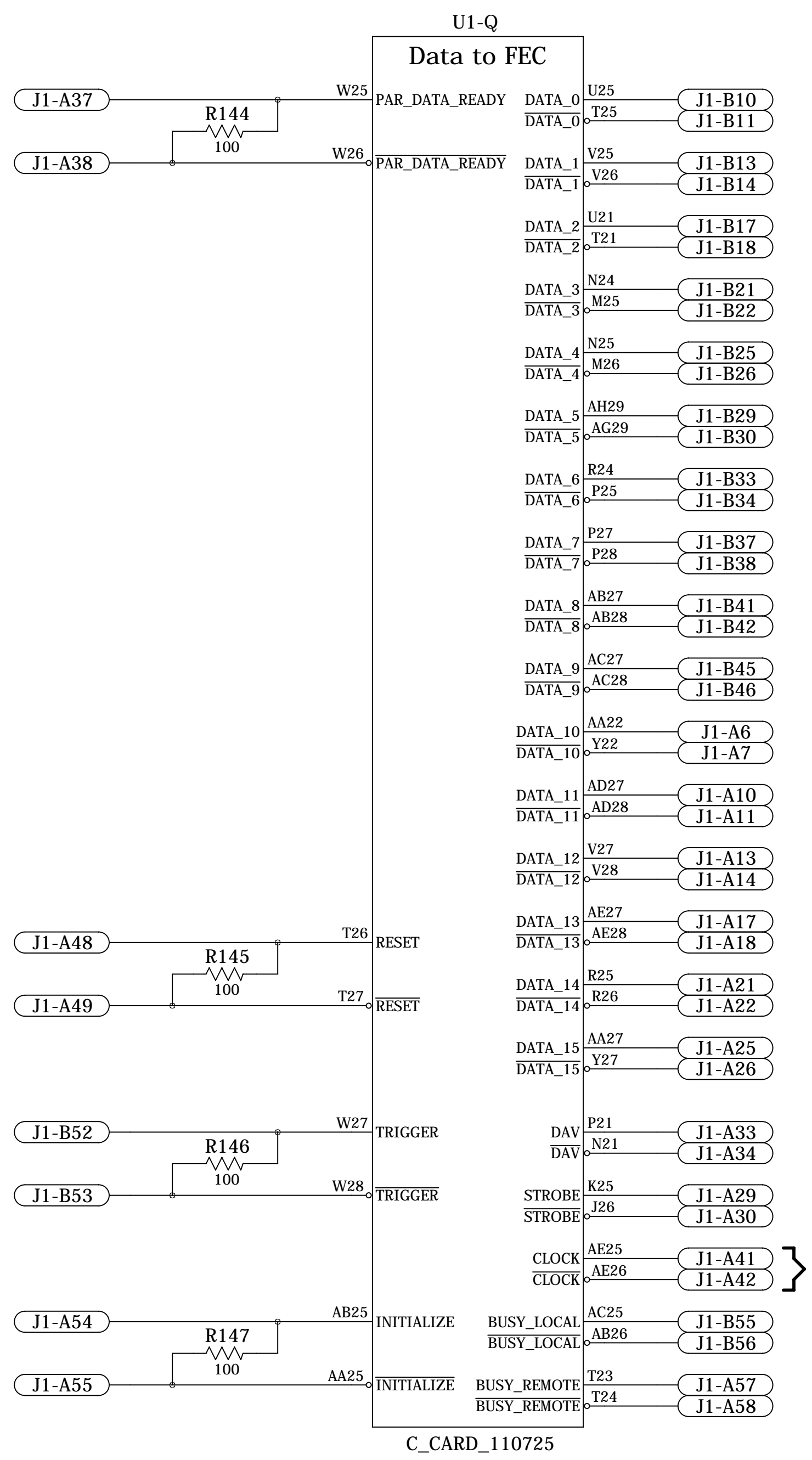
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COMPANY: **University of Arizona**

TITLE: **C-Card Schematic**  
**C-Card to FEC Logical Connections**

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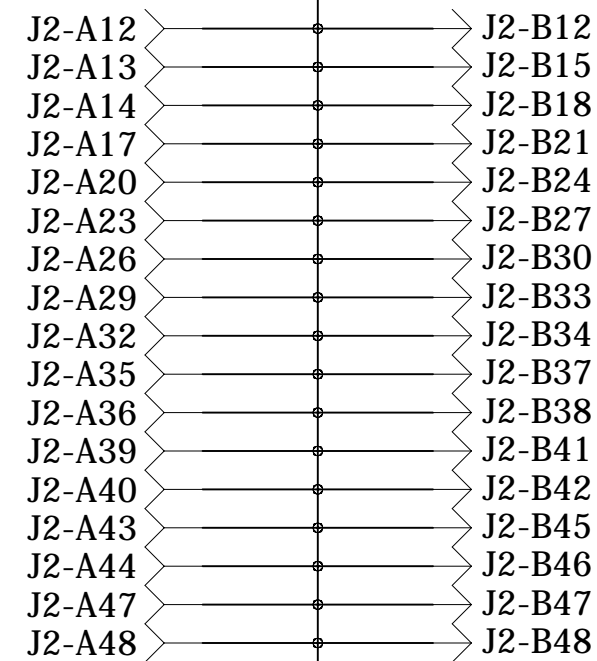
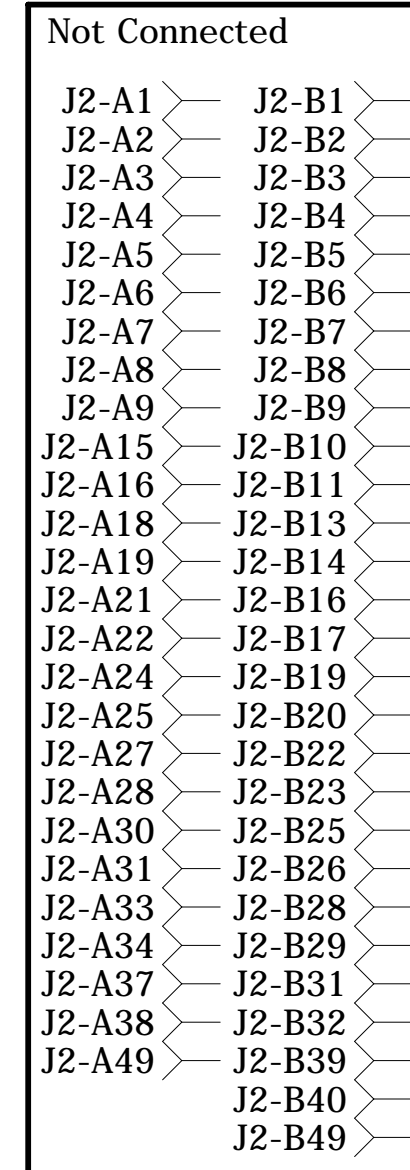
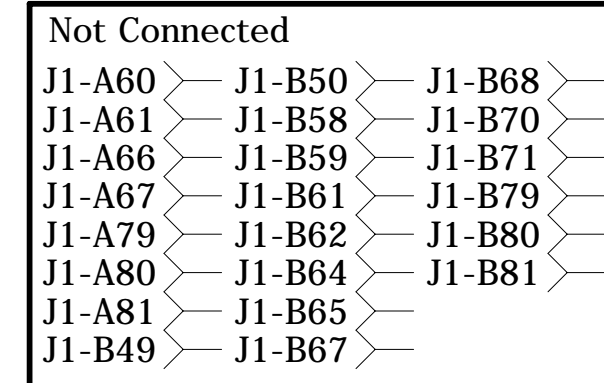
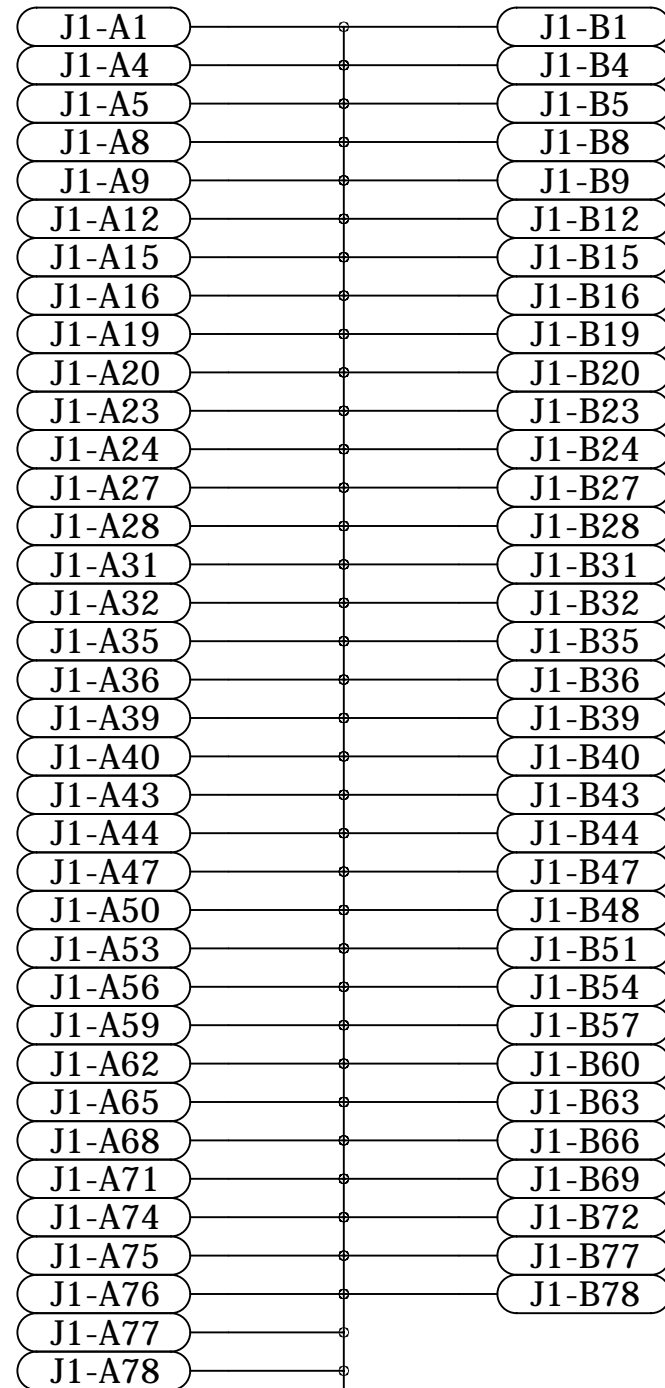
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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



COMPANY: **University of Arizona**

TITLE: **C-Card Schematic**

DRAWN: J. Steinberg	DATED: 6/14/2010
CHECKED: <Checked By>	DATED: <Checked Date>
QUALITY CONTROL: <QC By>	DATED: <QC Date>
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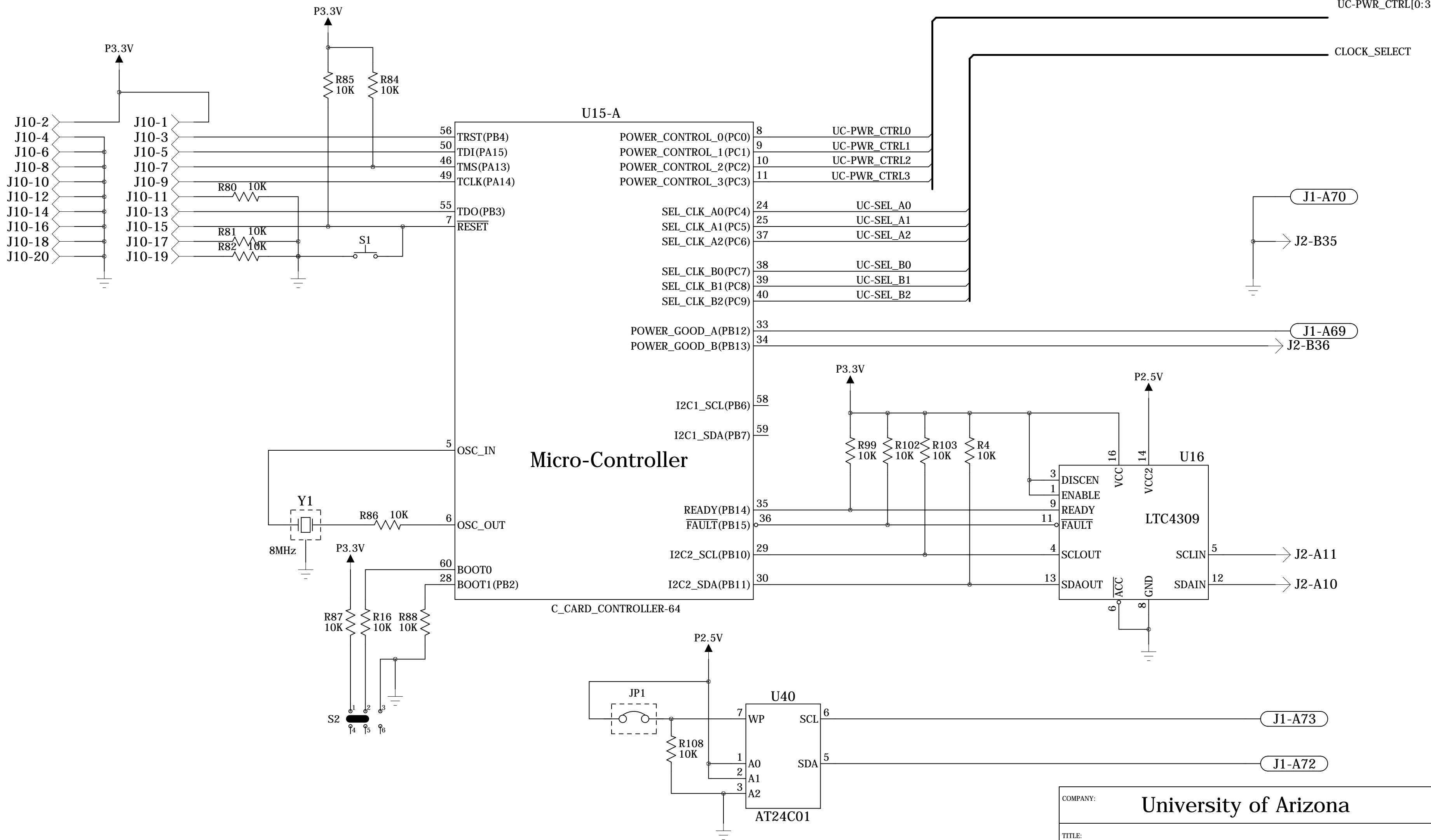
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COMPANY: University of Arizona

TITLE: C-Card Schematic

DRAWN: J. Steinberg	DATED: 6/14/2010
CHECKED: <Checked By>	DATED: <Checked Date>
QUALITY CONTROL: <QC By>	DATED: <QC Date>
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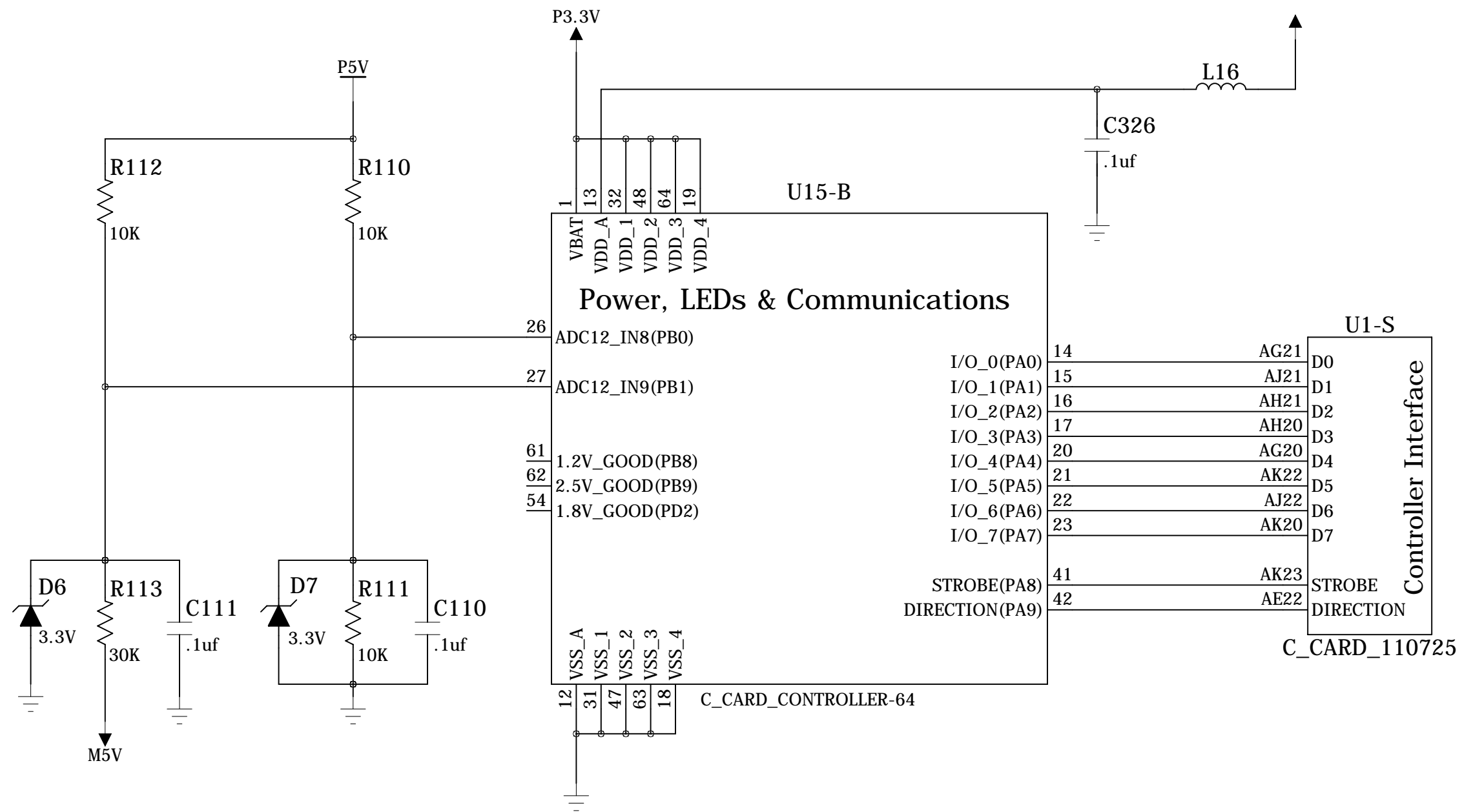
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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



COMPANY: **University of Arizona**

TITLE: **C-Card Schematic**

DRAWN: <b>J. Steinberg</b>	DATED: <b>6/14/2010</b>
CHECKED: <Checked By>	DATED: <Checked Date>
QUALITY CONTROL: <QC By>	DATED: <QC Date>
RELEASED: <Released By>	DATED: <Release Date>

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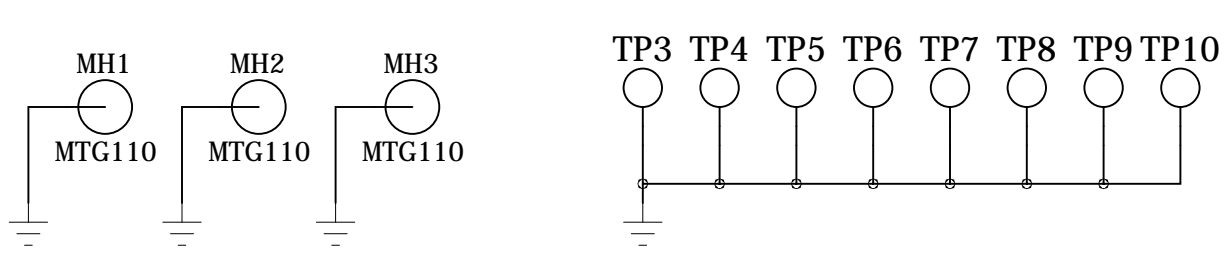
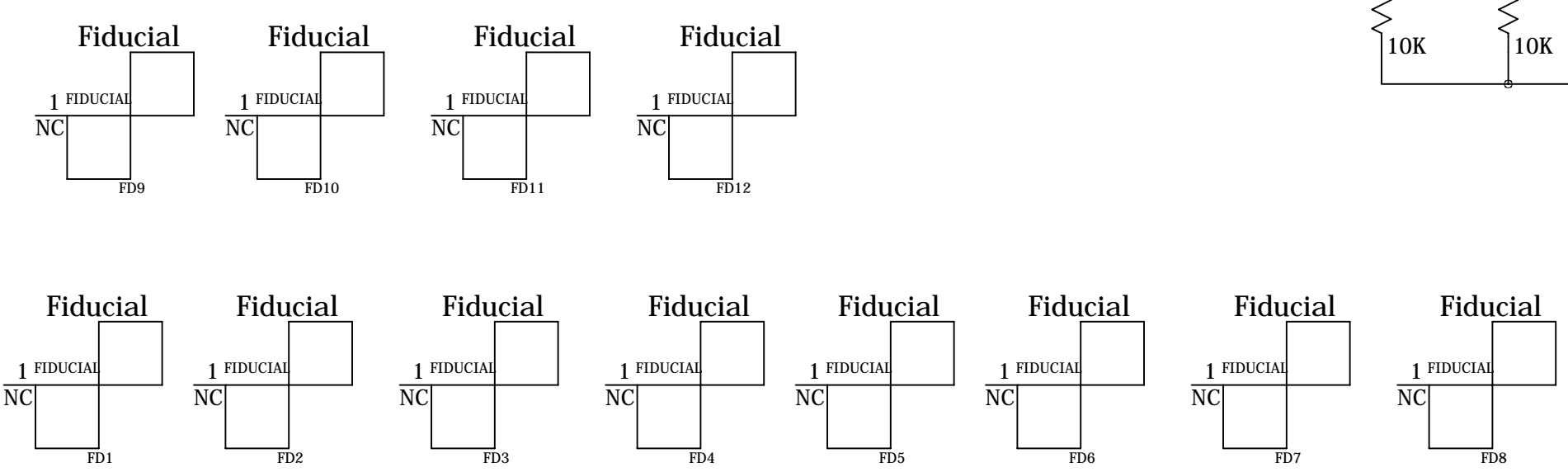
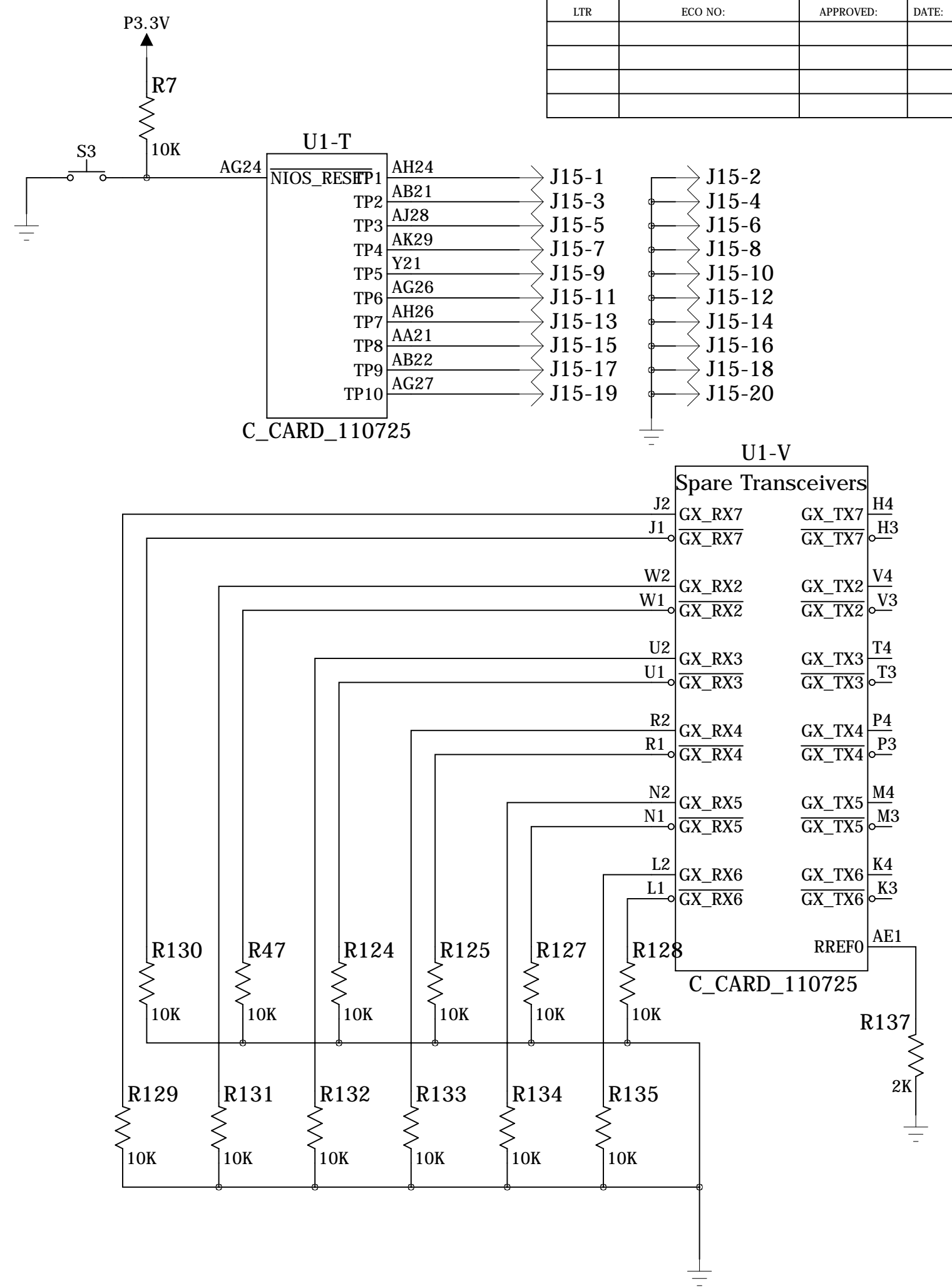
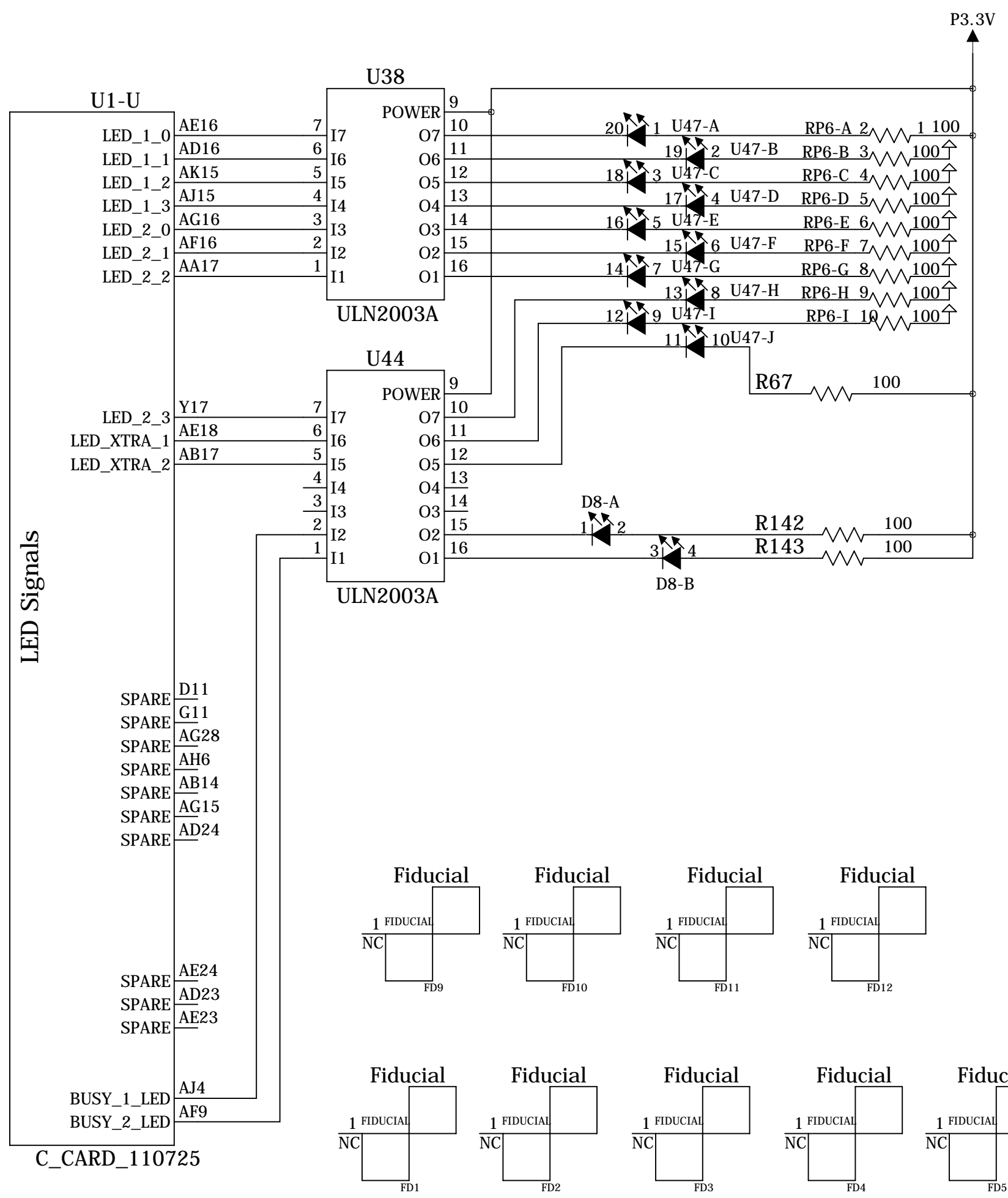
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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



COMPANY: University of Arizona			
TITLE: C-Card Schematic			
DRAWN: J. Steinberg	DATED: 6/14/2010	CODE: <Code>	SIZE: C
CHECKED: <Checked By>	DATED: <Checked Date>	DRAWING NO: PCB-0220-BD	
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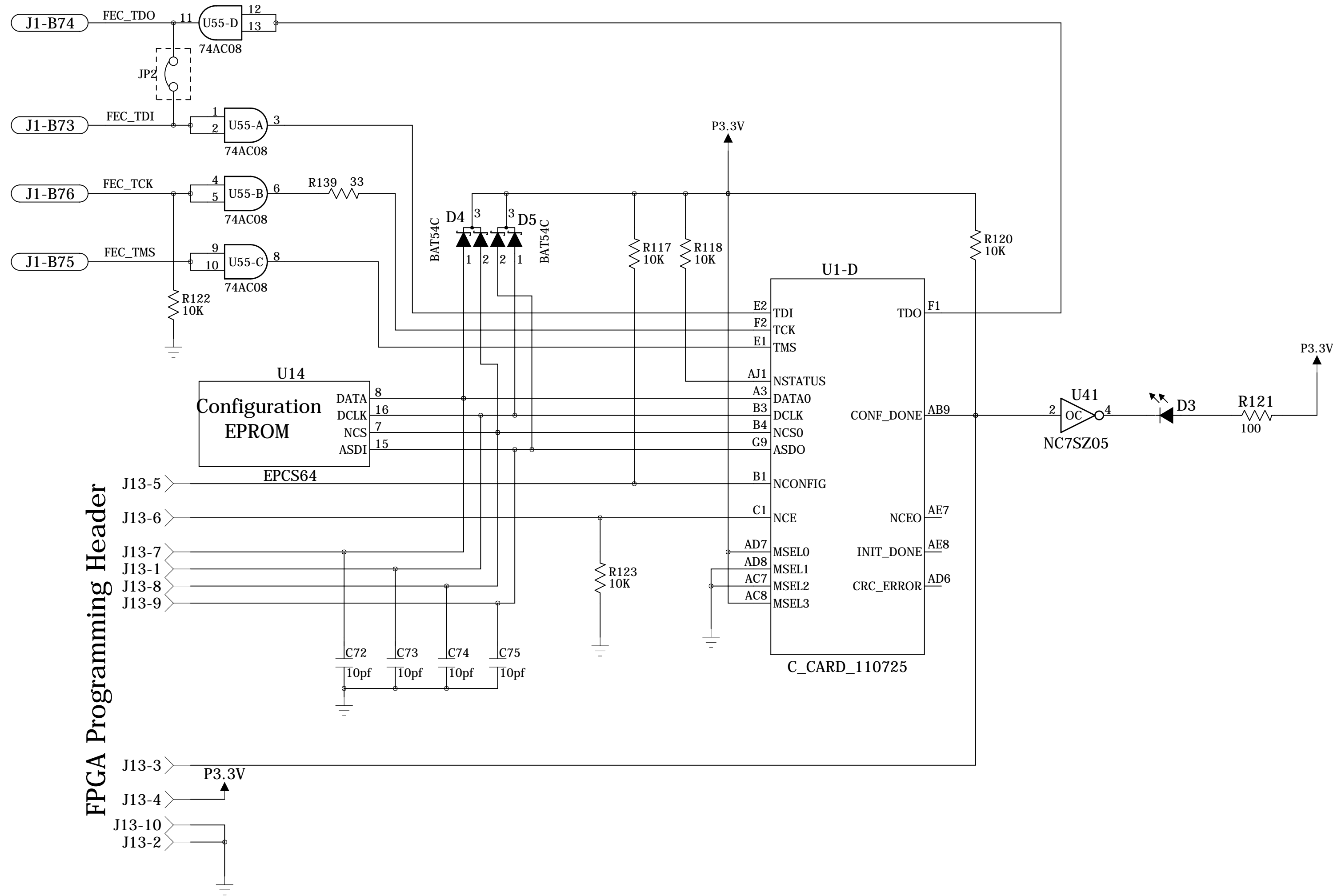
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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Connections for JTAG



FPGA Programming Header

COMPANY: University of Arizona			
TITLE: C-Card Schematic			
DRAWN: J. Steinberg	DATED: 6/14/2010	CODE:	SIZE:
CHECKED: <Checked By>	DATED: <Checked Date>	DRAWING NO: PCB-0220-BD	REV: A
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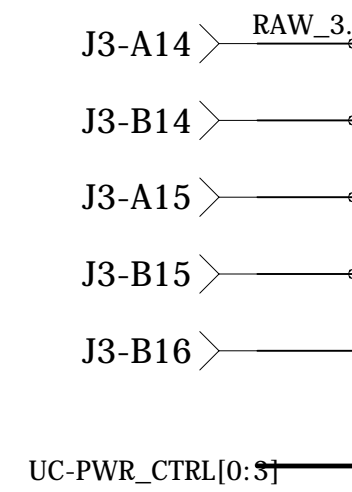
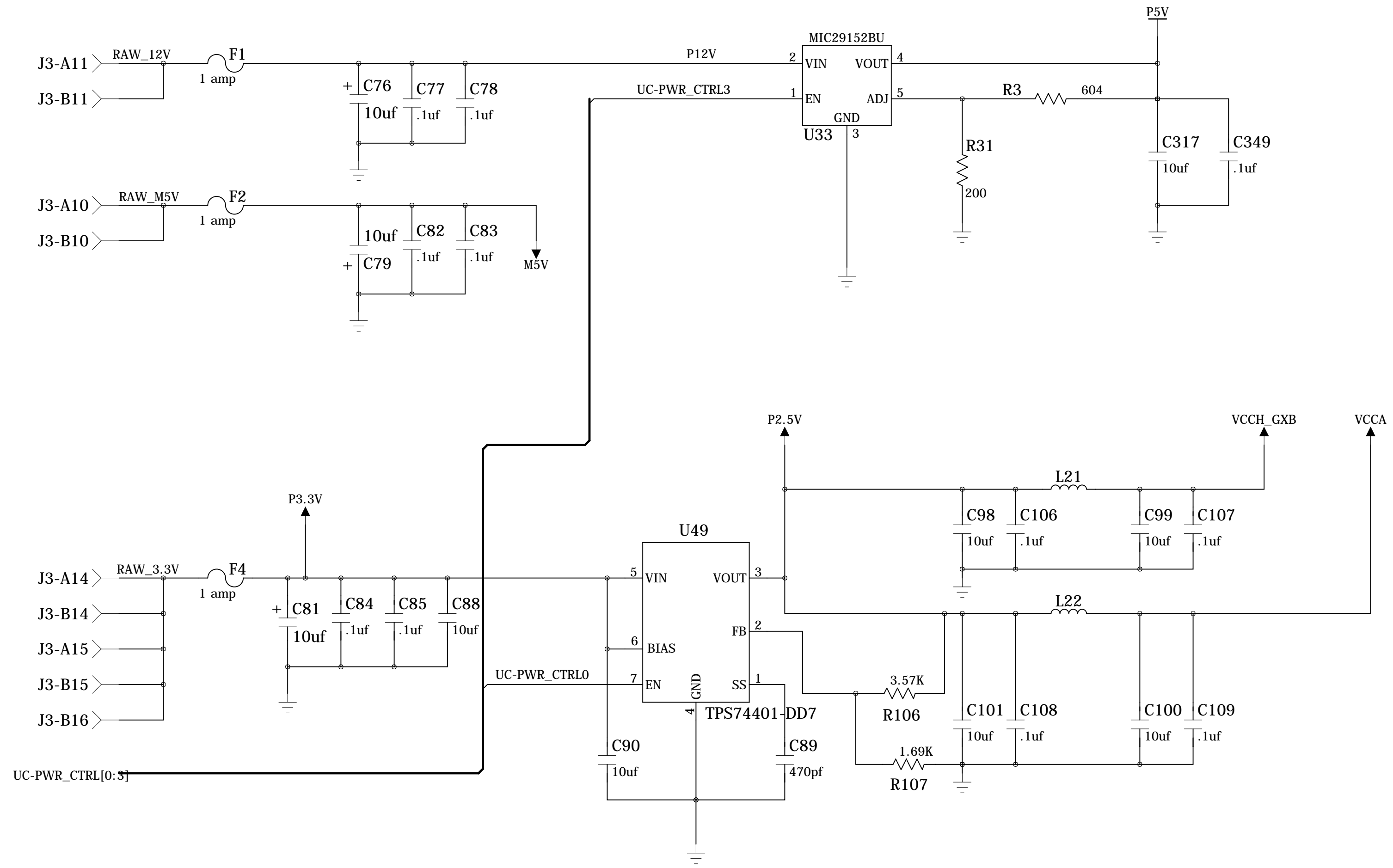
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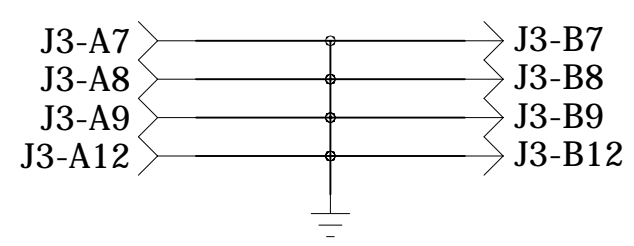
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J3-A3	J3-B3
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J3-A5	J3-B5
J3-A6	J3-B6
J3-A13	J3-B13
J3-A16	J3-B17
J3-A17	J3-B18
J3-A18	



COMPANY: University of Arizona			
TITLE: C-Card Schematic			
DRAWN: J. Steinberg	DATED: 6/14/2010	CODE: <Code>	SIZE: C
CHECKED: <Checked By>	DATED: <Checked Date>	DRAWING NO: PCB-0220-BD	REV: A
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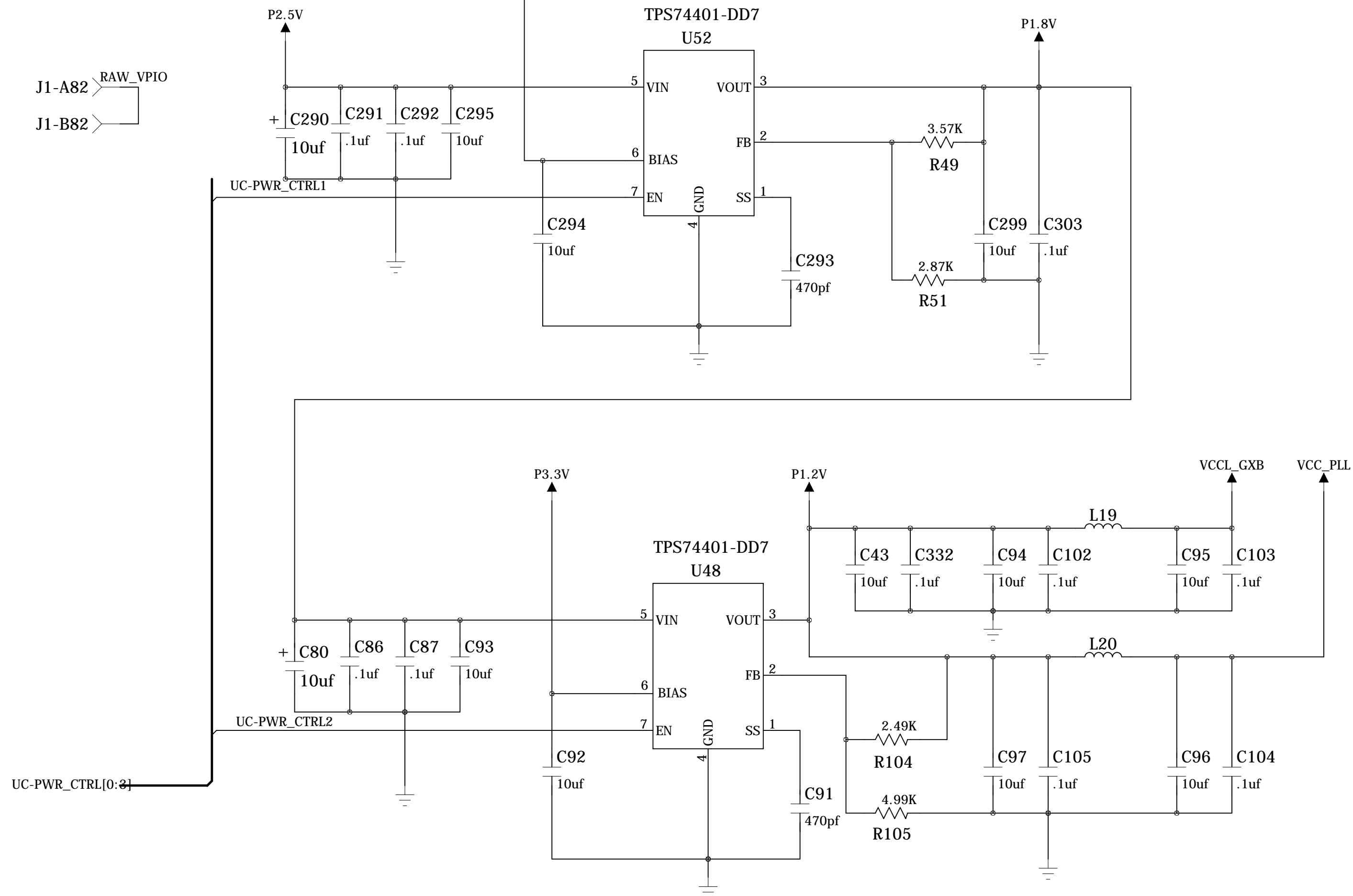
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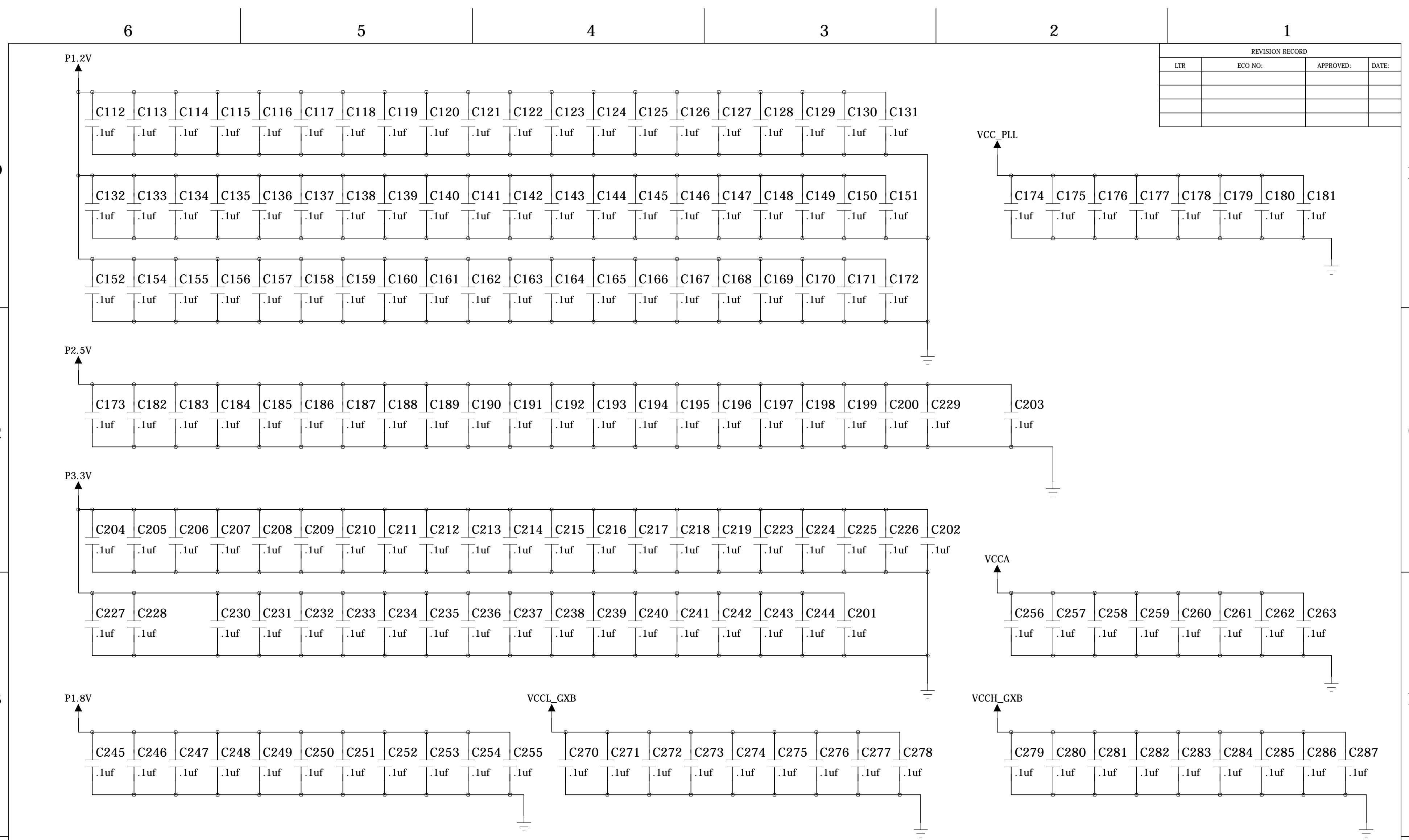
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LTR	ECO NO:	APPROVED:	DATE:

Note:  
VPIO is set to 2.5V on the FEC "A" Connector



COMPANY: University of Arizona			
TITLE: C-Card Schematic			
DRAWN: J. Steinberg	DATED: 6/14/2010	CODE: <Code>	SIZE: C
CHECKED: <Checked By>	DATED: <Checked Date>	DRAWING NO: PCB-0220-BD	REV: A
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RELEASED: <Released By>	DATED: <Release Date>		

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



Decoupling Capacitors for FPGA  
 All capacitors are size 0201

DRAWN: J. Steinberg	DATED: 6/14/2010
CHECKED: <Checked By>	DATED: <Checked Date>
QUALITY CONTROL: <QC By>	DATED: <QC Date>
RELEASED: <Released By>	DATED: <Release Date>

COMPANY: <b>University of Arizona</b>			
TITLE: <b>C-Card Schematic</b>			
CODE: <b>&lt;Code&gt;</b>	SIZE: <b>C</b>	DRAWING NO: <b>PCB-0220-BD</b>	REV: <b>A</b>
SHEET: 23 of 26			

6

5

4

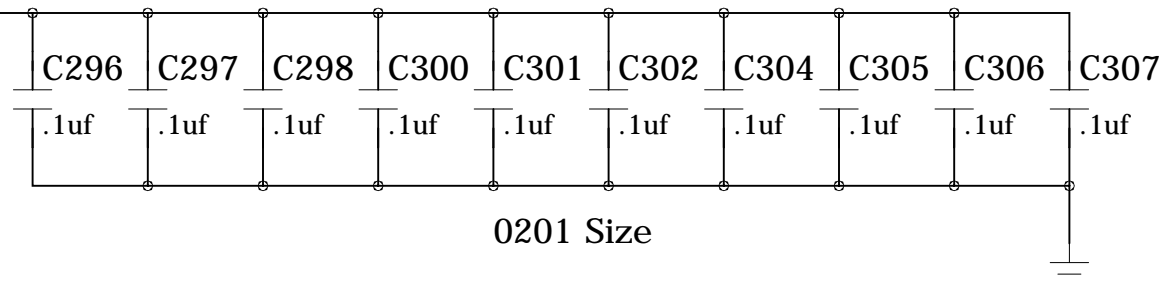
3

2

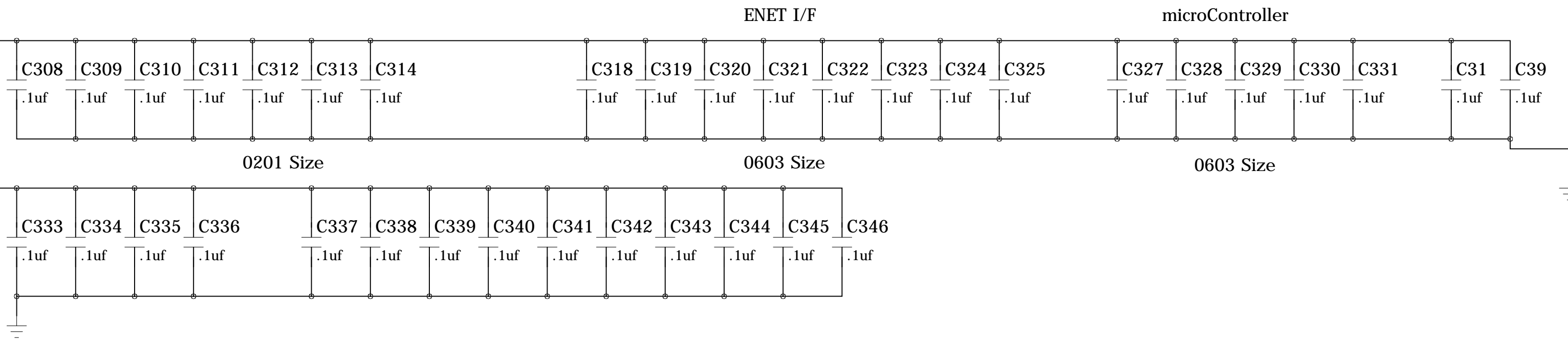
1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

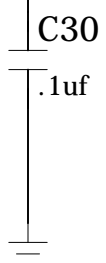
P1.8V



P3.3V



P2.5V



COMPANY: <b>University of Arizona</b>			
TITLE: <b>C-Card Schematic</b>			
DRAWN: <b>J. Steinberg</b>	DATED: <b>6/14/2010</b>	CODE:	SIZE: <b>C</b>
CHECKED: <b>&lt;Checked By&gt;</b>	DATED: <b>&lt;Checked Date&gt;</b>	DRAWING NO: <b>PCB-0220-BD</b>	REV: <b>A</b>
QUALITY CONTROL: <b>&lt;QC By&gt;</b>	DATED: <b>&lt;QC Date&gt;</b>	SHEET: 24 of 26	
RELEASED: <b>&lt;Released By&gt;</b>	DATED: <b>&lt;Release Date&gt;</b>		



6

5

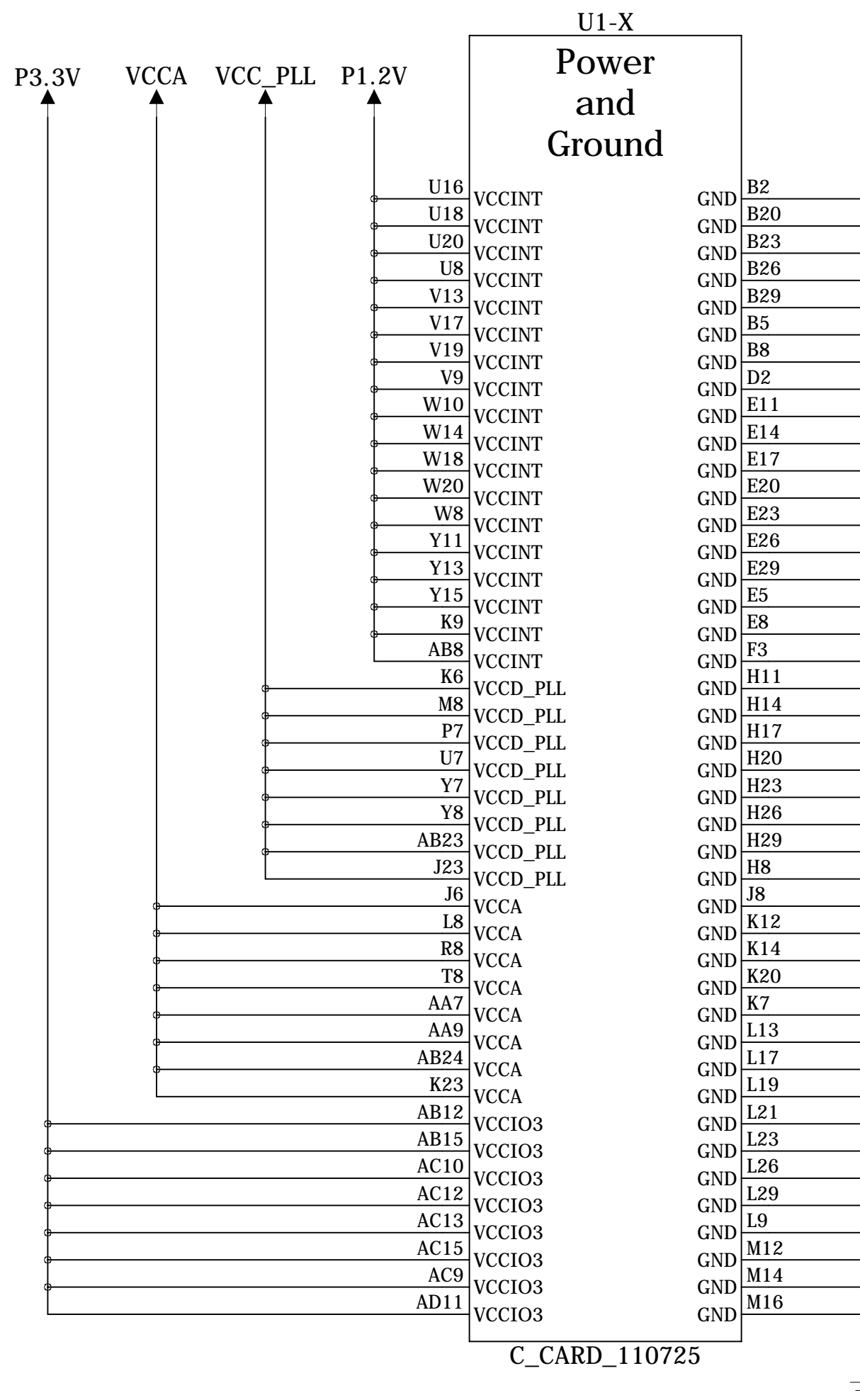
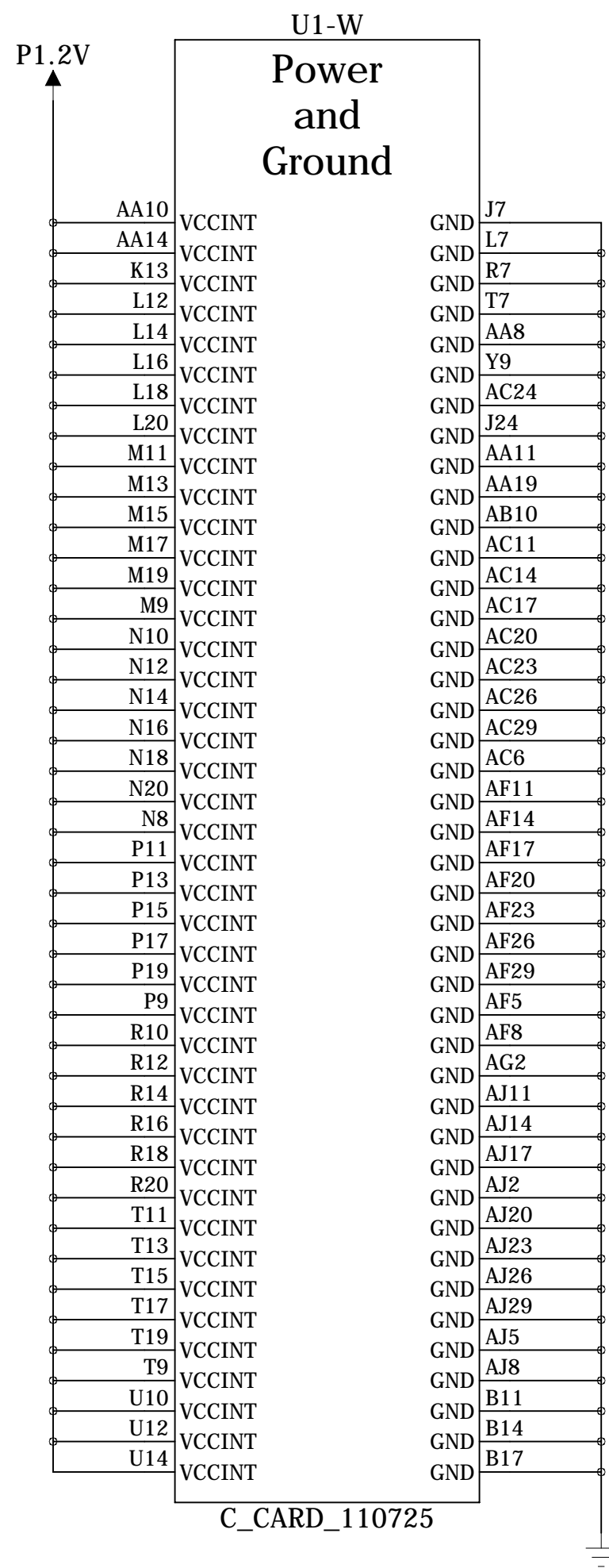
4

3

2

1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



COMPANY: <b>University of Arizona</b>			
TITLE: <b>C-Card Schematic</b>			
DRAWN: <b>J. Steinberg</b>	DATED: <b>6/14/2010</b>	CODE: <b>&lt;Code&gt;</b>	SIZE: <b>C</b>
CHECKED: <b>&lt;Checked By&gt;</b>	DATED: <b>&lt;Checked Date&gt;</b>	DRAWING NO: <b>PCB-0220-BD</b>	
QUALITY CONTROL: <b>&lt;QC By&gt;</b>	DATED: <b>&lt;QC Date&gt;</b>	REV: <b>A</b>	
RELEASED: <b>&lt;Released By&gt;</b>	DATED: <b>&lt;Release Date&gt;</b>	SHEET: 25 of 26	

6

5

4

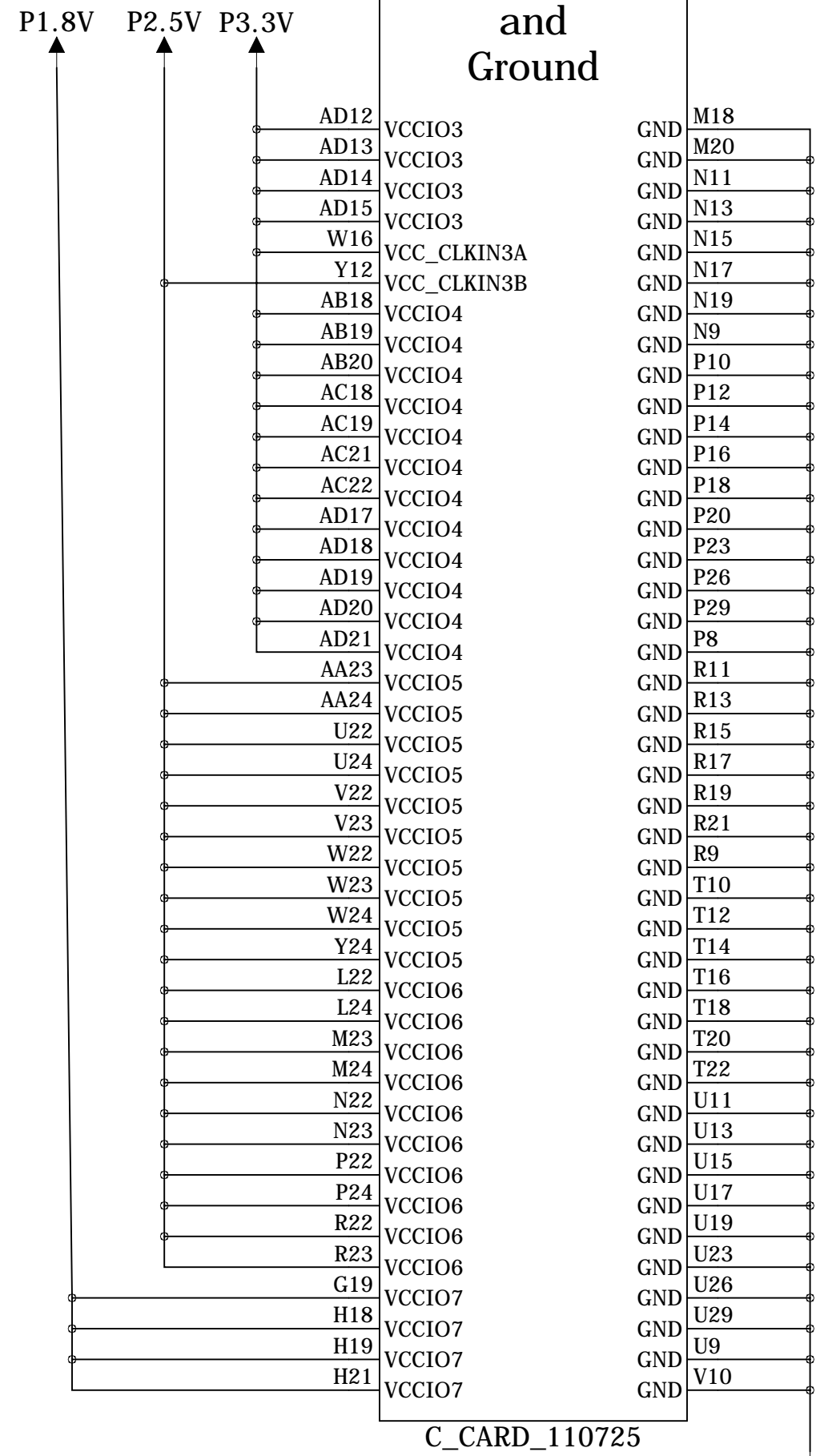
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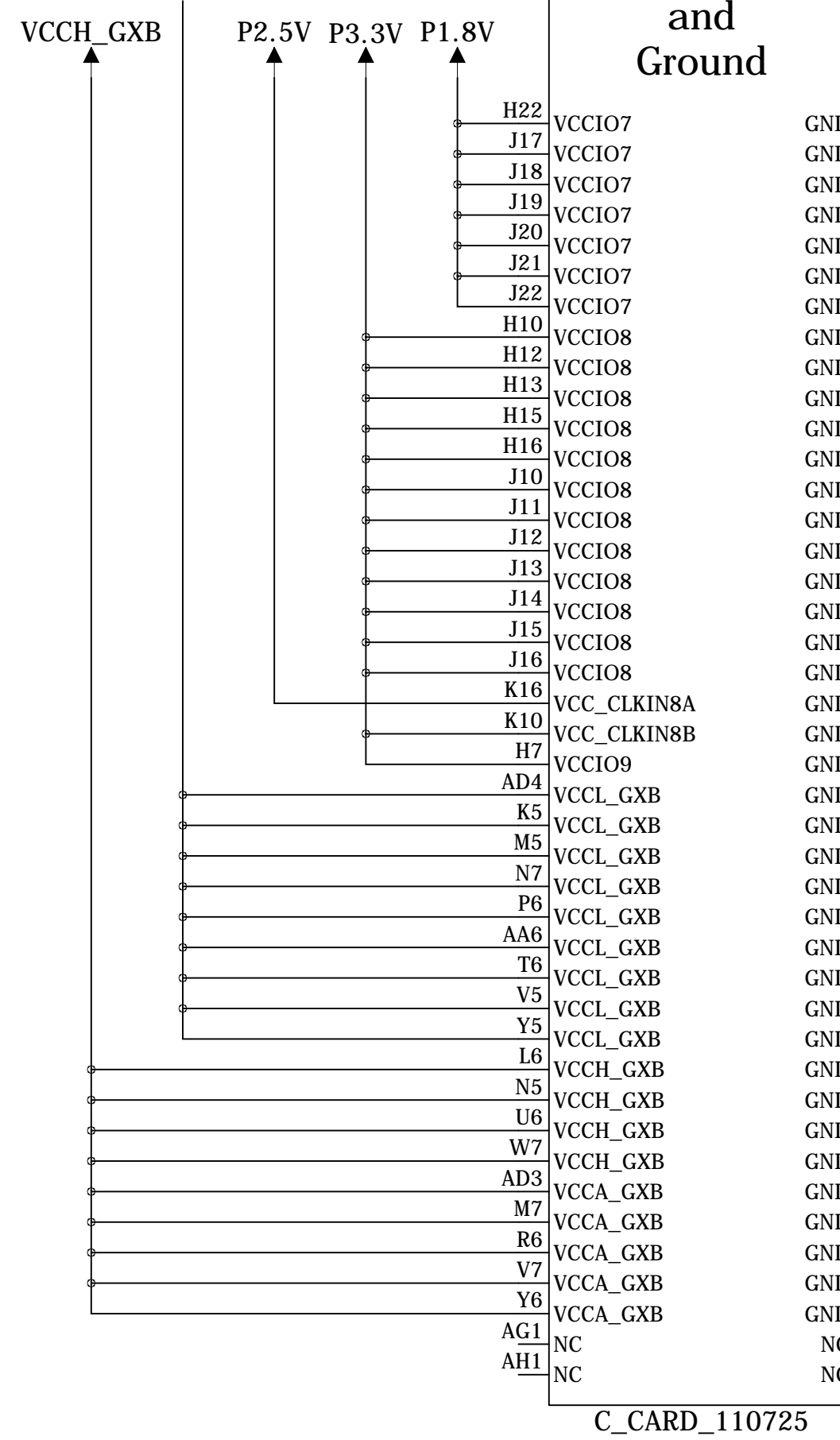
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

**U1-Y  
Power  
and  
Ground**



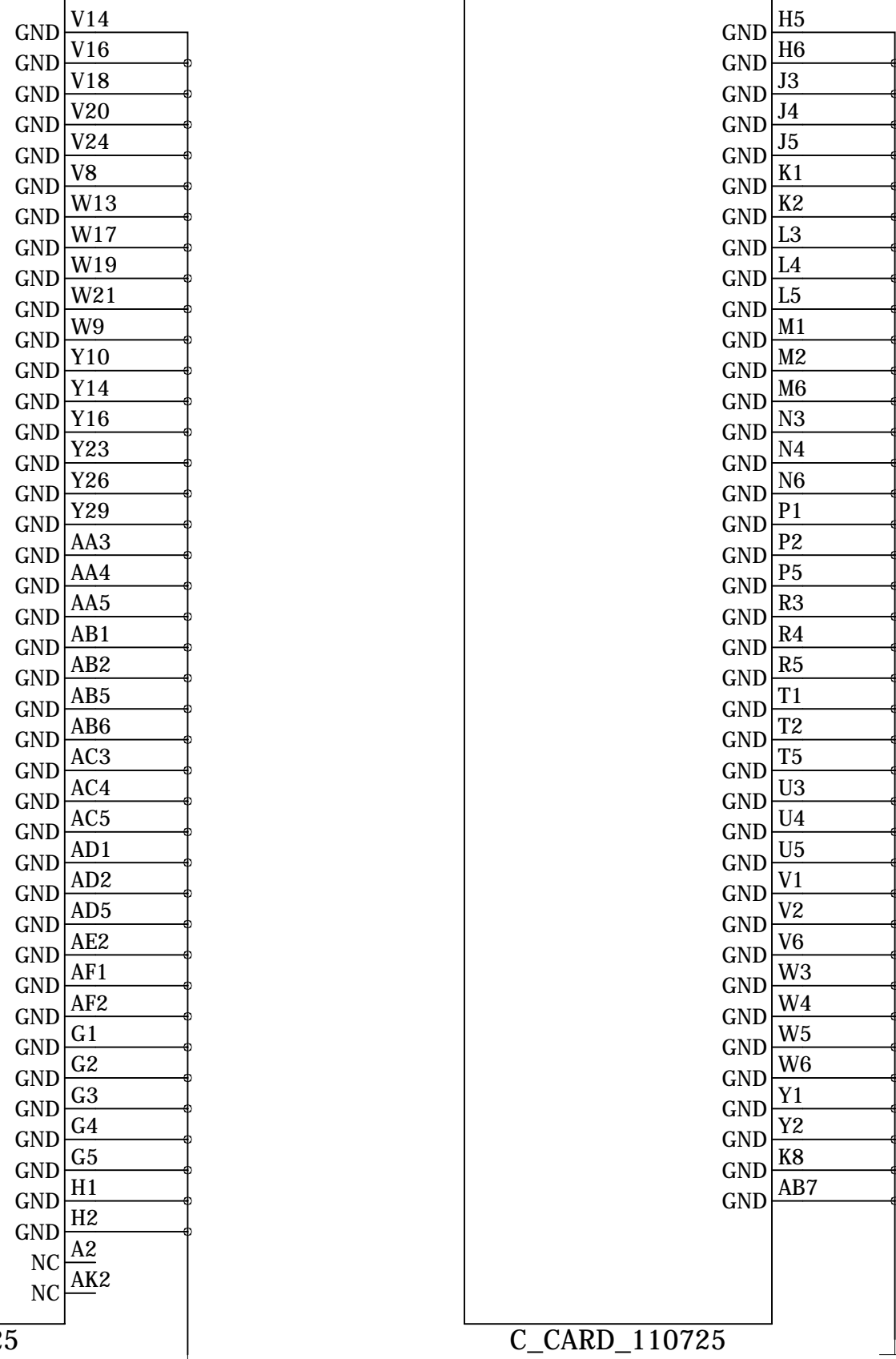
C\_CARD\_110725

**U1-Z  
Power  
and  
Ground**



C\_CARD\_110725

**U1-AA  
Ground**



C\_CARD\_110725

COMPANY: **University of Arizona**

TITLE: **C-Card Schematic**

DRAWN: J. Steinberg	DATED: 6/14/2010
CHECKED: <Checked By>	DATED: <Checked Date>
QUALITY CONTROL: <QC By>	DATED: <QC Date>
RELEASED: <Released By>	DATED: <Release Date>

CODE:	SIZE:	DRAWING NO:	REV:
<Code>	C	PCB-0220-BD	A