Xilinx Artix 7 - Micro Megas Front End - 8 VMM Card	
Function	**Sheet Number**
1_0301-MMFE-8_TitleSheet	1
2_0301-MMFE-8_Bank0	2
3_0301-MMFE-8_Bank14lvds	3
4_0301-MMFE-8_Bank13miniSAS	4
5_0301-MMFE-8_Bank15vmm12	5
6_0301-MMFE-8_Bank16vmm34	6
7_0301-MMFE-8_Bank35vmm56	7
8_0301-MMFE-8_Bank34vmm78	8
9_0301-MMFE-8_Ethernet	9
10_0301-MMFE-8_MGT	10
11_0301-MMFE-8_Power1	11
12_0301-MMFE-8_Power2	12
13_0301-MMFE-8_Power3	13
14_0301-MMFE-8_Power4	14
15_0301-MMFE-8_Power5	15
16_0301-MMFE-8_Analog1	16
17_0301-MMFE-8_Analog2	17
18_0301-MMFE-8_Analog3	18
19_0301-MMFE-8_Analog4	19
20_0301-MMFE-8_Analog5	20
21_0301-MMFE-8_Analog6	21
22_0301-MMFE-8_Analog7	22
23_0301-MMFE-8_Analog8	23
24_0301-MMFE-8_VMM	24

THE UNIVERSITY OF ARIZONA®

Physics Department
0301-MMFE-8 A
11/11/2014
10:24:28 AM

Services / NRE

PCB1
ASSY_PCB_Layout
PCB layout / 5 boards

PCB2
ASSY_PCB_Man
PCB only

PCB3
ASSY_PCB_Assy
PCB assembly

Accessories

CBL1
CBL-miniSAS-36
miniSAS 4i 36 ckts

CBL2
CBL-miniSAS-36
miniSAS 4i 36 ckts

Title: *0301-MMFE-8_Title*		*University of Arizona* *1118 E 4th St* *Tucson, Arizona 85721*
Size: B	Engineer: William Hart	Revision: A
Date: 11/11/2014	Time: 10:24:28 AM	Sheet 1 of 23
File: C:\Pjcts\AltProj\0301-MMFE_8\0301-MMFE8-11-10-14tst\1_0301-MMFE-8_TitleSheet.SchDoc		*billhart@email.arizona.edu*

Bank 0:
Contains Configuration and Analog - Digital Converter functionality.
Bank Voltage is 2V5.

N25Q256A11EF840x is256Mb Quad SPI FLASH, used to configure the FPGA. XC7A200T requires 77,845,216b stream.

Since Flash does not typically run at 2V5, translators must be used.

All paired routing is 100 Ohm Differential and length matched TBD
All un-paired routing is 50 Ohm single ended.

JTAG

Diode is used to prevent any current backflow from a Parallel IV cable connection. Diode is probably no-longer required, Pullups are probably no longer required either

Use Digilent JTAG HS1,2 Programming Cable Part # 410-249P-KIT in place of installing JTAG SMT2 Surface-Mount Programming Module.

SPI Flash ROM Signal / Pin Equivalences
C = Clock = Input
DQ0 = Serial Data In = Input
DQ1 = Serial Data Out = Output
S_N = CS = Input
For Quad, DQ pins are BiDirectional...

Per Impact Help:
Micron (Numonyx)
N25Q 3.3V (1) 32Mb – 256Mb Kintex™-7, Artix™-7
N25Q 1.8V (1) 32Mb – 256Mb Kintex-7/Virtex-7, Artix- 7
1.For Numonyx N25Q: Top, Bottom, and Uniform block sectors are supported.

Place serial termination resistor close to the FPGA

Configuration Done

Please Refer to XAPP586

Configuration Flash

Reconfigure Switch

SSWITCH TACTILE SPST-NO 0.02A 15V

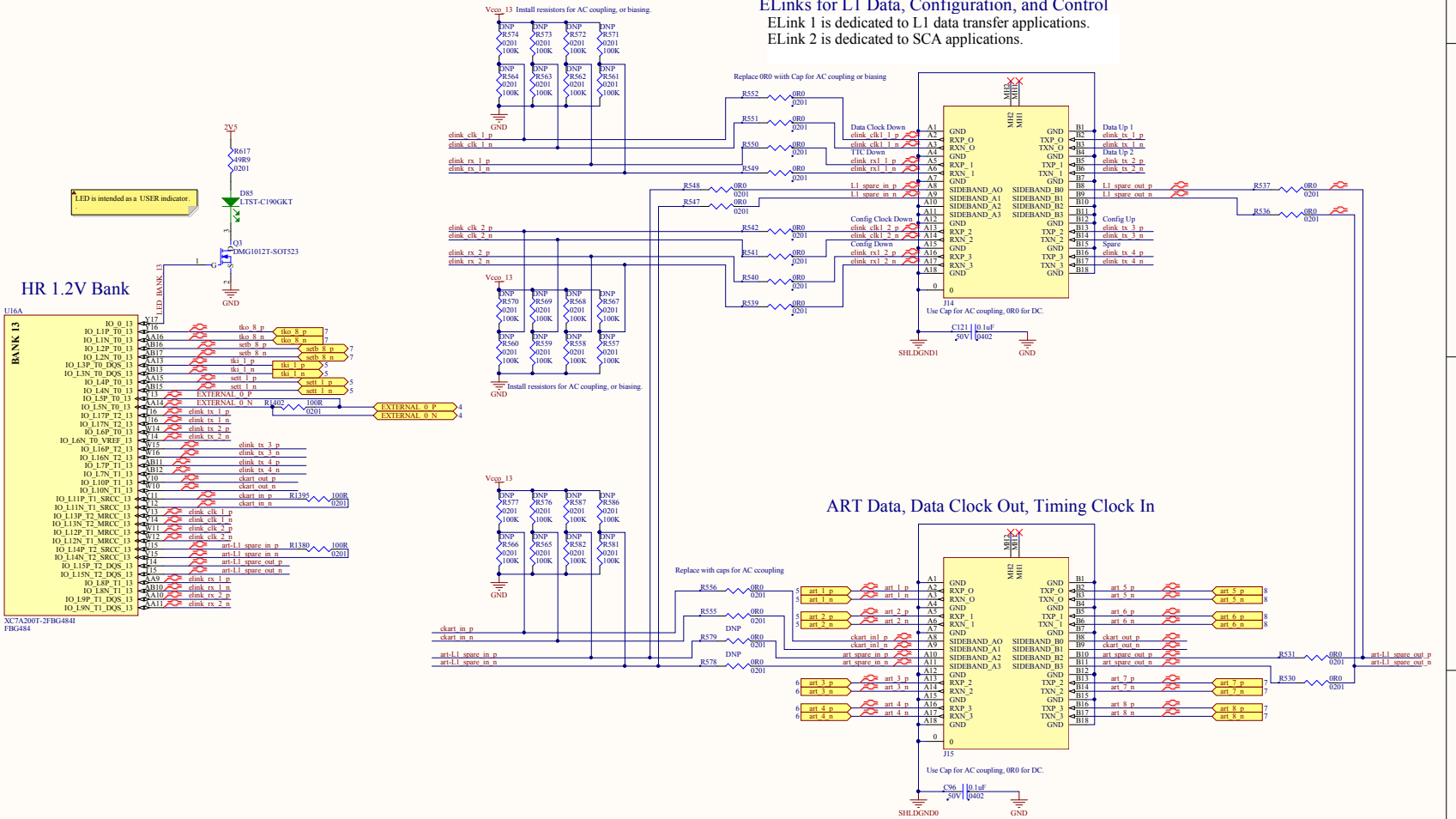
XADC SE Analog Mux for last 8 channels

Connect Vrefp and Vrefn to ground when using internal reference

DX_P and DX_N are the Anode and Cathode of an internal [to the FPGA] temperature sensing diode.

Title: 0301-MMFE-8_Bank0			University of Arizona 1118 E 4th St Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 11/11/2014	Time: 10:24:28 AM	Sheet 2 of 23	
File: C:\Pjcts\AltProj\0301-MMFE_8\0301-MMFE8-11-10-14tst2.DSN			Drawn By: William Hart

HR Bank 13:
Sufficient 1.2V Differential IO for 1.5 VMM.
All paired routing is 100 Ohm Differential and length matched TBD
All un-paired routing is 50 Ohm single ended.
Bank Voltage is at 1.2V.
Vref is handled internally by INTERNAL_VREF and pins are available for IO.
DCI is not available in HR banks.
It is unclear whether DIFF_TERM will work correctly.
All non-clock pairs may be pin-swapped as pairs within the bank.
Clock indicated nets are routed to clock input where possible.

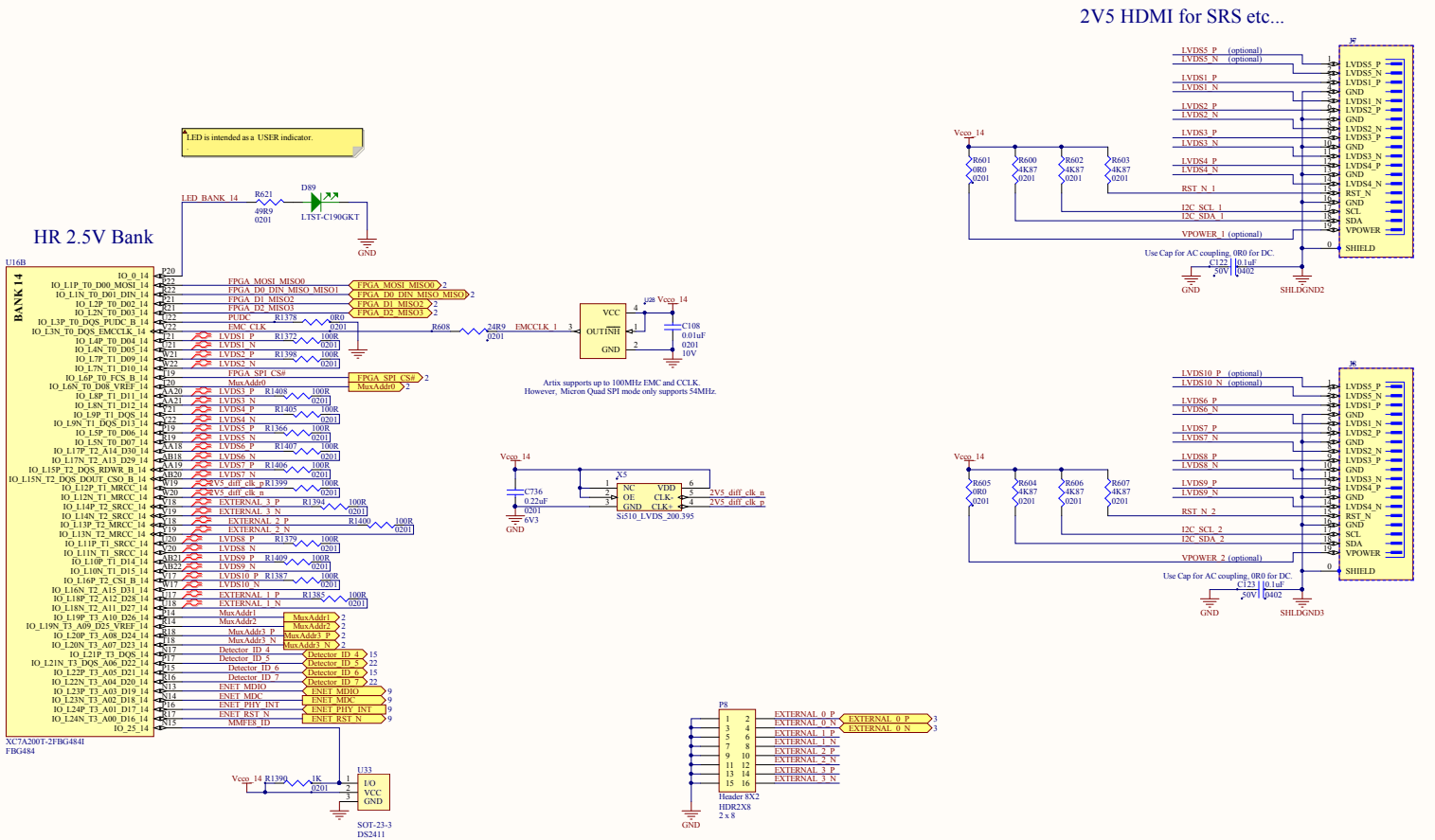


Title: 0301-MMFE-8_Bank13			University of Arizona 1118 E 4th St Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 11/11/2014	Time: 10:24:29 AM	Sheet 3 of 23	
File: C:\Picts\AltProt\0301-MMFE_8\0301-MMFE8-11-10-14tst3.SchDoc			Drawn By: William Hart mmSAS.SchDoc

HR Bank 14:
Sufficient 2.5V IO for Elink, 2x uHDMI, PHY, External IO.
Ethernet MD Interface:
Trace Impedence = 40 Ohms
Length match to < 385 mil
Spacing is 10 mil for short runs, 4 mils for parallel runs < 500 mils

All paired routing is 100 Ohm Differential and length matched TBD
All un-paired routing is 50 Ohm single ended.

Bank Voltage is at 2.5V, not adjustible due to PHY.
Vref is handled internally by INTERNAL_VREF and pins are available for IO.
DCI is not available in HR banks.
It is unclear whether DIFF_TERM will work correctly.
All non-clock pairs may be pin-swapped as pairs within the bank.
Clock indicated nets are routed to clock input where possible.



Title: 0301-MMFE-8_Bank16			University of Arizona 1118 E 4th St Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	
Date: 11/11/2014	Time: 10:24:29 AM	Sheet 4 of 23	billhart@email.arizona.edu
File: C:\Pjcts\AltProj\0301-MMFE_8\0301-MMFE8-11-10-14\sf-d			

HR Bank 15:
Sufficient 1.2V Differential IO for part of a VMM, 1 uHDMI, 2 Ext IO pairs.
8 Differential Analog Inputs
All paired routing is 100 Ohm Differential and length matched TBD
All un-paired routing is 50 Ohm single ended.
Bank Voltage is at 1.2V.
Vref is handled internally by INTERNAL_VREF and pins are available for IO.
DCI is not available in HR banks.
It is unclear whether DIFF_TERM will work correctly.
All non-clock pairs may be pin-swapped as pairs within the bank.
Clock indicated nets are routed to clock input where possible.

MMCX Coax Connectors for mounting and grounding.
Center is for signal monitor
Current location is mapped in Givi's drawing
Now have 8 available

LED is intended as a USER indicator.

HR 1.2V Bank

VMM2-1,2 Signals

Title:	0301-MMFE-8_Bank15
Size:	C
Engineer:	William Hart
Revision:	A
Date:	11/11/2014
Time:	10:24:29 AM
Sheet	5 of 23
File:	C:\Pjcts\AltProj\0301-MMFE_8\0301-MMFE8-11-10-14rbf5\0301-MMFE8-11-10-14rbf5.SchDoc

University of Arizona
1118 E 4th St
Tucson, Arizona 85721
billhart@email.arizona.edu

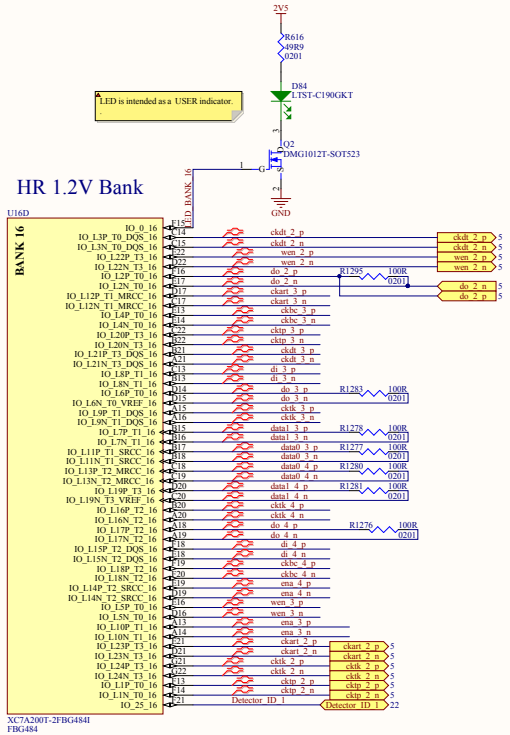
HR Bank 16:
Sufficient 1.2V Differential IO for 2 VMM, Clock to / from ART.
8 Differential Analog Inputs
All paired routing is 100 Ohm Differential and length matched TBD
All un-paired routing is 50 Ohm single ended.
Bank Voltage is at 1.2V.
Vref is handled internally by INTERNAL_VREF and pins are available for IO.
DCI is not available in HR banks.
It is unclear whether DIFF_TERM will work correctly.
All non-clock pairs may be pin-swapped as pairs within the bank.
Clock indicated nets are routed to clock input where possible.

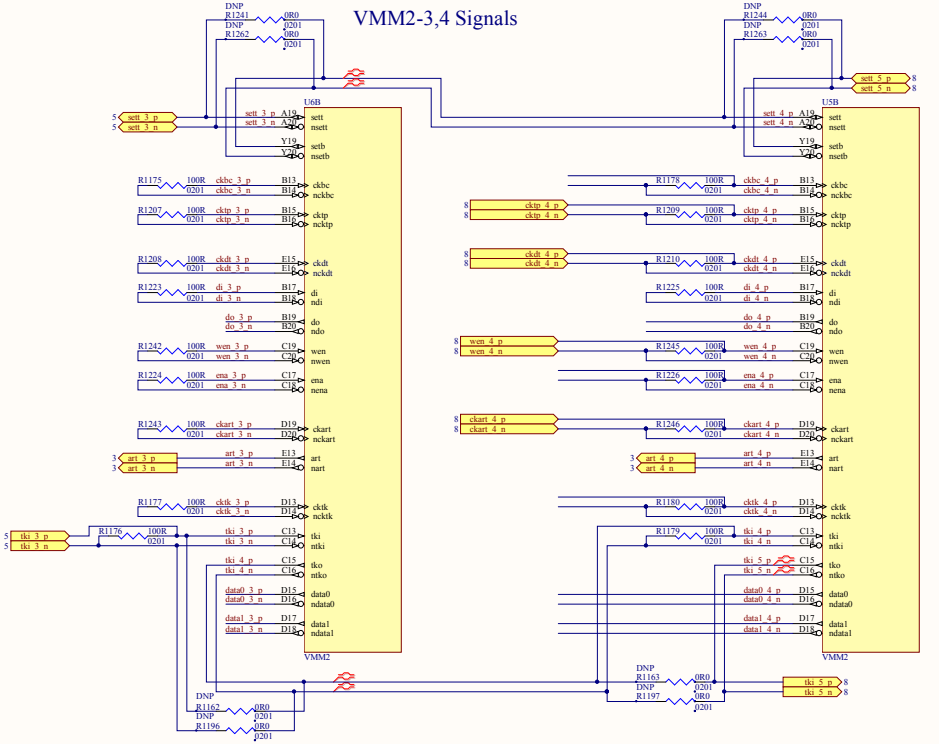
sett: ch0 neighbor trigger
ckbc: BC clock (timestamp Gray-code counter advance)
cktp: test pulse clock
di: configuration data input
do: configuration data output
tki: token input (in analog mode)
tko: token output (in analog mode)

ena: acquisition start/stop
ena high, wen low: acquisition is enabled
internally enabled after 40ns from ena high
in two-phase (analog) mode is acquisition
in continuous (digital) mode is acquisition and readout
ena low, wen low: in two-phase mode is readout
ena pulse, wen high: global reset (acquisition and registers)

wen: configuration enable
wen high: configuration mode
wen pulse: acquisition reset (also resets BC counter)

cktk: token clock
data0: flag and first data line (flag and address in analog mode)
data1: second data line
ckart: ART clock
art: ART output
ckdt: configuration (data input), data output and 6-bit ADC clock
setb: ch63 neighbor trigger





Title:	0301-MMFE-8_Bank12
Size:	C
Engineer:	William Hart
Revision:	A
Date:	11/11/2014
Time:	10:24:29 AM
Sheet	6 of 23
File:	C:\Pcts\AltProj\0301-MMFE_8\0301-MMFE8-11-10-14\sch6_Bank12.SchDoc

University of Arizona
1118 E 4th St
Tucson, Arizona 85721
billhart@email.arizona.edu

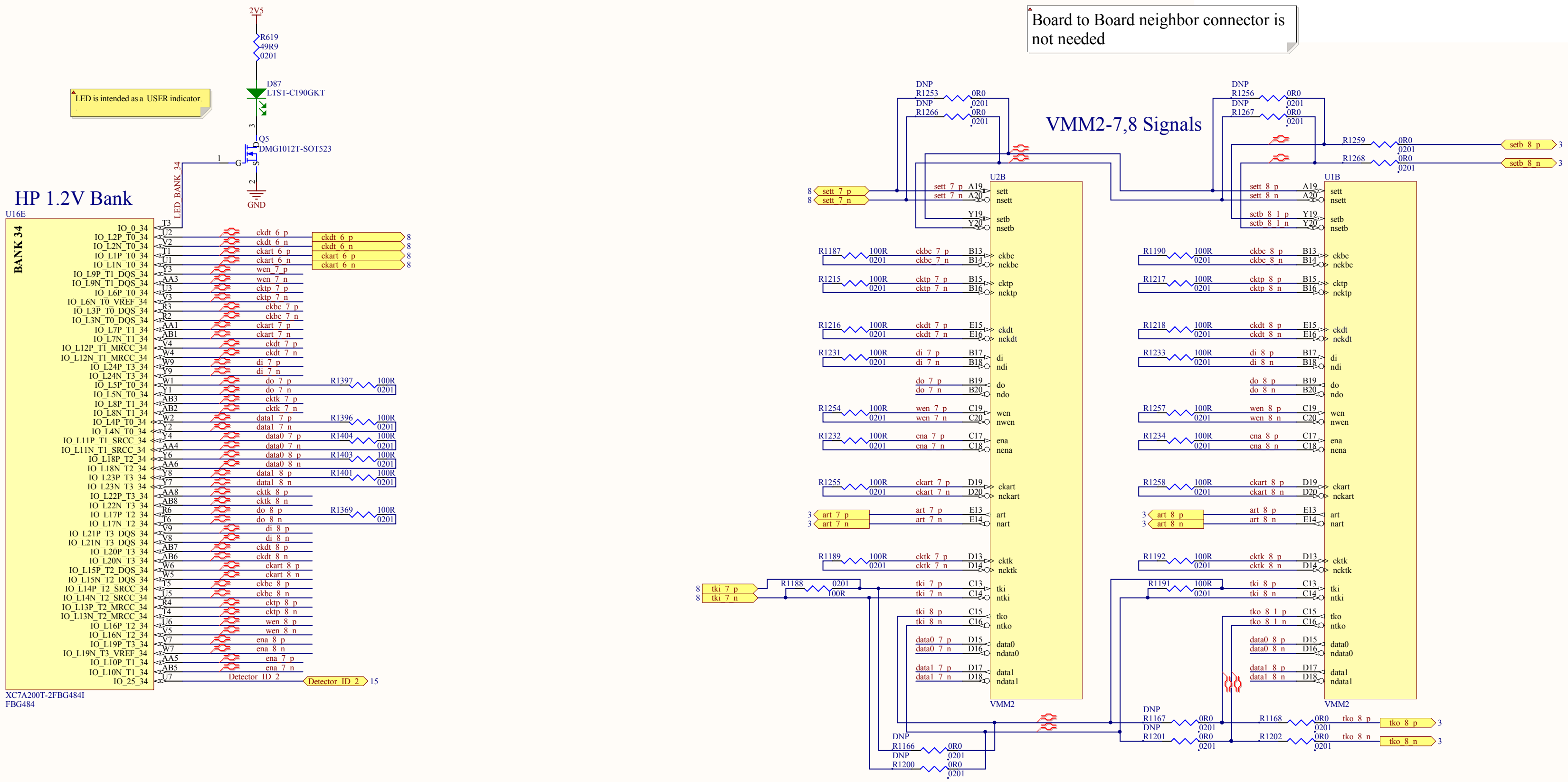
sett: ch0 neighbor trigger
ckbc: BC clock (timestamp Gray-code counter advance)
cktp: test pulse clock
di: configuration data input
do: configuration data output
tki: token input (in analog mode)
tko: token output (in analog mode)

ena: acquisition start/stop
ena high, wen low: acquisition is enabled
internally enabled after 40ns from ena high
in two-phase (analog) mode is acquisition
in continuous (digital) mode is acquisition and readout
ena low, wen low: in two-phase mode is readout
ena pulse, wen high: global reset (acquisition and registers)

wen: configuration enable
wen high: configuration mode
wen pulse: acquisition reset (also resets BC counter)

cktk: token clock
data0: flag and first data line (flag and address in analog mode)
data1: second data line
ckart: ART clock
art: ART output
ckdt: configuration (data input), data output and 6-bit ADC clock
setb: ch63 neighbor trigger

HR Bank 35:
Sufficient 1.2V Differential IO for 2 VMM's.
All paired routing is 100 Ohm Differential and length matched TBD
All un-paired routing is 50 Ohm single ended.
Bank Voltage is at 1.2V.
Vref is handled internally by INTERNAL_VREF and pins are available for IO.
DCI is available in HP banks.
It is unclear whether DIFF_TERM will work correctly.
All non-clock pairs may be pin-swapped as pairs within the bank.
Clock indicated nets are routed to clock input where possible.



Title: *0301-MMFE-8_Bank33*

Size: C Engineer: William Hart Revision: A

Date: 11/11/2014 Time: 10:24:29 AM Sheet 7 of 23

File: C:\Pjcts\AltProj\0301-MMFE_8\0301-MMFE8-11-10-14tst\7 Drawn By: William Hart ...vmm78.SchDoc

University of Arizona
1118 E 4th St
Tucson, Arizona 85721
billhart@email.arizona.edu

HR Bank 34:
Sufficient 1.2V Differential IO for 2 VMM's.
All paired routing is 100 Ohm Differential and length matched TBD
All un-paired routing is 50 Ohm single ended.
Bank Voltage is at 1.2V.
Vref is handled internally by INTERNAL_VREF and pins are available for IO.
DCI is available in HP banks.
It is unclear whether DIFF_TERM will work correctly.
All non-clock pairs may be pin-swapped as pairs within the bank.
Clock indicated nets are routed to clock input where possible.

sett: ch0 neighbor trigger
ckbc: BC clock (timestamp Gray-code counter advance)
cktp: test pulse clock
di: configuration data input
do: configuration data output
tki: token input (in analog mode)
tko: token output (in analog mode)

ena: acquisition start/stop
ena high, wen low: acquisition is enabled
internally enabled after 40ns from ena high
in two-phase (analog) mode is acquisition
in continuous (digital) mode is acquisition and readout
ena low, wen low: in two-phase mode is readout
ena pulse, wen high: global reset (acquisition and registers)

wen: configuration enable
wen high: configuration mode
wen pulse: acquisition reset (also resets BC counter)

cktk: token clock
data0: flag and first data line (flag and address in analog mode)
data1: second data line
ckart: ART clock
art: ART output
ckdt: configuration (data input), data output and 6-bit ADC clock
setb: ch63 neighbor trigger

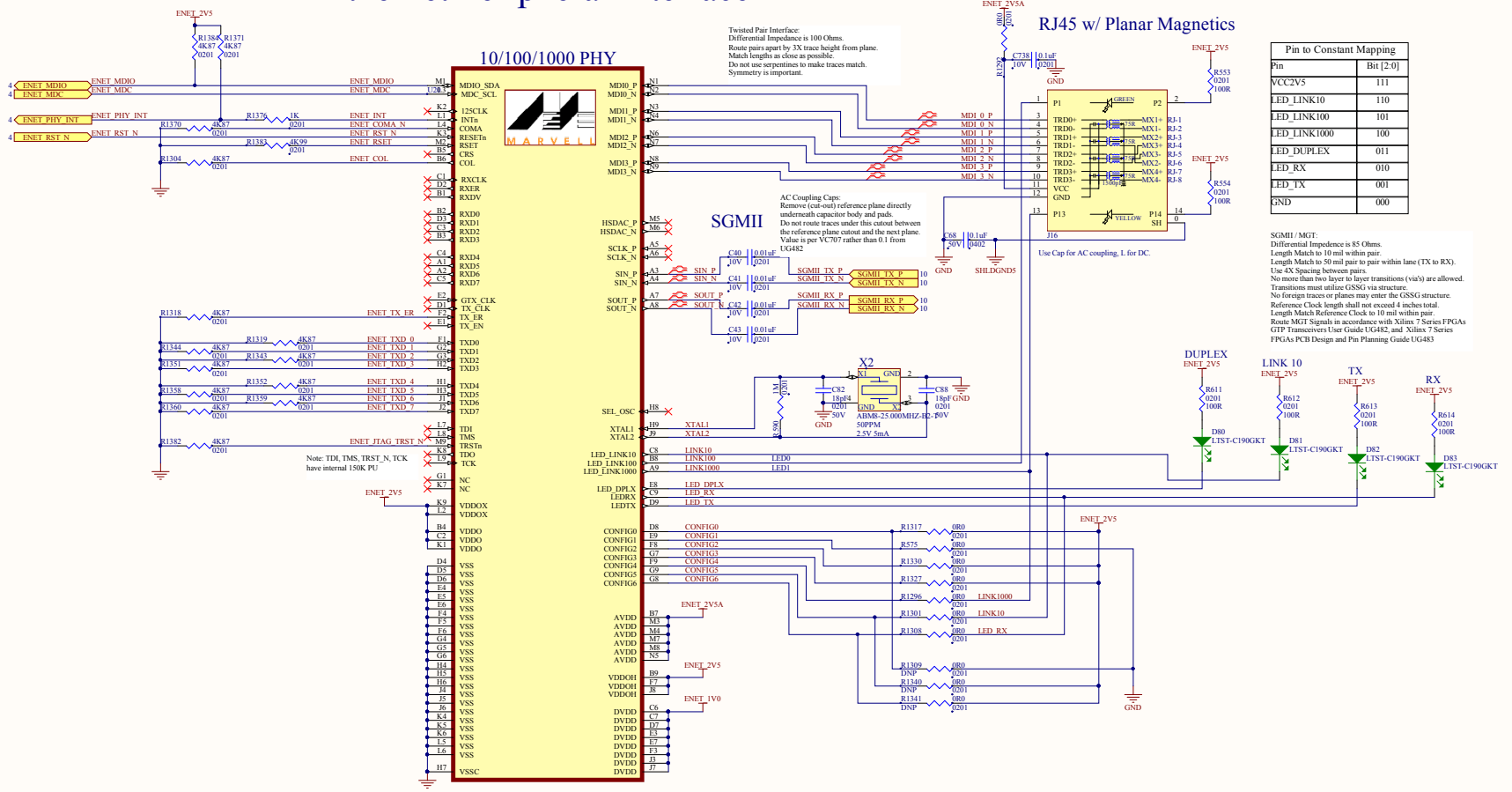
HP 1.2V Bank

VMM2-5,6 Signals

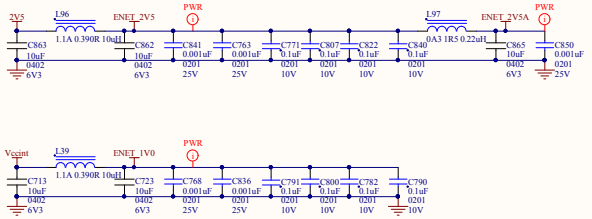
LED is intended as a USER indicator.

Title:	0301-MMFE-8_Bank34	University of Arizona	
Size: C	Engineer: William Hart	Revision: A	1118 E 4th St Tucson, Arizona 85721
Date: 11/11/2014	Time: 10:24:30 AM	Sheet 8 of 23	billhart@email.arizona.edu
File: C:\Pjcts\AltProj\0301-MMFE_8\0301-MMFE8-11-10-14st8\0301-MMFE8-11-10-14st8.SchDoc			

Ethernet Peripheral Interface



Pin to Constant Mapping	
Pin	Bit [2:0]
VCC2V5	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
GND	000



Pin	Bit[2]	Bit[1]	Bit[0]		
CFG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	111	PHYAddr "00111". Don't advertise the PAUSE bit
CFG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	
CFG2	ANEG[3]	ANEG[2]	ANEG[1]	111	Auto-Neg en, advertise all caps; prefer slave. Auto crossover enabled. 125 CLK option disabled.
CFG3	ANEG[0]	ENA_XC	DIS_125	111	
CFG4	HWCFG_MD[2]	HWCFG_MD[1]	HWCFG_MD[0]	100	SGMII w/o Clock w/ Auto-Neg to Cu. 0100 Fiber/copper auto-detect disabled. Sleep mode disabled.
CFG5	DIS_FC	DIS_SLEEP	HWCFG_MD[3]	110	
CFG6	0 = MDC/MDIO 1 = TWSI	0 = INT Active HIGH 1 = INT Active LOW	0 = 50 OHM SGMII 1 = 75 OHM SGMII	010	MDC/MDIO selected. Active LOW interrupt 50Ohm SGMII / Fiber option.

VCC2V5	111
GND	000
VCC2V5	111
VCC2V5	111
LED_LINK1000	100
LED_LINK10	110
LED_RX	010

Title: *0301-MMFE-8_Ethernet*

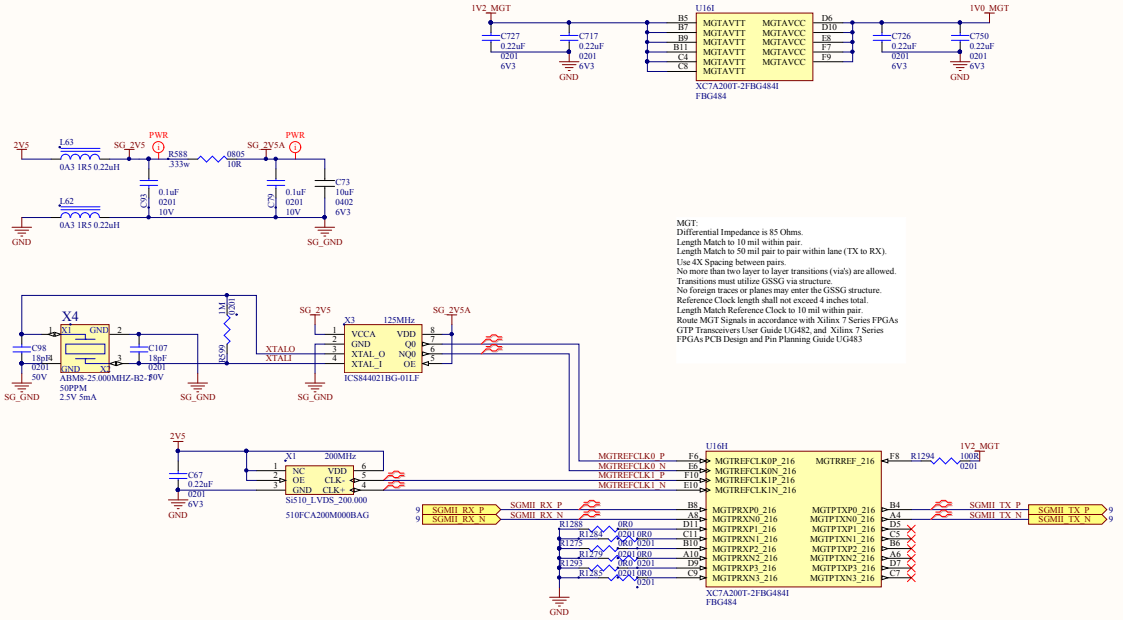
University of Arizona
1118 E 4th St
Tucson, Arizona 85721

Size: C | Engineer: William Hart | Revision: A

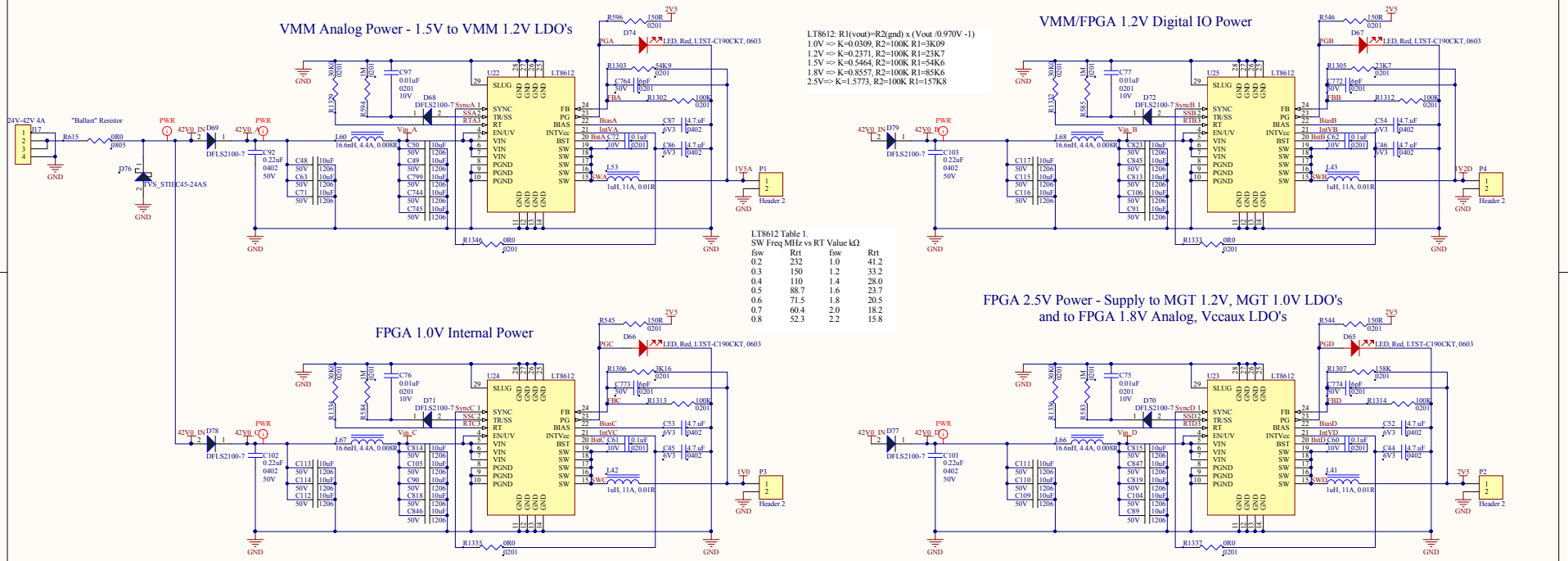
Date: 11/11/2014 Time: 10:24:30 AM | Sheet 9 of 23

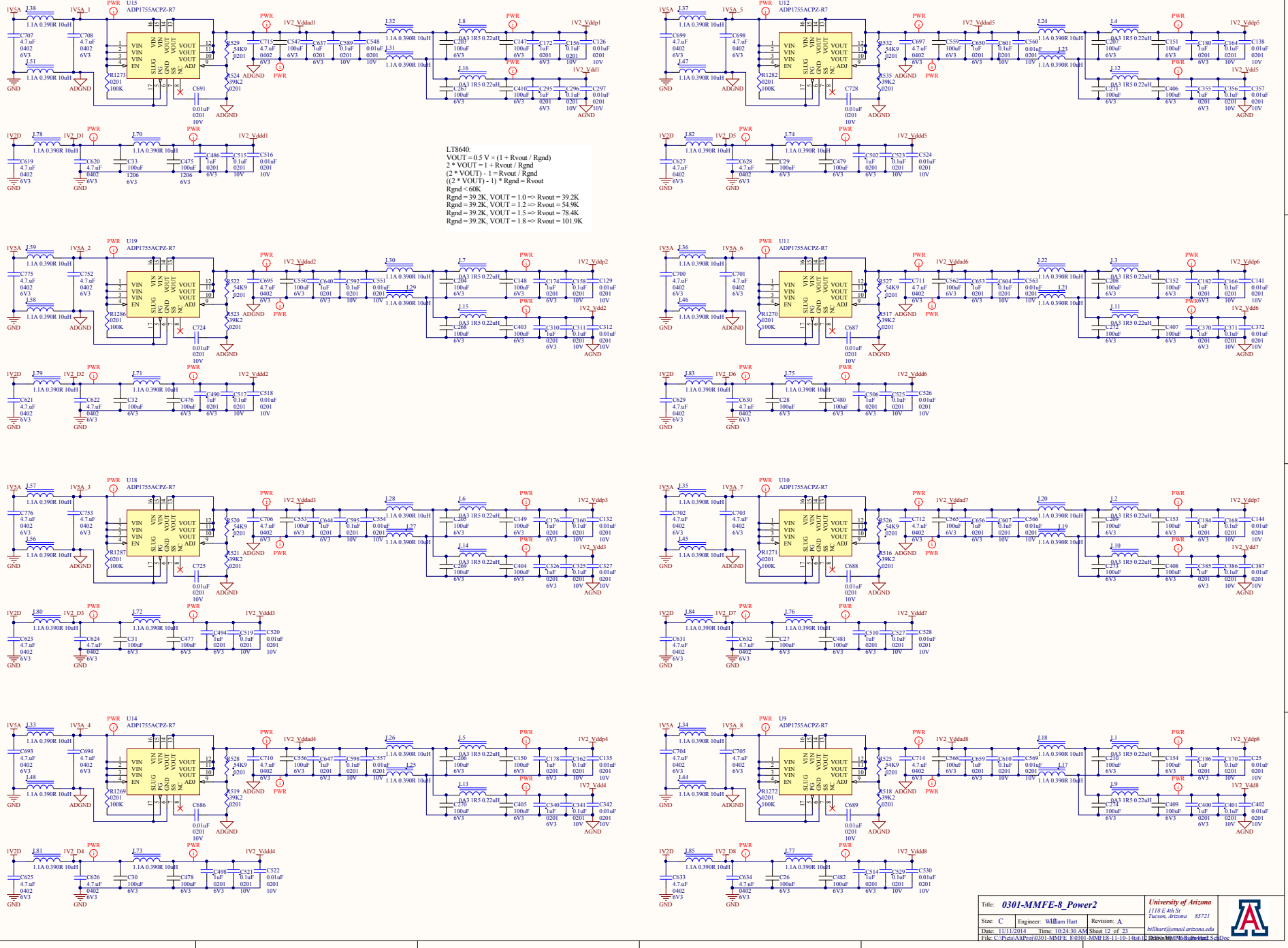
File: C:\Pjcts\AltPro\0301-MMFE_8.03\0301-MMFE8-11-10-14\sf9_Ethernet.SchDoc

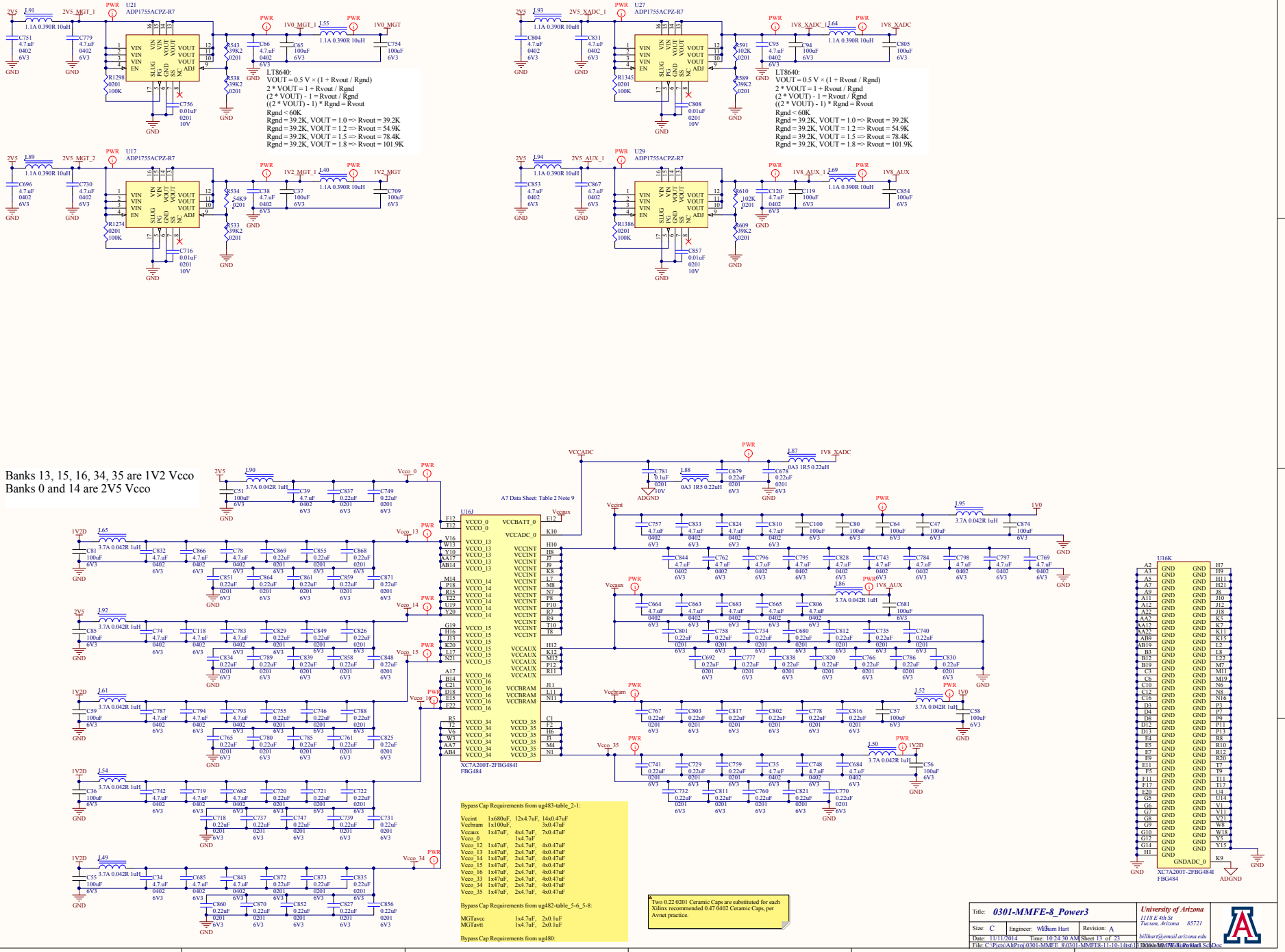
billhart@email.arizona.edu

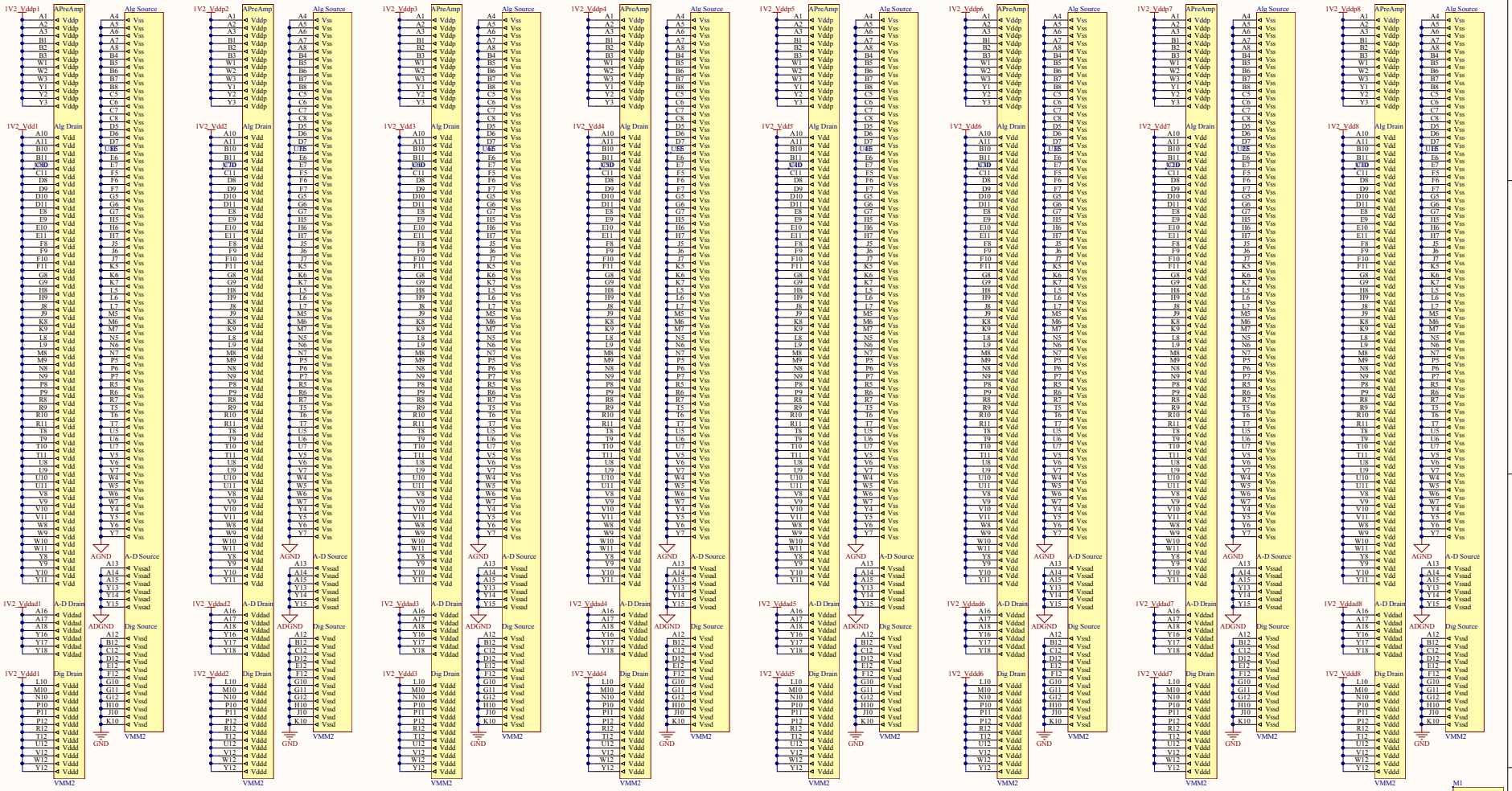


Title: 0301-MMFE-8_MGT			University of Arizona 1118 E 4th St Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 11/11/2014 Time: 10:24:30 AM	Sheet 10 of 23		
File: C:\Pjcts\AltProj\0301-MMFE_8.0301-MMFE8-11-10-14tst\[D:\Pjcts\AltProj\0301-MMFE_8.0301-MMFE8-11-10-14tst\MGT.SchDoc			

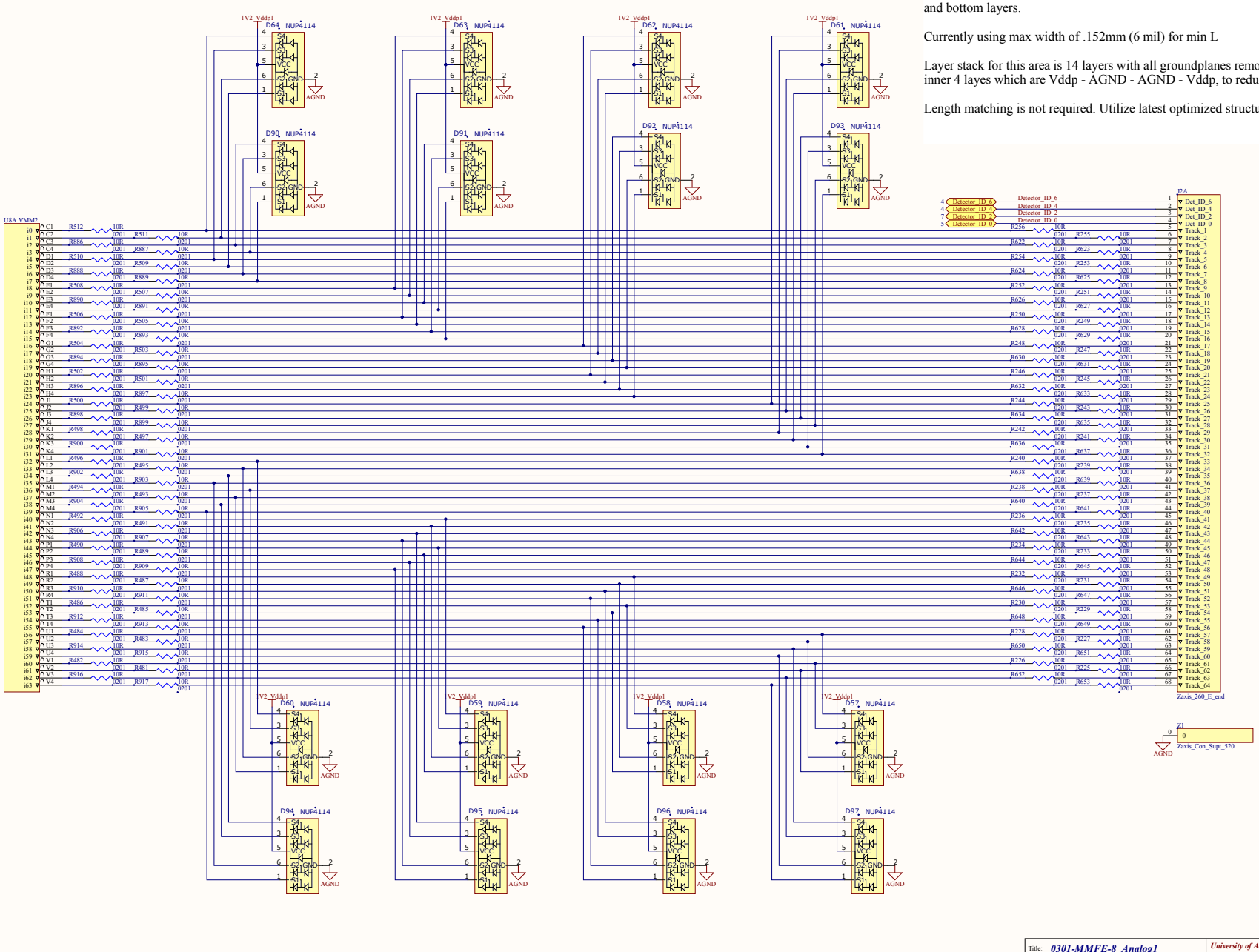

VMM Analog Power - 1.5V to VMM 1.2V LDO's
VMM/FPGA 1.2V Digital IO Power
FPGA 1.0V Internal Power
FPGA 2.5V Power - Supply to MGT 1.2V, MGT 1.0V LDO's and to FPGA 1.8V Analog, Vccaux LDO's
LT8612: R1(vout)=R2(gnd) x (Vout /0.970V -1)
1.0V => K=0.0309, R2=100K R1=3K09
1.2V => K=0.2371, R2=100K R1=23K7
1.5V => K=0.5464, R2=100K R1=54K6
1.8V => K=0.8557, R2=100K R1=85K6
2.5V=> K=1.5773, R2=100K R1=157K8
LT8612 Table 1.
SW Freq MHz vs RT Value kΩ
fsw Rrt fsw Rrt
0.2 232 1.0 41.2
0.3 150 1.2 33.2
0.4 110 1.4 28.0
0.5 88.7 1.6 23.7
0.6 71.5 1.8 20.5
0.7 60.4 2.0 18.2
0.8 52.3 2.2 15.8
Power Estimates:
LT8612 #1 1.5Vanlg
Ianlg18 = 8*0.427ianlg12 (via ADP1755ACPZ-1-8)
= 3.4A + losses
LT8612 #2 1.2Vdgtl
Idgtl12 = 8*.150Aidig12
+ 0.621Aicco12 = 1.821A + losses
LT8612 #3 1.0Vfpga
Ifpga10 = 3.15Aiccint
+ 0.100Aicebram = 3.65A + losses
LT8612 #4 2.5Vfpga
Ifpga25 = 0.621Aicco25
+ 0.511Aimgtavcc10 (viaADP1755ACPZ-9)
+ .36Aimgtavtt (viaADP1755ACPZ-10)
+ 0.32iccaux
=1.8A + losses
Note:
Iccauxq (Vaux Quiescent) = 7mA
1.8V LVCMOS25 or 33 = 2-24mA per pin
1.2V SSTL / HSTL 8mA per pin max
When laying out power, please route point to point first, with trace width sufficient to carry the required current.
Pours or splits can then be instantiated afterwards, without fear of islands or choke points.
This is especially crittical for FPGA power distribution, and makes verification easier.
Ground Referance for Probes
ESR:
DF = tan(phi) = ESR / Xc = 0.1 for CC
ESR = DF * Xc = DF / (2*pi*f*C) = Xc / Q = tan(phi) * Xc
Z = (ESR^2 + (Xl-Xc)^2)^0.5
Fr = 1 / (2*pi*(L*C)^0.5)
Spec for Al and Film caps @100KHz
Spec for Al and Tant @120Hz
ESR = Rdielc(0-3MHz) + Rmetal(30-300MHz)
ESR2 = ESR1 * (f2/f1)^0.5
ESR calculations for ceramic caps use DF of 10%, meas'd @ 120 Hz, used @ 1MHz = 0.005Ohms worst case.
Title: 0301-MMFE-8_Power1
University of Arizona
1118 E 4th St
Tucson, Arizona 85721
Size: C
Engineer: William Hart
Revision: A
billhart@email.arizona.edu
Date: 11/11/2014 Time: 10:24:30 AM Sheet 11 of 23
File: C:\Pjcts\AltProj\0301-MMFE_8\0301-MMFE8-11-10-14sch\0301-MMFE8-Power1.SchDoc


U15
ADP1755ACPZ-R7
U12
ADP1755ACPZ-R7
U19
ADP1755ACPZ-R7
U11
ADP1755ACPZ-R7
U18
ADP1755ACPZ-R7
U10
ADP1755ACPZ-R7
U14
ADP1755ACPZ-R7
U9
ADP1755ACPZ-R7
1V5A_1
1V5A_5
1V5A_2
1V5A_6
1V5A_3
1V5A_7
1V5A_4
1V5A_8
1V2_Vddad1
1V2_Vddad5
1V2_Vddad2
1V2_Vddad6
1V2_Vddad3
1V2_Vddad7
1V2_Vddad4
1V2_Vddad8
1V2_Vddp1
1V2_Vddp5
1V2_Vddp2
1V2_Vddp6
1V2_Vddp3
1V2_Vddp7
1V2_Vddp4
1V2_Vddp8
1V2_Vdd1
1V2_Vdd5
1V2_Vdd2
1V2_Vdd6
1V2_Vdd3
1V2_Vdd7
1V2_Vdd4
1V2_Vdd8
1V2D
1V2_D1
1V2_D5
1V2_D2
1V2_D6
1V2_D3
1V2_D7
1V2_D4
1V2_D8
PWR
GND
ADGND
AGND
LT8640:
VOUT = 0.5 V × (1 + Rvout / Rgnd)
2 * VOUT = 1 + Rvout / Rgnd
(2 * VOUT) - 1 = Rvout / Rgnd
((2 * VOUT) - 1) * Rgnd = Rvout
Rgnd < 60K
Rgnd = 39.2K, VOUT = 1.0 => Rvout = 39.2K
Rgnd = 39.2K, VOUT = 1.2 => Rvout = 54.9K
Rgnd = 39.2K, VOUT = 1.5 => Rvout = 78.4K
Rgnd = 39.2K, VOUT = 1.8 => Rvout = 101.9K
Title: 0301-MMFE-8_Power2
University of Arizona
1118 E 4th St
Tucson, Arizona 85721
billhart@email.arizona.edu
Size: C
Engineer: William Hart
Revision: A
Date: 11/11/2014
Time: 10:24:30 AM
Sheet 12 of 23
File: C:\Pjcts\AltProj\0301-MMFE_8\0301-MMFE8-11-10-14tst\[0301-MMFE8_Power2.SchDoc]

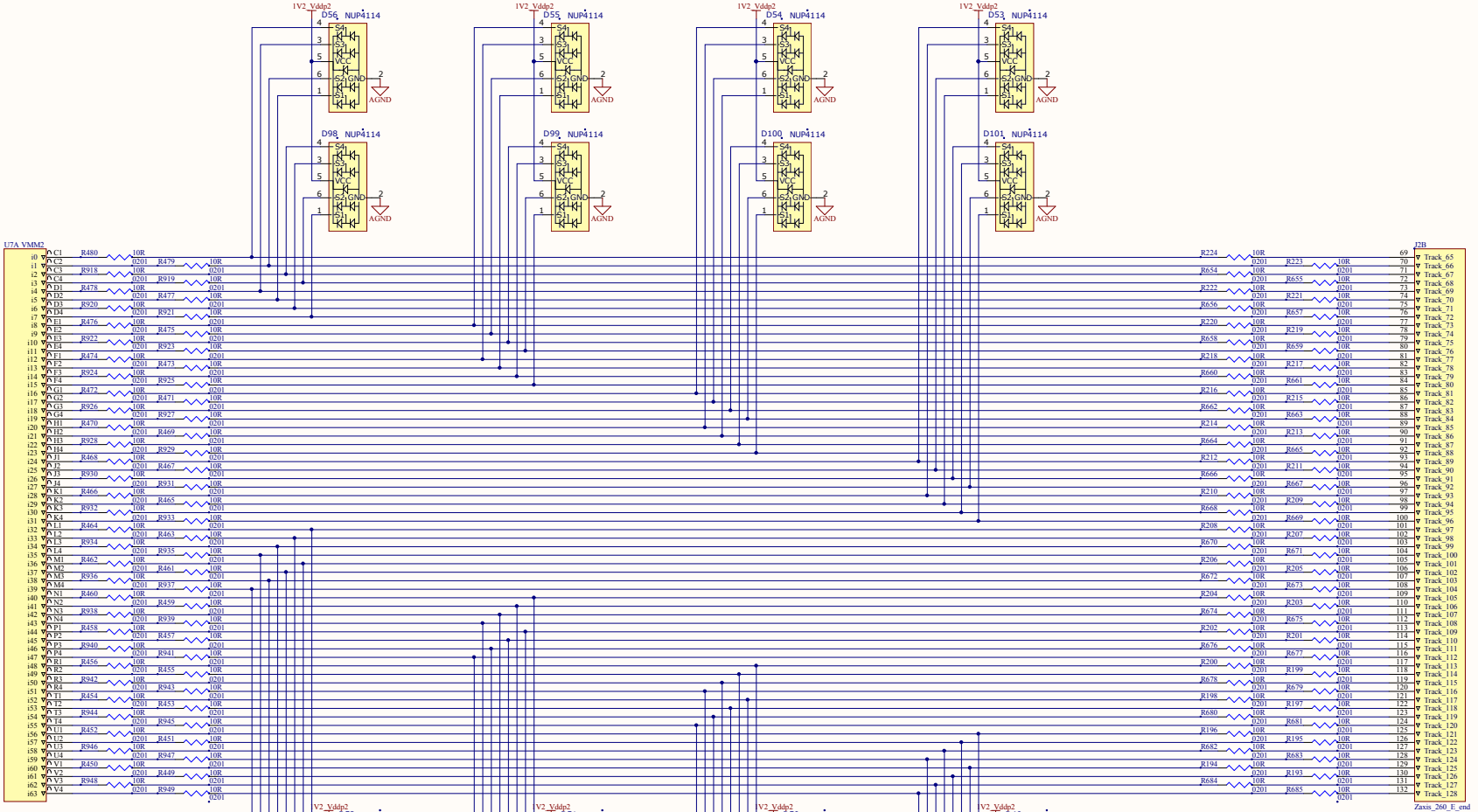

U21 ADP1755ACPZ-R7
2V5
2V5_MGT_1
1V0_MGT_1
1V0_MGT
L91
L55
1.1A 0.390R 10uH
LT8640:
VOUT = 0.5 V × (1 + Rvout / Rgnd)
2 * VOUT = 1 + Rvout / Rgnd
(2 * VOUT) - 1 = Rvout / Rgnd
((2 * VOUT) - 1) * Rgnd = Rvout
Rgnd < 60K
Rgnd = 39.2K, VOUT = 1.0 => Rvout = 39.2K
Rgnd = 39.2K, VOUT = 1.2 => Rvout = 54.9K
Rgnd = 39.2K, VOUT = 1.5 => Rvout = 78.4K
Rgnd = 39.2K, VOUT = 1.8 => Rvout = 101.9K
U27 ADP1755ACPZ-R7
2V5_XADC_1
1V8_XADC_1
1V8_XADC
L93
L64
U17 ADP1755ACPZ-R7
2V5_MGT_2
1V2_MGT_1
1V2_MGT
L89
L40
U29 ADP1755ACPZ-R7
2V5_AUX_1
1V8_AUX_1
1V8_AUX
L94
L69
Banks 13, 15, 16, 34, 35 are 1V2 Vcco
Banks 0 and 14 are 2V5 Vcco
A7 Data Sheet: Table 2 Note 9
U16J
XC7A200T-2FBG484I
FBG484
VCCADC
Vccaux
Vccint
Vccbram
Vcco_0
Vcco_13
Vcco_14
Vcco_15
Vcco_16
Vcco_34
Vcco_35
L90
L87
L88
L86
L95
L52
L50
L65
L92
L61
L54
L49
3.7A 0.042R 1uH
0A3 1R5 0.22uH
U16K
GNDADC_0
ADGND
Bypass Cap Requirements from ug483-table_2-1:
Vccint 1x680uF, 12x4.7uF, 14x0.47uF
Vccbram 1x100uF, 3x0.47uF
Vccaux 1x47uF, 4x4.7uF, 7x0.47uF
Vcco_0 1x4.7uF
Vcco_12 1x47uF, 2x4.7uF, 4x0.47uF
Vcco_13 1x47uF, 2x4.7uF, 4x0.47uF
Vcco_14 1x47uF, 2x4.7uF, 4x0.47uF
Vcco_15 1x47uF, 2x4.7uF, 4x0.47uF
Vcco_16 1x47uF, 2x4.7uF, 4x0.47uF
Vcco_33 1x47uF, 2x4.7uF, 4x0.47uF
Vcco_34 1x47uF, 2x4.7uF, 4x0.47uF
Vcco_35 1x47uF, 2x4.7uF, 4x0.47uF
Bypass Cap Requirements from ug482-table_5-6_5-8:
MGTavcc 1x4.7uF, 2x0.1uF
MGTavtt 1x4.7uF, 2x0.1uF
Bypass Cap Requirements from ug480:
Two 0.22 0201 Ceramic Caps are substituted for each Xilinx recommended 0.47 0402 Ceramic Caps, per Avnet practice.
Title: 0301-MMFE-8_Power3
University of Arizona
1118 E 4th St
Tucson, Arizona 85721
billhart@email.arizona.edu
Size: C
Engineer: William Hart
Revision: A
Date: 11/11/2014 Time: 10:24:30 AM Sheet 13 of 23
File: C:\Pjcts\AltPro\0301-MMFE_8\0301-MMFE8-11-10-14stuff\0301-MMFE8_Power3.SchDoc



Title: 0301-MMFE-8_Power4			University of Arizona 1118 E 4th St Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	
Date: 11/11/2014	Time: 10:24:31 AM	Sheet 14 of 23	billhart@email.arizona.edu
File: C:\Pjcts\AltProj\0301-MMFE_8\0301-MMFE8-11-10-14stf.IPJ			

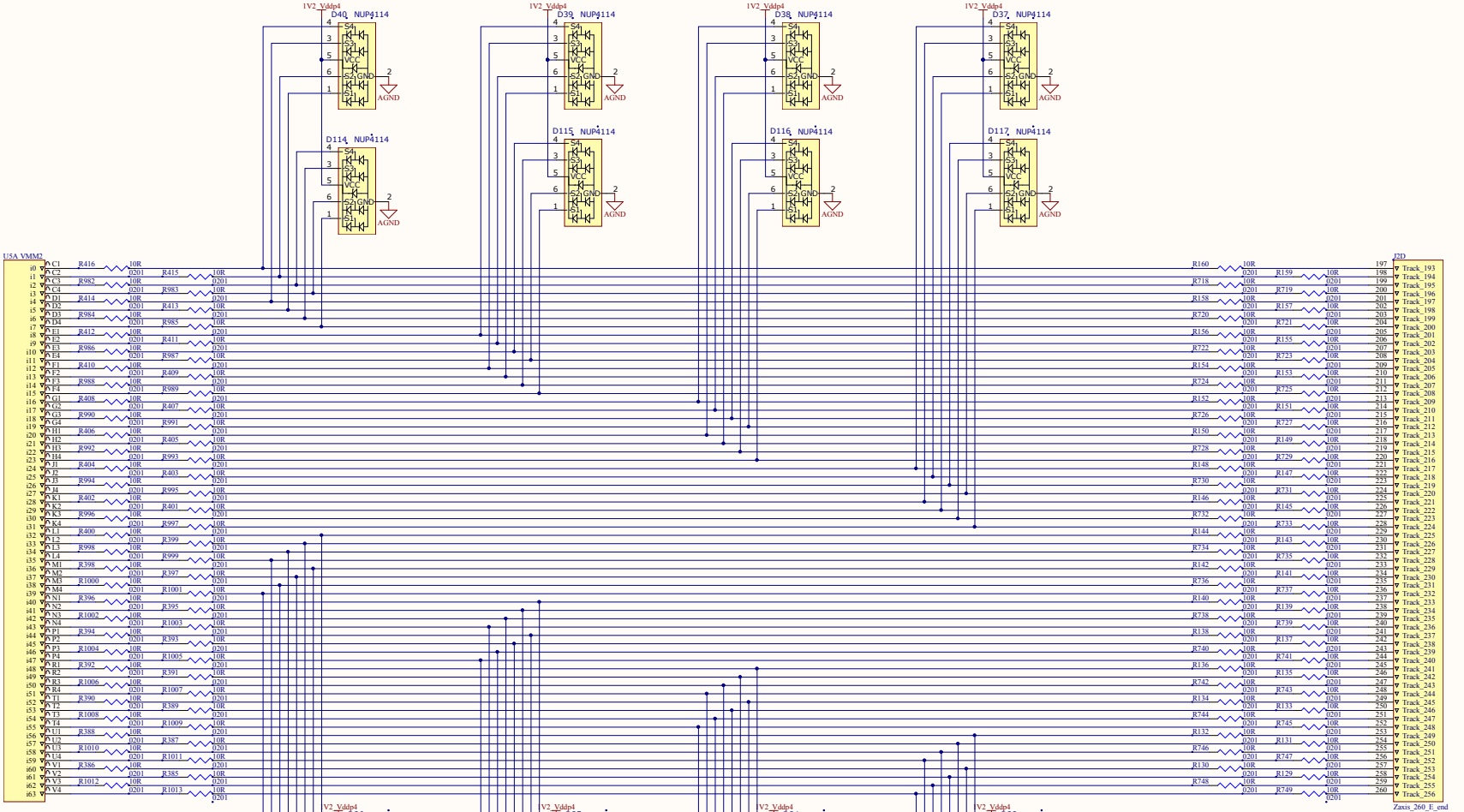

Analog Input Routing:
Traces from input connectors (Zaxis, Zebra, etc) are routed alternately to top and bottom layers.
Currently using max width of .152mm (6 mil) for min L
Layer stack for this area is 14 layers with all groundplanes removed except for inner 4 laves which are Vddp - AGND - AGND - Vddp, to reduce capacitance.
Length matching is not required. Utilize latest optimized structures.
USA_VMM2
J2A
Zaxis_260_E_end
Zaxis_Con_Supt_520
Title: 0301-MMFE-8_Analog1
University of Arizona
1118 E 4th St
Tucson, Arizona 85721
billhart@email.arizona.edu
Size: C
Engineer: William Hart
Revision: A
Date: 11/11/2014 Time: 10:24:31 AM
Sheet 15 of 23

Title: *0301-MMFE-8_Power5*			*University of Arizona*
Size: C	Engineer: William Hart	Revision: A	*1118 E 4th St Tucson, Arizona 85721*
Date: 11/11/2014	Time: 10:24:31 AM	Sheet 15 of 24	*billhart@email.arizona.edu*
File: C:\Pjcts\AltProj\0301-MMFE_8\0301-MMFE8-11-10-14stf.[illegible]Power5.SchDoc			

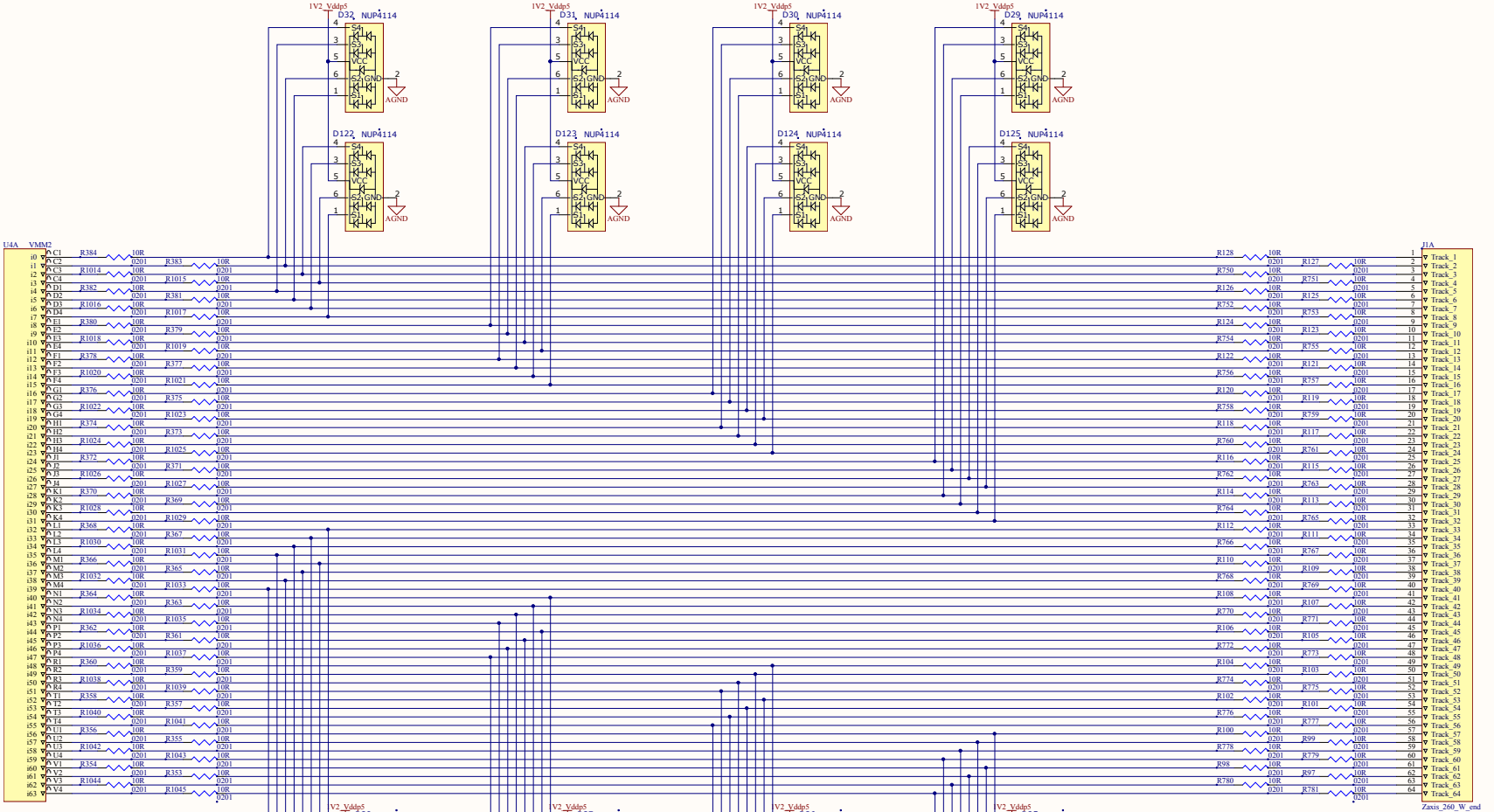


Title: 0301-MMFE-8_Analog2			University of Arizona 1118 E 4th St Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 11/11/2014	Time: 10:24:32 AM	Sheet 16 of 23	
File: C:\Pjcts\AltPro\0301-MMFE_8\0301-MMFE8-11-10-14stf.[illegible]			

Title: 0301-MMFE-8_Analog3			University of Arizona 1118 E 4th St Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 11/11/2014	Time: 10:24:32 AM	Sheet 17 of 23	
File: C:\Pjcts\AltPro\0301-MMFE_8\0301-MMFE8-11-10-14st\[0301-MMFE8_Analog3.SchDoc			

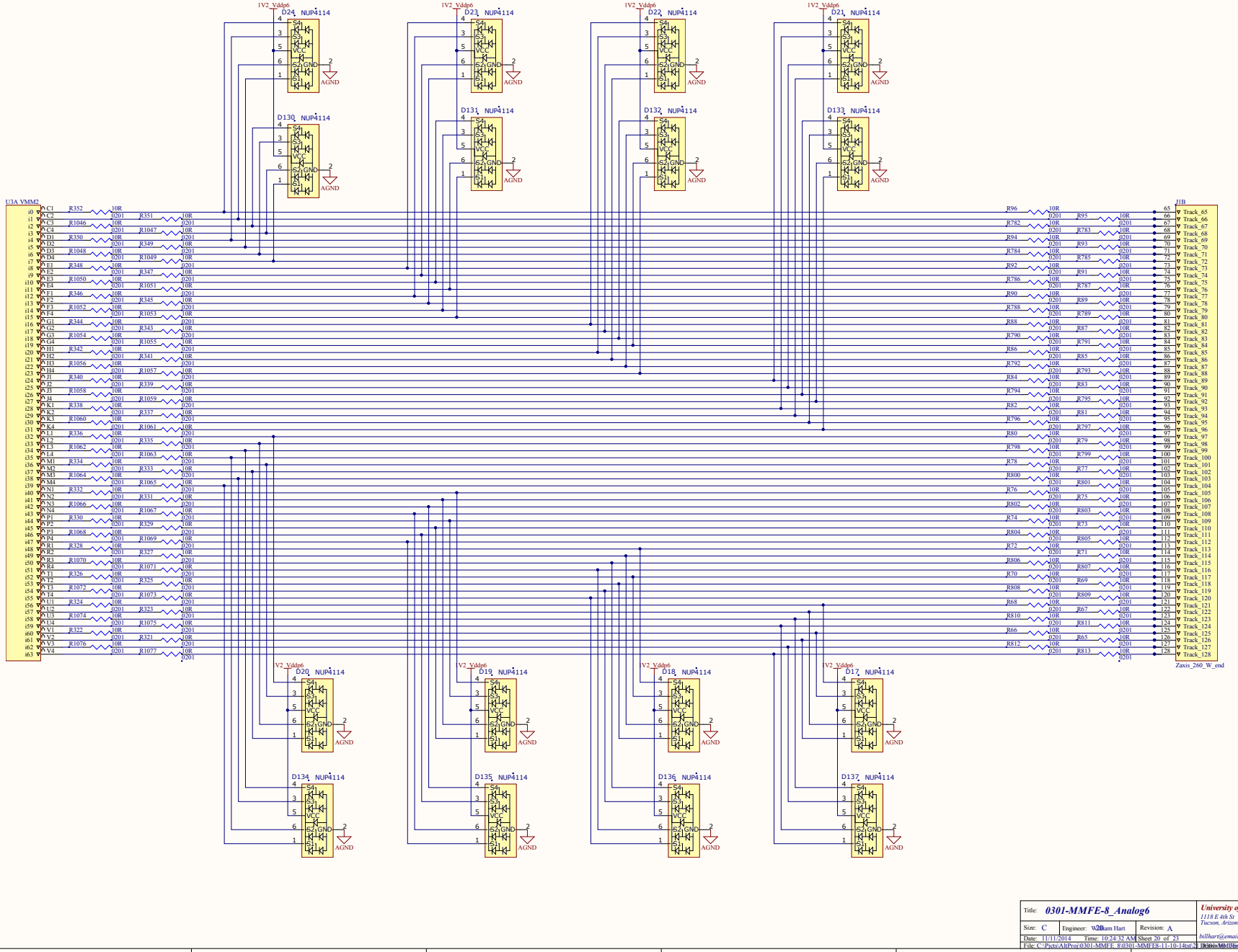


Title: 0301-MMFE-8_Analog4			University of Arizona 1118 E 4th St Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 11/11/2014	Time: 10:24:32 AM	Sheet 18 of 23	
File: C:\Pjcts\AltPro\0301-MMFE_8\0301-MMFE8-11-10-14st\[Page18.SchDoc]			



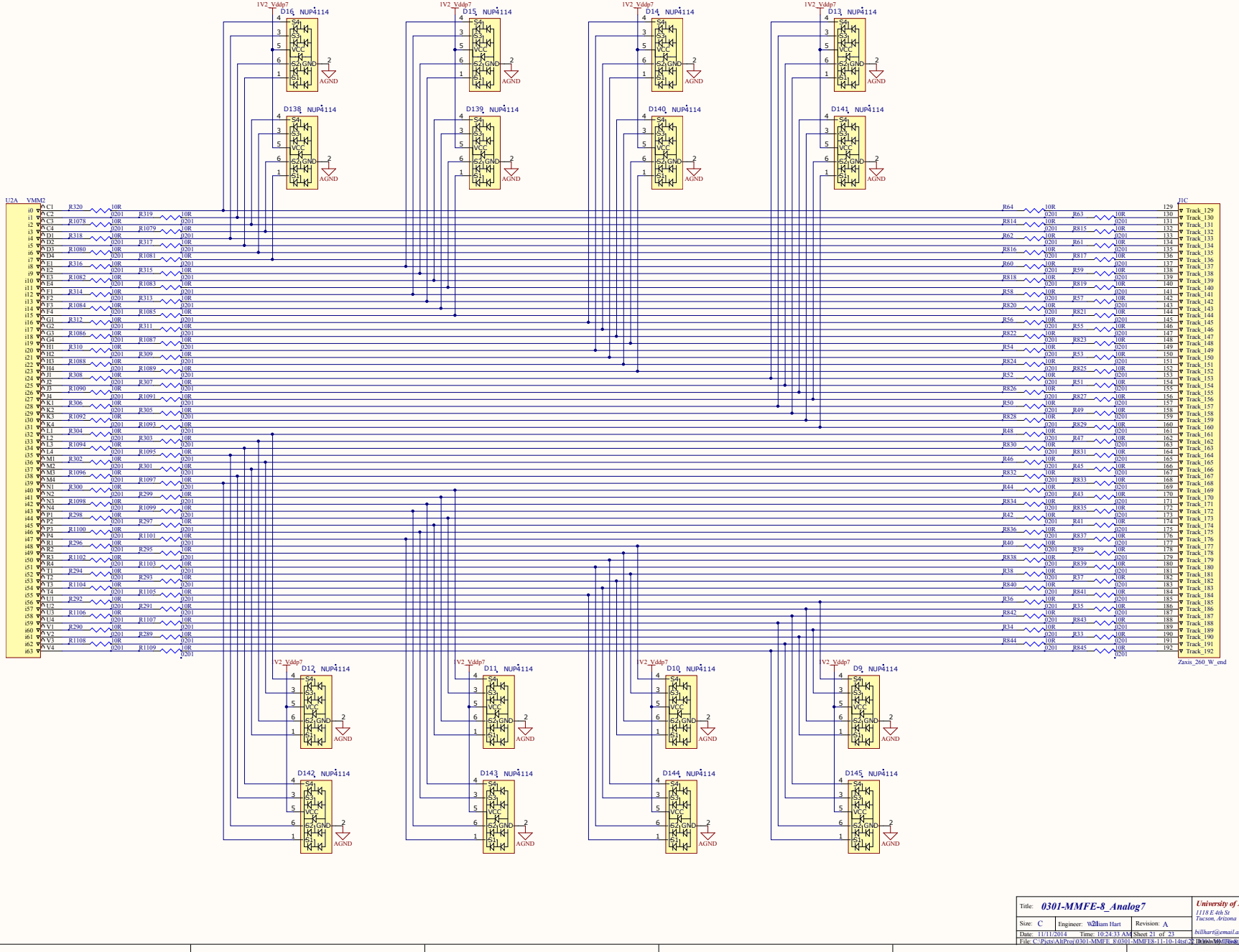
Title:	0301-MMFE-8_Analog5
Size:	C
Engineer:	William Hart
Revision:	A
Date:	11/11/2014
Time:	10:24:32 AM
Sheet	19 of 23
File:	C:\Pjcts\AltProj\0301-MMFE_8\0301-MMFE8-11-10-14stC2D.SchDoc

University of Arizona
1118 E 4th St
Tucson, Arizona 85721
billhart@email.arizona.edu

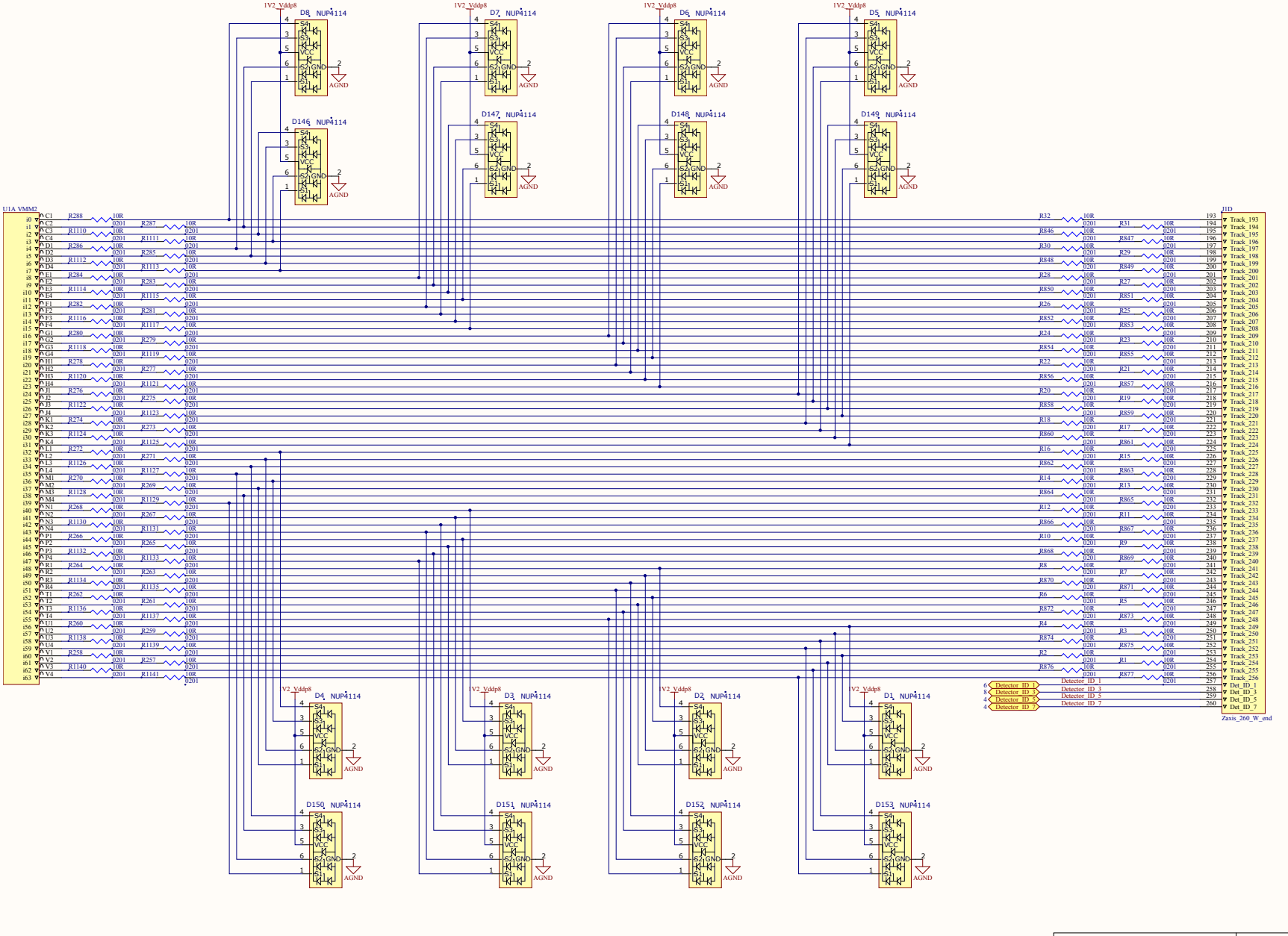


Title:	0301-MMFE-8_Analog6		
Size: C	Engineer: William Hart	Revision: A	
Date: 11/11/2014	Time: 10:24:32 AM	Sheet 20 of 23	
File: C:\Pjcts\AltProj\0301-MMFE_8\0301-MMFE8-11-10-14st2.PrjPcb\0301-MMFE8_Analog6.SchDoc			

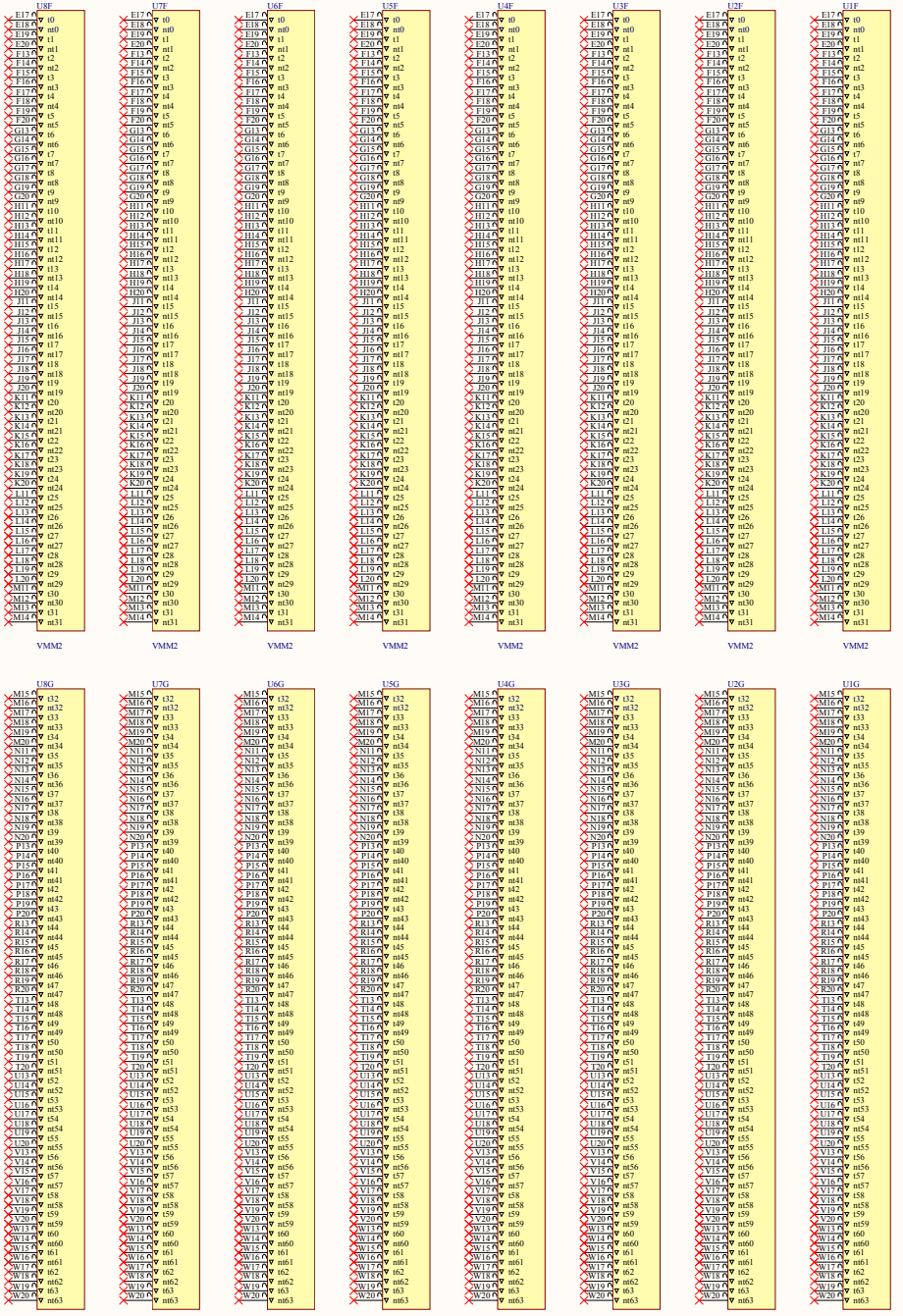
University of Arizona
1118 E 4th St
Tucson, Arizona 85721
billhart@email.arizona.edu



Title: 0301-MMFE-8_Analog7			University of Arizona 1118 E 4th St Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 11/11/2014	Time: 10:24:33 AM	Sheet 21 of 23	
File: C:\Pjcts\AltProj\0301-MMFE_8\0301-MMFE8-11-10-14stc2.PrjPcb\0301-MMFE8-Analog7.SchDoc			



Title: *0301-MMFE-8_Analog8*			*University of Arizona*
Size: C	Engineer: William Hart	Revision: A	*1118 E 4th St Tucson, Arizona 85721*
Date: 11/11/2014	Time: 10:24:33 AM	Sheet 22 of 23	*billhart@email.arizona.edu*
File: C:\Pjcts\AltPro\0301-MMFE_8\0301-MMFE8-11-10-14st2.PrjPcb			



Title: *0301-MMFE-8_VMM_ttp*			*University of Arizona*
			1118 E 4th St
			Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	*billhart@email.arizona.edu*
Date: 11/11/2014	Time: 10:24:33 AM	Sheet 23 of 23	
File: C:\Picts\AltPro\0301-MMFE_8\0301-MMFE8-11-10-14st2.DSN			