

Xilinx Artix 7 - Micro Megas Front End - 8 VMM Card

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**THE UNIVERSITY
OF ARIZONA**

Physics Department

0301-MMFE-8 A

11/11/2014

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Services / NRE

PCB1
ASSY_PCB_Layout
PCB layout / 5 boards

PCB2
ASSY_PCB_Man
PCB only

PCB3
ASSY_PCB_Assy
PCB assembly

Accessories

CBL1
CBL-miniSAS-36
miniSAS 4i 36 ckts

CBL2
CBL-miniSAS-36
miniSAS 4i 36 ckts

Title: 0301-MMFE-8_Title			University of Arizona 1118 E 4th St Tucson, Arizona 85721		
Size: B	Engineer: William Hart	Revision: A	billhart@email.arizona.edu		
Date: 11/11/2014	Time: 10:24:28 AM	Sheet 1 of 23	C:\Pjcts\A\Proj\0301-MMFE_8\0301-MMFE8-11-10-14\st1		
File: C:\Pjcts\A\Proj\0301-MMFE_8\0301-MMFE8-11-10-14\st1			0301-MMFE-8_VMM_SchDoc		

Bank 0:
 Contains Configuration and Analog - Digital Converter functionality.
 Bank Voltage is 2V5.

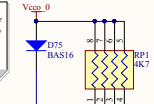
N25Q256A11EF840x is 256Mb Quad SPI FLASH, used to configure the FPGA. XC7A200T requires 77,845,216b stream.

Since Flash does not typically run at 2V5, translators must be used.

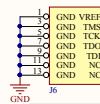
All paired routing is 100 Ohm Differential and length matched TBD
 All un-paired routing is 50 Ohm single ended.

JTAG

Diode is used to prevent any current backflow from a Parallel IV cable connection. Diode is probably no longer required. Pullups are probably no longer required either



Use Digilent JTAG HS1.2 Programming Cable Part #410-249P-KIT in place of installing JTAG SMT2 Surface-Mount Programming Module.

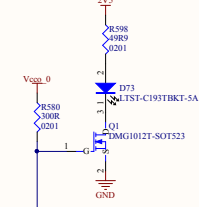


SPI Flash ROM Signal / Pin Equivalences
 C = Clock = Input
 DQ0 = Serial Data In = Input
 DQ1 = Serial Data Out = Output
 S, N = CS = Input
 For Quad, DQ pins are BiDirectional...

Per Impact Help:
 Micron (Nanmemory)
 N25Q 3.3V (1) 32Mb - 256Mb Kintex™-7, Artix™-7
 N25Q 1.8V (1) 32Mb - 256Mb Kintex-7, Virtex-7
 1 For Nanmemory N25Q: Top, Bottom, and Uniform block sectors are supported.

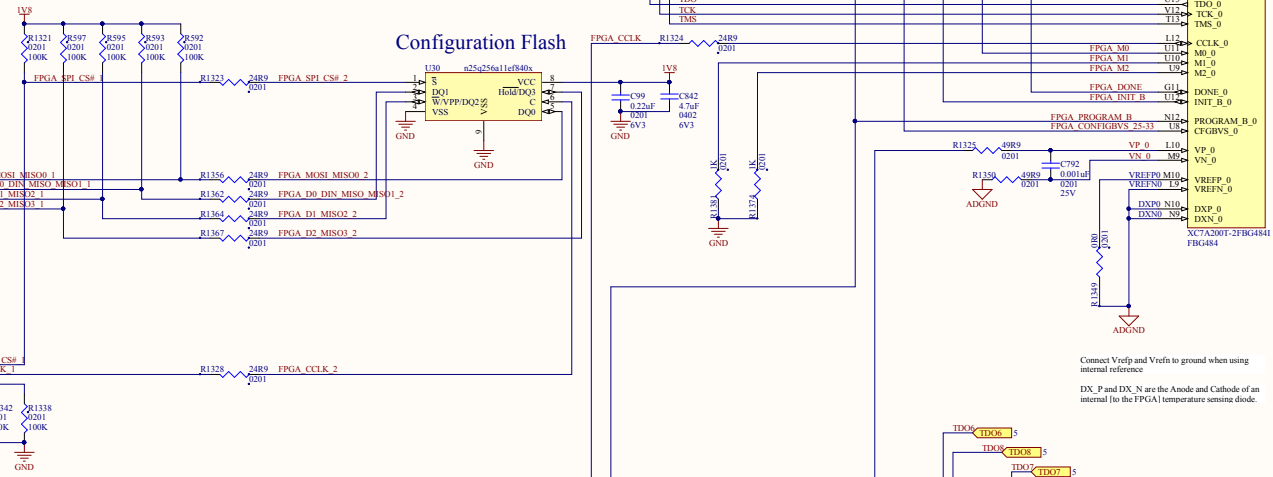
Place serial termination resistor close to the FPGA

Configuration Done

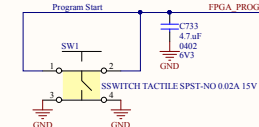


Please Refer to XAPP586

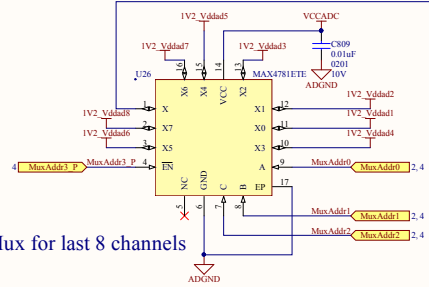
Configuration Flash



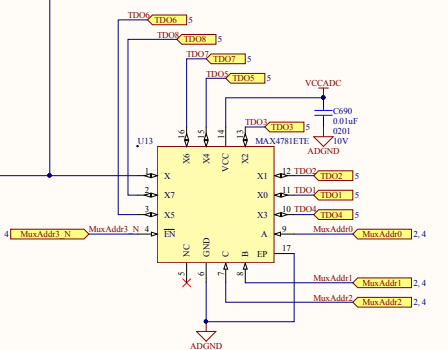
Reconfigure Switch



XADC SE Analog Mux for last 8 channels



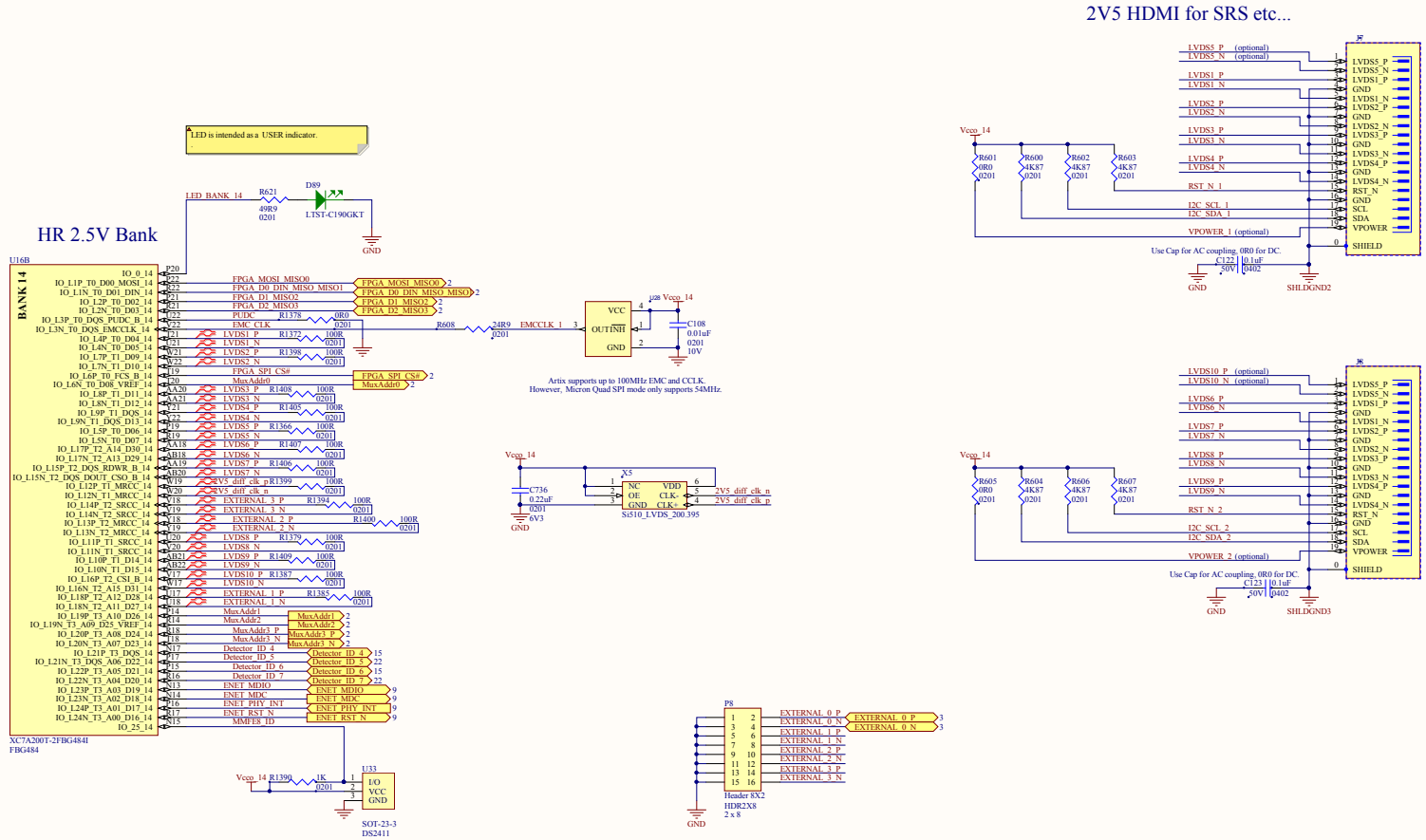
XADC SE Analog Mux for last 8 channels



HR Bank 14:
 Sufficient 2.5V IO for Elink, 2x uHDMI, PHY, External IO.
 Ethernet MD Interface:
 Trace Impedance = 40 Ohms
 Length match to < 385 mil
 Spacing is 10 mil for short runs, 4 mils for parallel runs < 500 mils

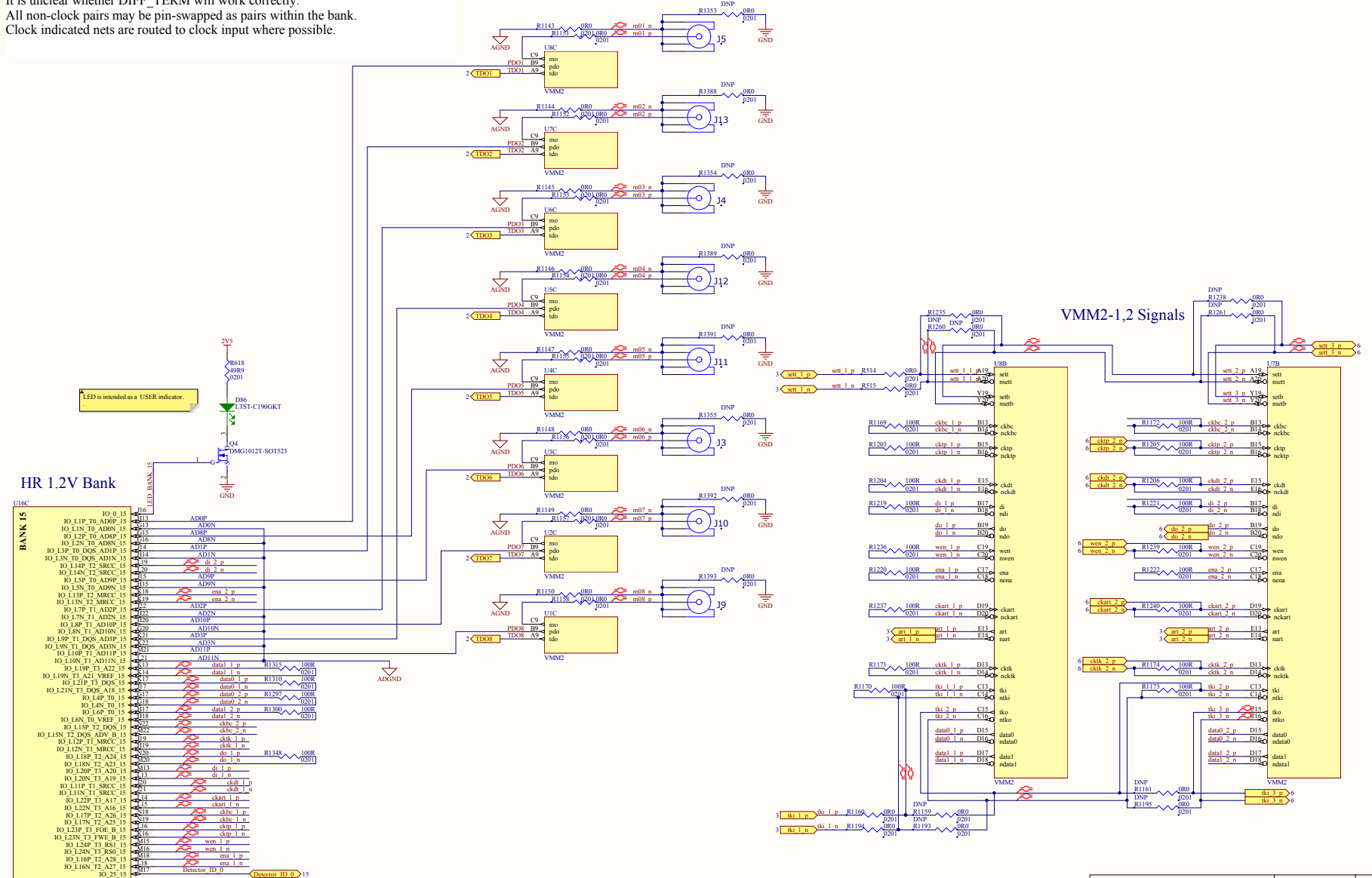
All paired routing is 100 Ohm Differential and length matched TBD
 All un-paired routing is 50 Ohm single ended.

Bank Voltage is at 2.5V, not adjustable due to PHY.
 Vref is handled internally by INTERNAL_VREF and pins are available for IO.
 DCI is not available in HR banks.
 It is unclear whether DIFF_TERM will work correctly.
 All non-clock pairs may be pin-swapped as pairs within the bank.
 Clock indicated nets are routed to clock input where possible.



HR Bank 15:
 Sufficient 1.2V Differential IO for part of a VMM, 1 uHDMI, 2 Ext IO pairs.
 8 Differential Analog Inputs
 All paired routing is 100 Ohm Differential and length matched TBD
 All un-paired routing is 50 Ohm single ended.
 Bank Voltage is at 1.2V.
 Vref is handled internally by INTERNAL_VREF and pins are available for IO.
 DCI is not available in HR banks.
 It is unclear whether DIFF_TERM will work correctly.
 All non-clock pairs may be pin-swapped as pairs within the bank.
 Clock indicated nets are routed to clock input where possible.

MMMX Coax Connectors for mounting and grounding.
 Center is for signal minimize.
 Current location is mapped in Giv's drawing.
 Now have 8 available.



HR Bank 16:
 Sufficient 1.2V Differential IO for 2 VMM, Clock to / from ART.
 8 Differential Analog Inputs
 All paired routing is 100 Ohm Differential and length matched TBD
 All un-paired routing is 50 Ohm single ended.
 Bank Voltage is at 1.2V.
 Vref is handled internally by INTERNAL_VREF and pins are available for IO.
 DCI is not available in HR banks.
 It is unclear whether DIFF_TERM will work correctly.
 All non-clock pairs may be pin-swapped as pairs within the bank.
 Clock indicated nets are routed to clock input where possible.

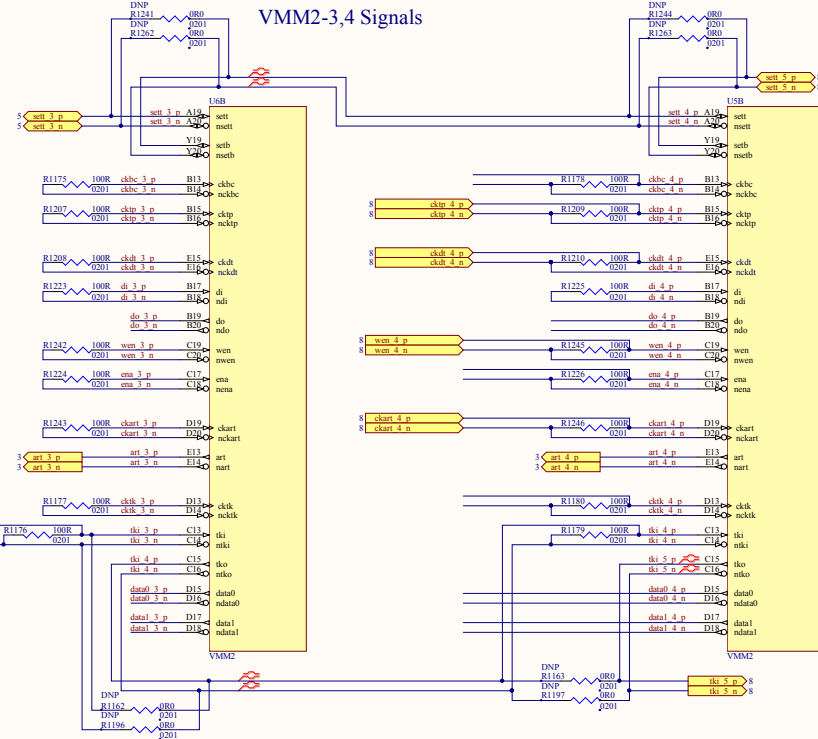
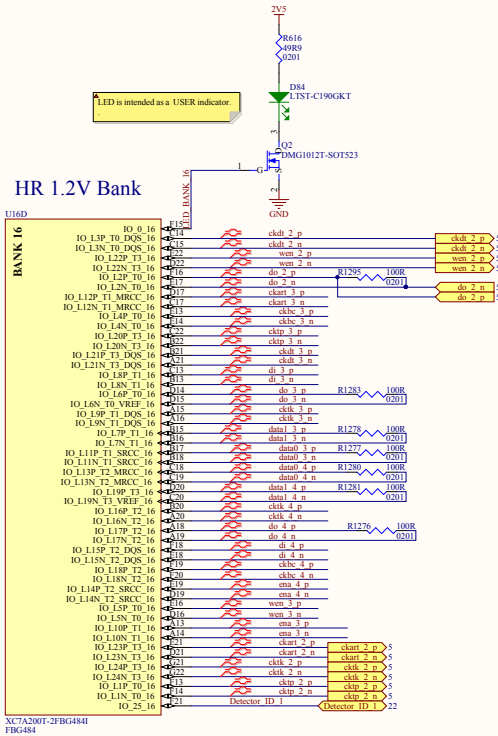
```

set:    ch0 neighbor trigger
ckbc:   BC clock (timestamp Gray-code counter advance)
cktp:   test pulse clock
ckrt:   configuration data input
do:     configuration data output
tki:    token input (in analog mode)
tko:    token output (in analog mode)

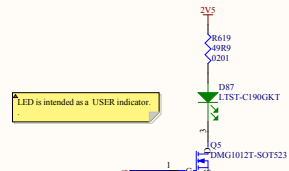
ena:    acquisition start/stop
ena high, wen low:  acquisition is enabled
                    internally enabled after 40ns from ena high
                    in two-phase (analog) mode is acquisition
                    in continuous (digital) mode is acquisition and readout
ena low, wen low:  in two-phase mode is readout
ena pulse, wen high: global reset (acquisition and registers)

wen:    configuration enable
wen high: configuration mode
wen pulse: acquisition reset (also resets BC counter)

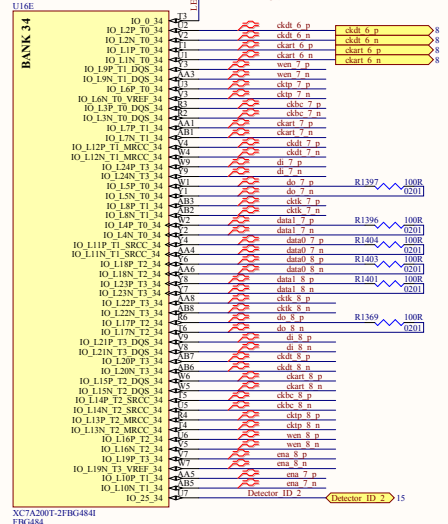
cktk:   token clock
data0:  flag and first data line (flag and address in analog mode)
data1:  second data line
ckart:  ART clock
art:    ART output
ckdt:   configuration (data input), data output and 6-bit ADC clock
ckb63:  neighbor trigger
  
```



HP Bank 35
 Sufficient 1.2V Differential IO for 2 VMMS.
 All paired routing is 100 Ohm Differential and length matched TMD
 All unpaired routing is 50 Ohm single-ended.
 Bank Voltage is at 1.2V
 User is handled internally by INTERNAL_VREF and pins are available for IO.
 DCI is available in HP banks.
 It is unclear whether DIFF_TERM will work correctly.
 All non-clock pairs may be pin-swapped in pairs within the bank.
 Clock indicated nets are routed to clock input where possible.
 Clock indicated nets are routed to clock input where possible.

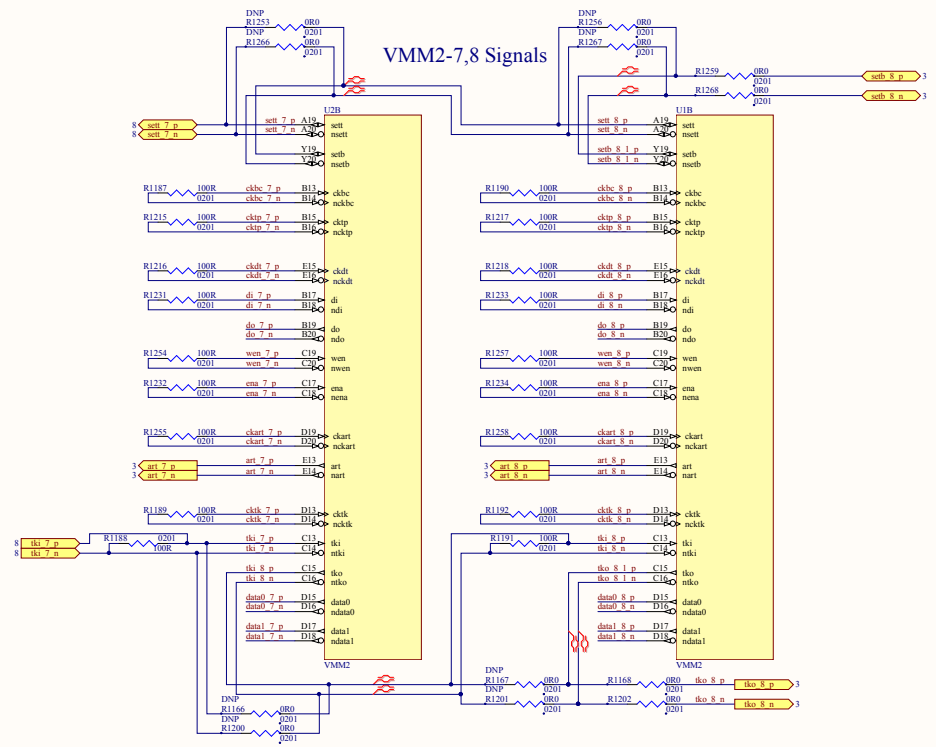


HP 1.2V Bank



- sett: ch0 neighbor trigger
- ckbc: BC clock (timestamp Gray-code counter advance)
- cktp: test pulse clock
- di: configuration data input
- do: configuration data output
- tki: token input (in analog mode)
- tko: token output (in analog mode)
- ena: acquisition start/stop
 ena high, wen low: acquisition is enabled internally enabled after 40ns from ena high in two-phase (analog) mode is acquisition in continuous (digital) mode is acquisition and readout in two-phase mode is readout
 ena low, wen low: acquisition is enabled
 ena pulse, wen high: global reset (acquisition and registers)
- wen: configuration enable
 wen high: configuration mode
 wen pulse: acquisition reset (also resets BC counter)
- ckk: token clock
- data0: flag and first data line (flag and address in analog mode)
- data1: second data line
- ckart: ART clock
- art: ART output
- ckdt: configuration (data input), data output and 6-bit ADC clock
- setb: ch63 neighbor trigger

Board to Board neighbor connector is not needed

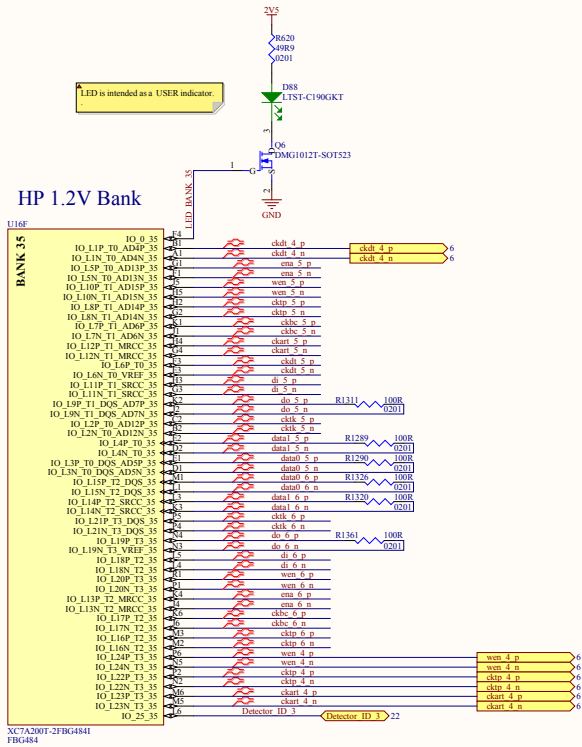


HP Bank 34
 Sufficient 1.2V Differential IO for 2 VMMS.
 All paired routing is 100 Ohm Differential and length matched TBD
 All un-paired routing is 50 Ohm single-ended.
 Bank Voltage is at 1.2V.
 Vref is handled internally by INTERNAL_VREF and pins are available for IO.
 IFC is available on HP bank.
 It is unclear whether DIFF_TERM will work correctly.
 All non-clock pairs may be pin-swapped as pairs within the bank.
 Clock indicated nets are routed to clock input where possible.

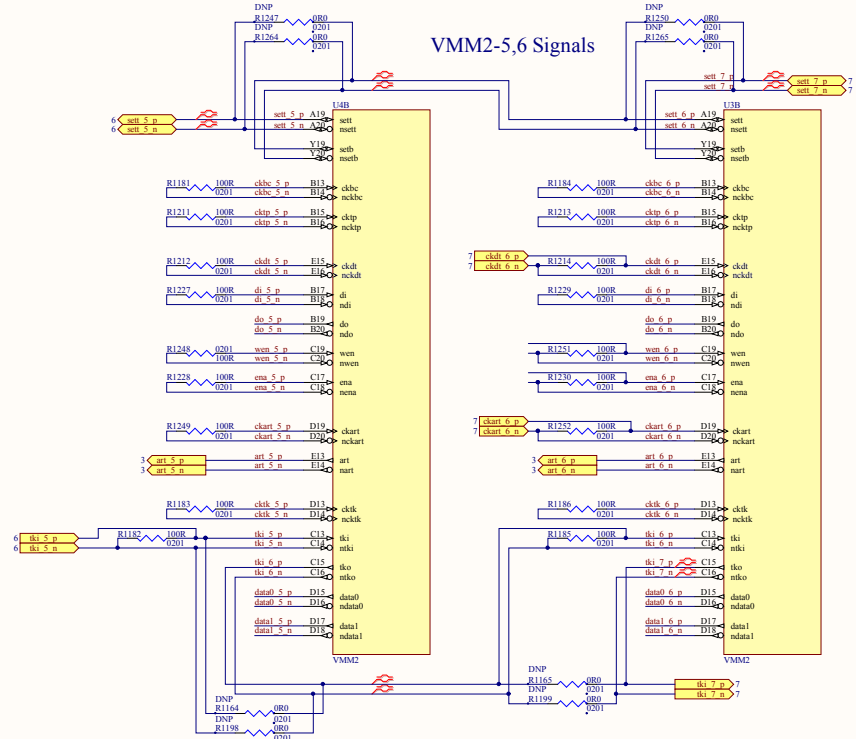
sett: ch0 neighbor trigger
 ckbc: BC clock (timestamp Gray-code counter advance)
 cktp: test pulse clock
 di: configuration data input
 do: configuration data output
 tki: token input (in analog mode)
 tko: token output (in analog mode)
 ena: acquisition start/stop
 ena high, wen low: acquisition is enabled internally enabled after 40ns from ena high in two-phase (analog) mode is acquisition in continuous (digital) mode is acquisition and readout
 ena low, wen low: in two-phase mode is readout
 ena pulse, wen high: global reset (acquisition and registers)
 wen: configuration enable
 wen high: configuration mode
 wen pulse: acquisition reset (also resets BC counter)
 cktk: token clock
 data0: flag and first data line (flag and address in analog mode)
 data1: second data line
 ckart: ART clock
 art: ART output
 ckdat: configuration (data input), data output and 6-bit ADC clock
 setb: ch63 neighbor trigger

LED is intended as a USER indicator

HP 1.2V Bank

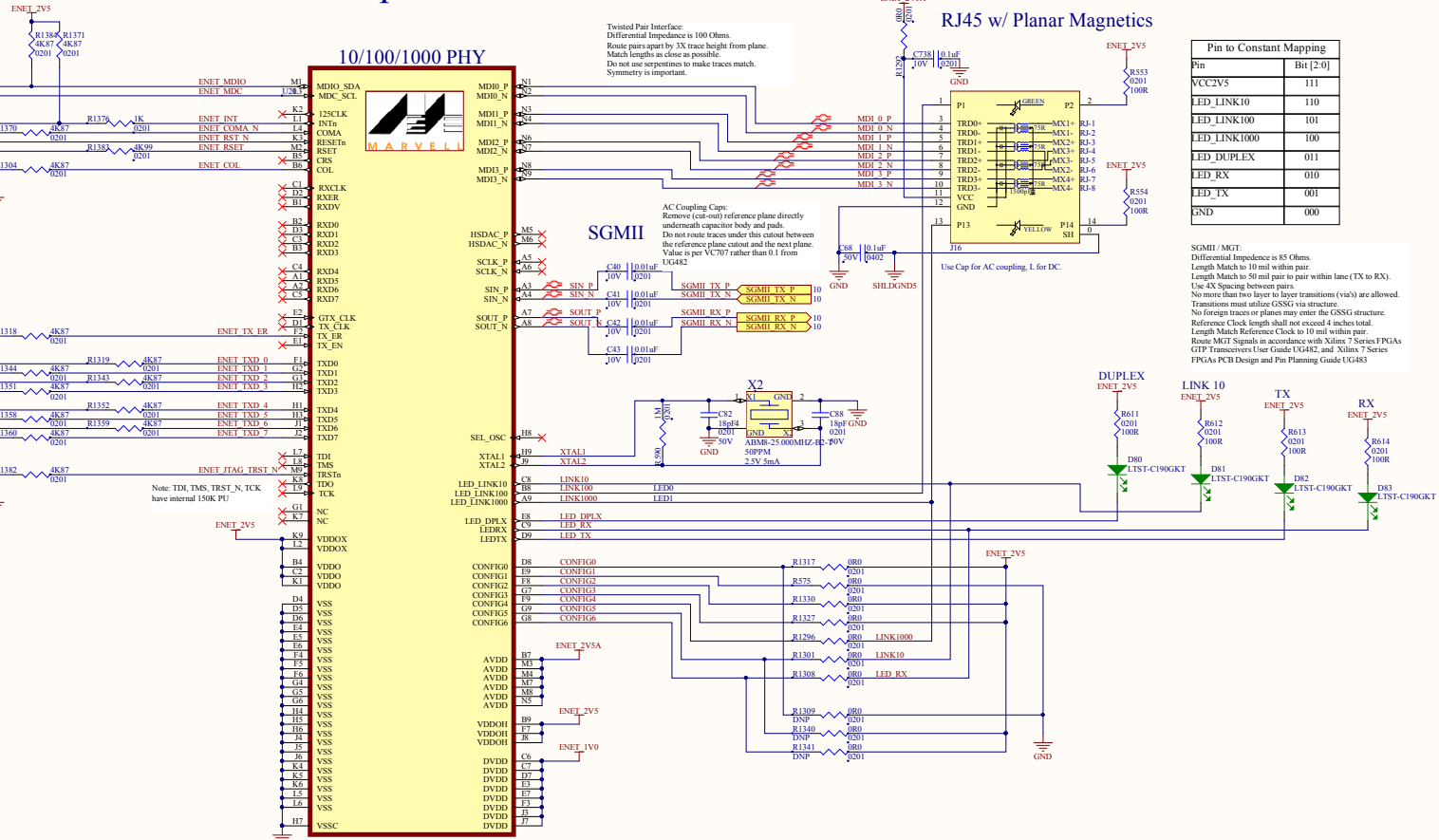


VMM2-5,6 Signals



MD Interface:
Trace Impedance = 40 Ohms
Length match to < 385 mil
Spacing is 10 mil for short runs, 4 mils for parallel runs < 500 mils.
Place series term resistor close to transmitter

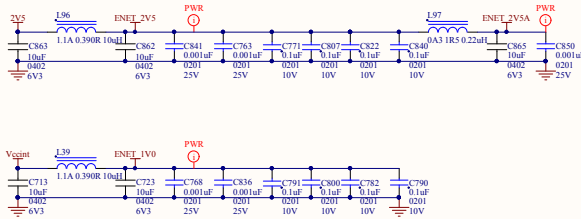
Ethernet Peripheral Interface

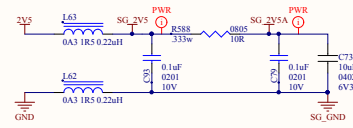
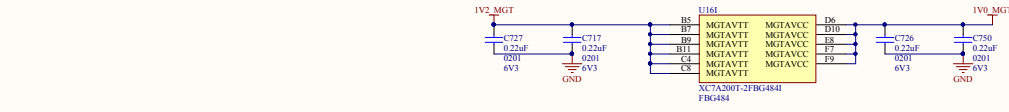


Pin	Bit [2:0]
VCC2V5	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
GND	000

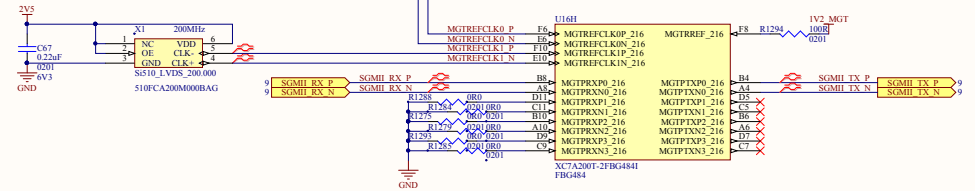
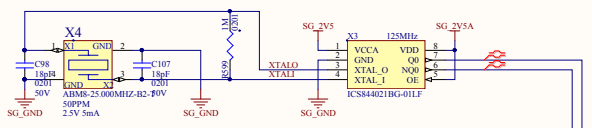
SGMII / MGT:
Differential Impedance is 85 Ohms.
Length Match to 50 mil within pair.
Length Match to 10 mil within pair (TX or RX).
Use 4X Spacing between pairs.
No more than two layer to layer transitions (via's) are allowed.
Transitions must utilize GSSG via structure.
No foreign traces or planes may enter the GSSG structure.
Reference Clock length shall not exceed 4 inches total.
Length Match Reference Clock to 10 mil within pair.
Route MGT Signals in accordance with Xilinx 7 Series FPGAs
GTP Transceivers User Guide UG482, and Xilinx 7 Series
FPGAs PCB Design and Pin Planning Guide UG483

Pin	Bit[2]	Bit[1]	Bit[0]		
CFG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	111	PHYAddr "00111". Don't advertise the PAUSE bit
CFG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	GND
CFG2	ANEG[3]	ANEG[2]	ANEG[1]	111	Auto-Neg on, advertise all caps, prefer slave. Auto crossover enabled. 125 CLK option disabled.
CFG3	ANEG[0]	ENA_XC	DIS_125	111	VCC2V5
CFG4	HWCFG_MD[2]	HWCFG_MD[1]	HWCFG_MD[0]	100	SGMII w/o Clock w/ Auto-Neg to Cu_0100 Fiber copper auto-detect disabled. Sleep mode disabled.
CFG5	DIS_FC	DIS_SLEEP	HWCFG_MD[3]	110	VCC2V5
CFG6	0 = MDC/MDIO 1 = TWSI	0 = INT Active HIGH 1 = INT Active LOW	0 = 50 OHM SGMII 1 = 75 OHM SGMII	010	MDC/MDIO selected. Active LOW interrupt 500nm SGMII / Fiber option.

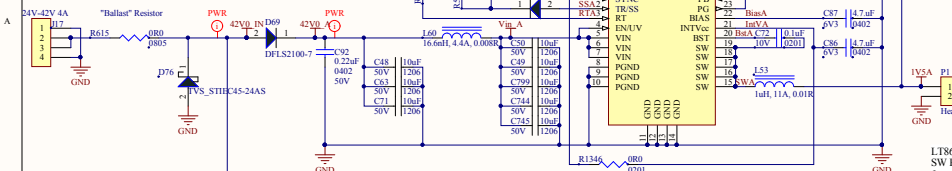




MGT:
 Differential Impedance is 85 Ohms.
 Length Match to 10 mil within pair.
 Length Match to 50 mil pair to pair within lane (TX to RX).
 Use 4X Spacing between pairs.
 No more than two layer to layer transitions (via's) are allowed.
 Transitions must utilize GSSG via structure.
 No foreign traces or planes may enter the GSSG structure.
 Reference Clock length shall not exceed 4 inches total.
 Length Match Reference Clock to 10 mil within pair.
 Route MGT Signals in accordance with Xilinx 7 Series FPGAs
 GTP Transceivers User Guide UG482, and Xilinx 7 Series
 FPGAs PCB Design and Pin Planning Guide UG483



VMM Analog Power - 1.5V to VMM 1.2V LDO's

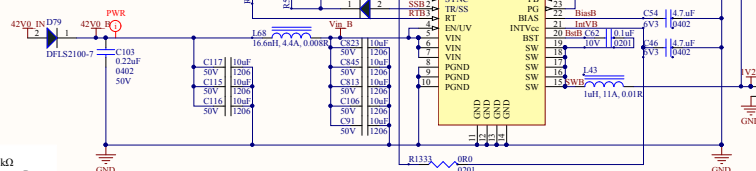


LT8612: $R1(vout)=R2(gnd) \times (Vout / 0.970V - 1)$
 1.0V ⇒ $K=0.0309, R2=100K, R1=3K09$
 1.2V ⇒ $K=0.2371, R2=100K, R1=23K7$
 1.5V ⇒ $K=0.5464, R2=100K, R1=54K6$
 1.8V ⇒ $K=0.8557, R2=100K, R1=85K6$
 2.5V ⇒ $K=1.5773, R2=100K, R1=157K8$

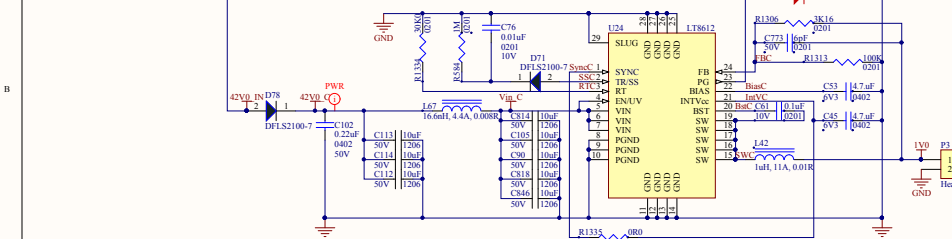
LT8612 Table 1.
SW Freq MHz vs RT Value kΩ

SW Freq MHz	RT Value kΩ	Rrt
0.2	232	1.0
0.3	150	1.2
0.4	110	1.4
0.5	88.7	1.6
0.6	71.5	1.8
0.7	60.4	2.0
0.8	52.3	2.2
		15.8

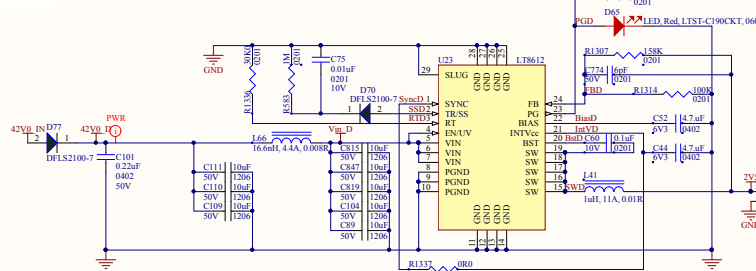
VMM/FPGA 1.2V Digital IO Power



FPGA 1.0V Internal Power



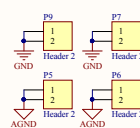
FPGA 2.5V Power - Supply to MGT 1.2V, MGT 1.0V LDO's and to FPGA 1.8V Analog, Vccaux LDO's



Power Estimates:
 LT8612 #1 1.5V Analog
 Iavg18 = 8*0.427A = 3.42A + losses
 LT8612 #2 1.2V Digital
 Iavg112 = 8*1.150A = 9.2A + losses
 LT8612 #3 1.0V FPGA
 Iavg10 = 3.15A + losses
 LT8612 #4 2.5V FPGA
 Iavg25 = 0.621A + losses
 + 0.511A Mgt12V
 + 36A Iavg18
 + 0.32A Vccaux
 = 1.8A + losses

Note:
 Iccauxq (Vaux Quiescent) = 7mA
 1.8V LVCMOS25 or 33 = 2-24mA per pin
 1.2V SSTL / HSTL 8mA per pin max

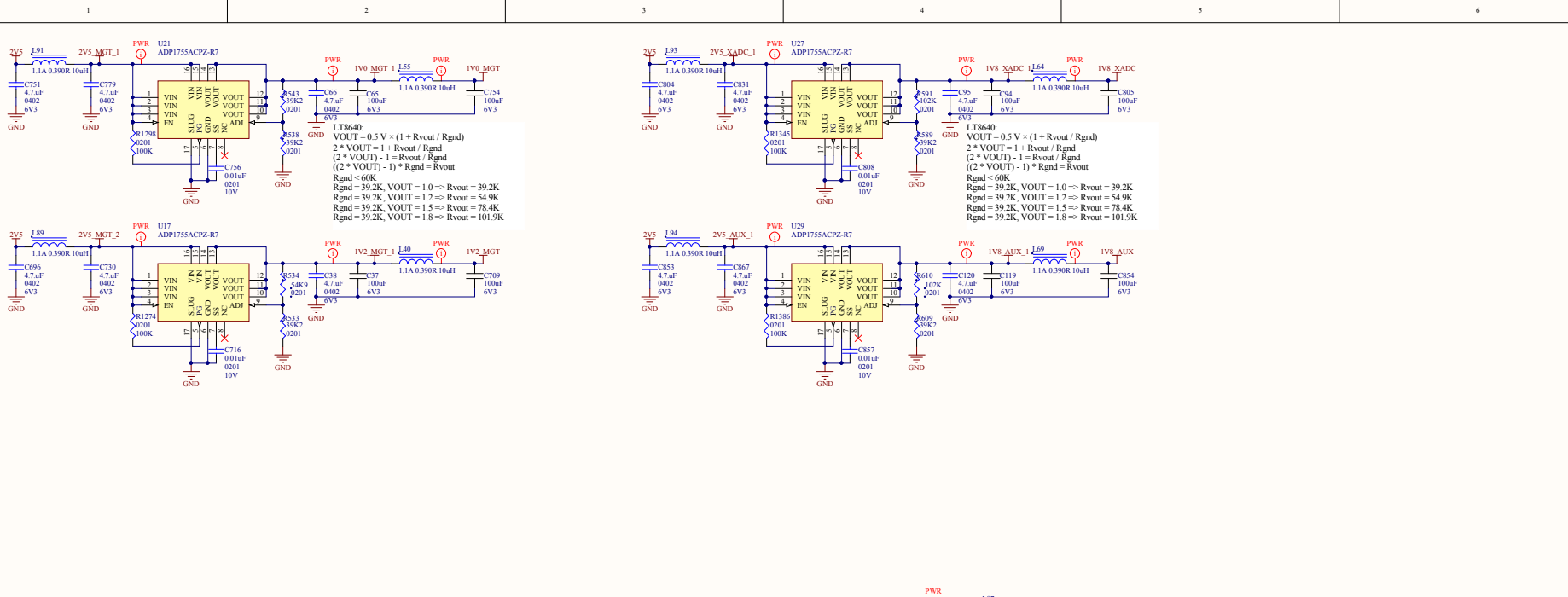
Ground Reference for Probes



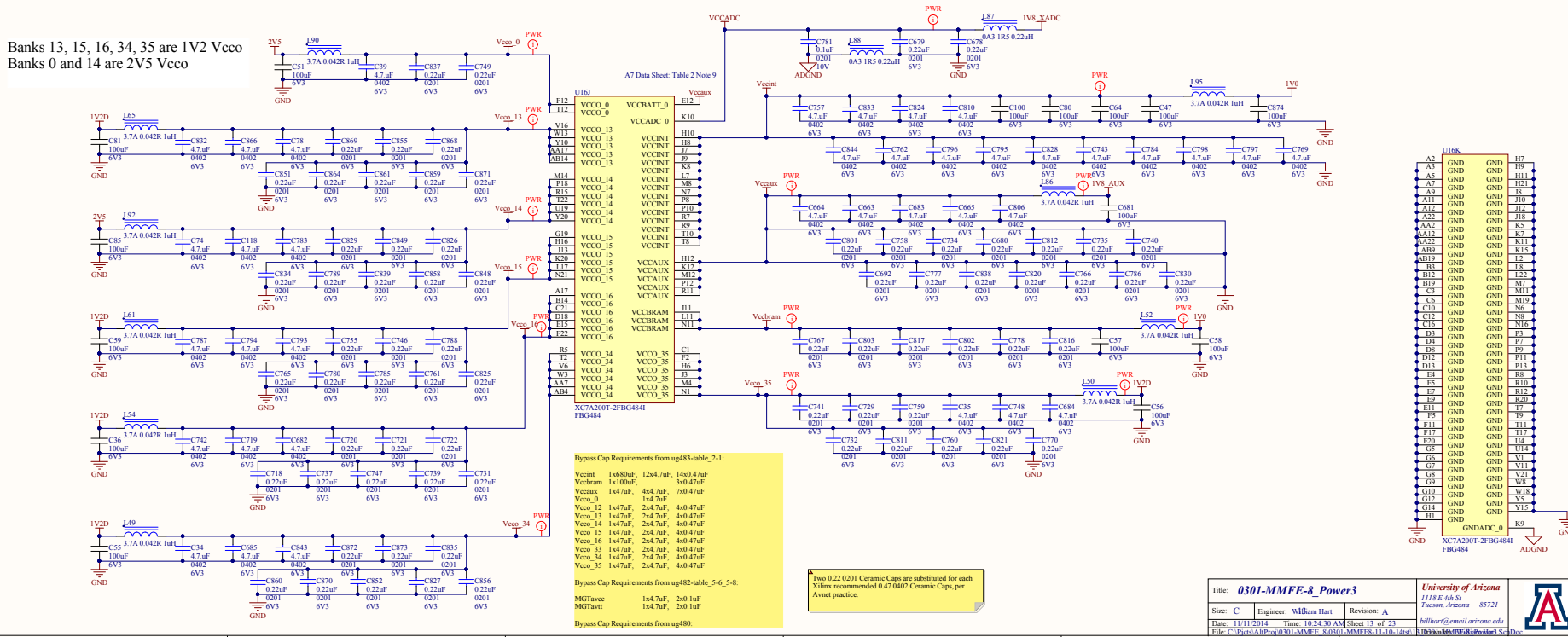
ISR:
 $DF = \tan(\phi) = ESR / Xc = 0.1$ for CC
 $ISR = DF * Xc = DF / (2 \pi f * C) = Xc / Q = \tan(\phi) * Xc$
 $Z = (ESR^2 + (Xc * Xc) / 2)^{0.5}$
 $f = 1 / (2 \pi * L * C)^{0.5}$
 Spec for Al and Film caps @ 100KHz
 Spec for Al and Tan @ 20Hz
 ISR = Radiq(0.3MHz) + Resmet(30-300MHz)
 ISR2 = ISR1 * (f2/f1)^0.5
 ISR calculations for ceramic caps use DF of 10%, max @ 120Hz, used @ 1MHz = 0.005Ohms worst case.

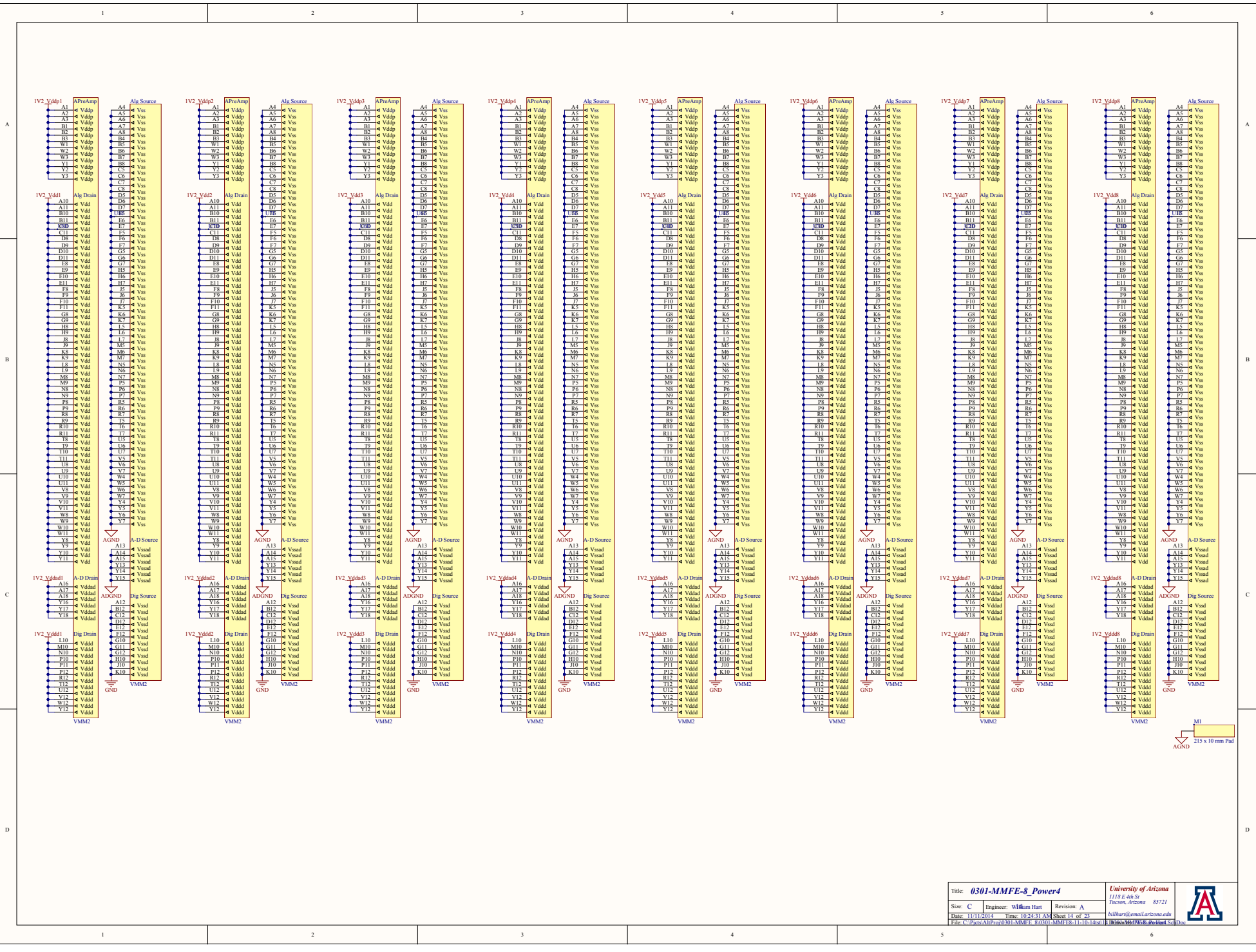
When laying out power, please route point to point first, with trace width sufficient to carry the required current.
 Pours or splits can then be instantiated afterwards, without fear of islands or choke points.
 This is especially critical for FPGA power distribution, and makes verification easier.





Banks 13, 15, 16, 34, 35 are 1V2 Vcco
 Banks 0 and 14 are 2V5 Vcco





Analog Input Routing:

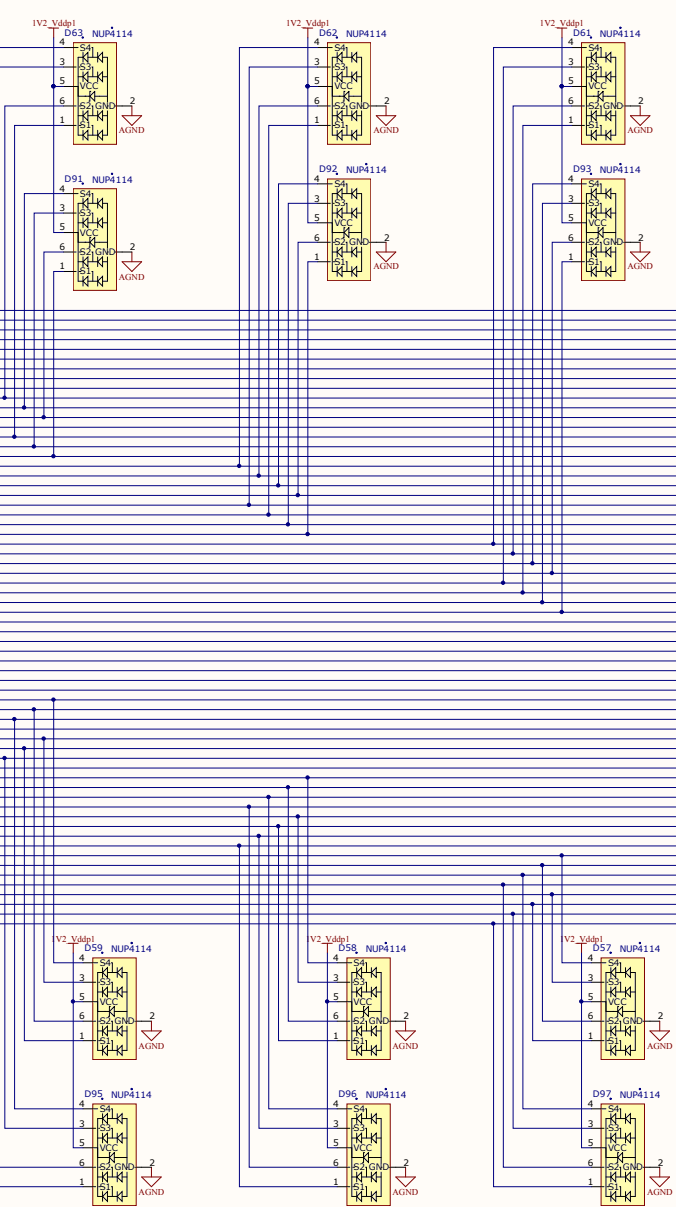
Traces from input connectors (Zaxis, Zebra, etc) are routed alternately to top and bottom layers.

Currently using max width of .152mm (6 mil) for min L.

Layer stack for this area is 14 layers with all groundplanes removed except for inner 4 layers which are Vddp - AGND - AGND - Vddp, to reduce capacitance.

Length matching is not required. Utilize latest optimized structures.

USA VMM2	Pin	Resistor	Value	Pin	Value	Pin	Value	Pin	Value
	WPC2	R512	10R						
	WPC3	R886	10R		R511	10R			
	WPC4	R201	10R		R887	10R			
	WPD1	R510	10R		R201	10R			
	WPD2	R888	10R		R509	10R			
	WPD3	R888	10R		R201	10R			
	WPD4	R508	10R		R889	10R			
	WPE2	R507	10R						
	WPE3	R890	10R		R505	10R			
	WPE4	R891	10R		R891	10R			
	WPF1	R506	10R		R201	10R			
	WPF2	R892	10R		R505	10R			
	WPF3	R891	10R						
	WPF4	R504	10R		R891	10R			
	WPG1	R503	10R		R503	10R			
	WPG2	R894	10R						
	WPG3	R894	10R		R893	10R			
	WPG4	R502	10R						
	WPH1	R502	10R		R201	10R			
	WPH2	R501	10R						
	WPH3	R896	10R		R201	10R			
	WPH4	R501	10R		R897	10R			
	WPI1	R500	10R						
	WPI2	R499	10R						
	WPI3	R898	10R		R899	10R			
	WPI4	R898	10R		R899	10R			
	WPK1	R498	10R						
	WPK2	R497	10R		R497	10R			
	WPK3	R500	10R		R201	10R			
	WPK4	R496	10R		R901	10R			
	WPL1	R496	10R						
	WPL2	R502	10R		R495	10R			
	WPL3	R502	10R						
	WPL4	R503	10R		R903	10R			
	WPM1	R494	10R						
	WPM2	R493	10R		R493	10R			
	WPM3	R904	10R						
	WPM4	R201	10R		R905	10R			
	WPN1	R492	10R						
	WPN2	R491	10R						
	WPN3	R906	10R						
	WPN4	R490	10R		R907	10R			
	WPP1	R489	10R						
	WPP2	R489	10R		R489	10R			
	WPP3	R908	10R						
	WPP4	R909	10R						
	WPR1	R488	10R		R487	10R			
	WPR2	R510	10R						
	WPR3	R510	10R		R911	10R			
	WPR4	R486	10R						
	WPR5	R486	10R						
	WPT1	R512	10R		R485	10R			
	WPT2	R512	10R						
	WPT3	R912	10R						
	WPT4	R913	10R		R911	10R			
	WPT5	R484	10R						
	WPT6	R483	10R						
	WPT7	R914	10R						
	WPT8	R914	10R		R915	10R			
	WPT9	R482	10R						
	WPT10	R481	10R						
	WPT11	R916	10R						
	WPT12	R917	10R						



Detector ID	Detector ID	Detector ID	Detector ID	Detector ID	Detector ID
D64	D63	D62	D61	D90	D91
D90	D91	D92	D91	D90	D97
D97	D96	D95	D97	D96	D95

Detector ID	Detector ID	Detector ID	Detector ID	Detector ID	Detector ID
D64	D63	D62	D61	D90	D91
D90	D91	D92	D91	D90	D97
D97	D96	D95	D97	D96	D95



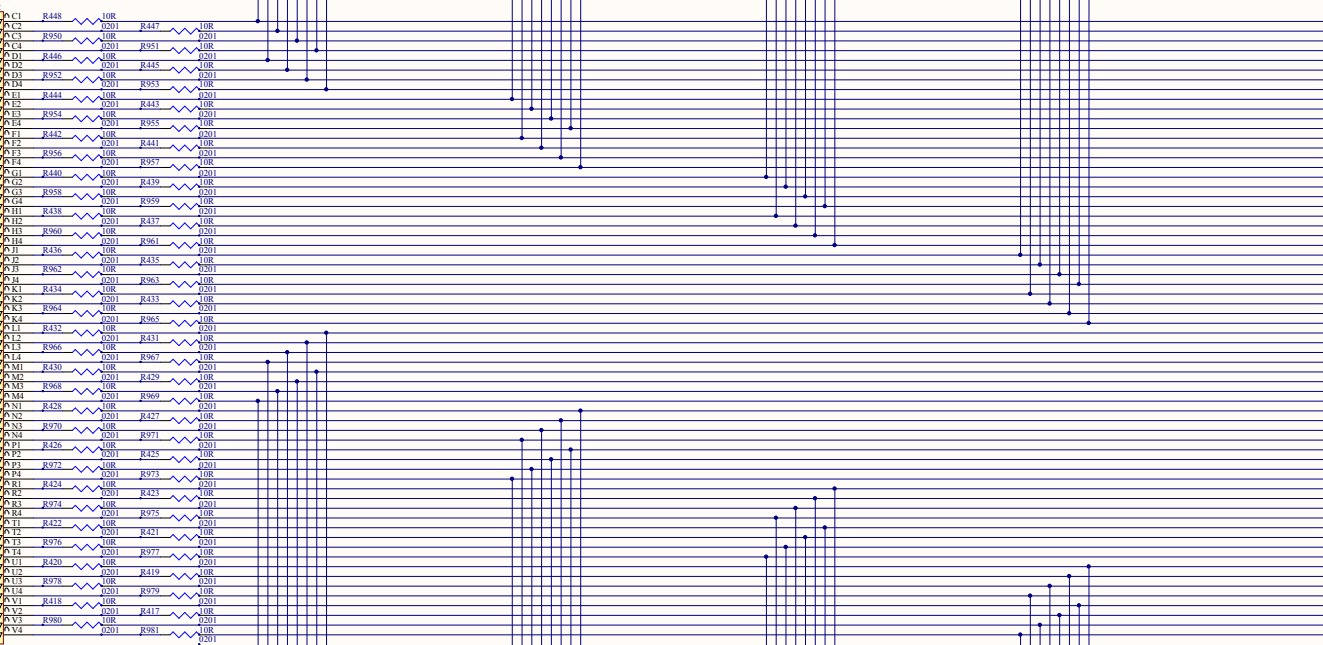
40	U1C1	R480	10R
41	U1C2	0201 R479	10R
42	U1C3	R918	10R
43	U1C4	0201 R919	0201
44	U1D1	R475	10R
45	U1D2	0201 R477	10R
46	U1D3	R920	10R
47	U1D4	0201 R921	10R
48	U1E1	R476	10R
49	U1E2	0201 R475	10R
50	U1E3	R922	10R
51	U1E4	0201 R923	10R
52	U1F1	R474	10R
53	U1F2	0201 R473	10R
54	U1F3	R924	10R
55	U1F4	0201 R925	10R
56	U1G1	R472	10R
57	U1G2	0201 R471	10R
58	U1G3	R926	10R
59	U1G4	0201 R927	10R
60	U1H1	R470	10R
61	U1H2	0201 R469	10R
62	U1H3	R928	10R
63	U1H4	0201 R929	10R
64	U1J1	R468	10R
65	U1J2	0201 R467	10R
66	U1J3	R930	10R
67	U1J4	0201 R931	10R
68	U1K1	R466	10R
69	U1K2	0201 R465	10R
70	U1K3	R932	10R
71	U1K4	0201 R933	10R
72	U1L1	R464	10R
73	U1L2	0201 R463	10R
74	U1L3	R934	10R
75	U1L4	0201 R935	10R
76	U1M1	R462	10R
77	U1M2	0201 R461	10R
78	U1M3	R936	10R
79	U1M4	0201 R937	10R
80	U1N1	R460	10R
81	U1N2	0201 R459	10R
82	U1N3	R938	10R
83	U1N4	0201 R939	10R
84	U1P1	R458	10R
85	U1P2	0201 R457	10R
86	U1P3	R940	10R
87	U1P4	0201 R941	10R
88	U1R1	R456	10R
89	U1R2	0201 R455	10R
90	U1R3	R942	10R
91	U1R4	0201 R943	10R
92	U1T1	R454	10R
93	U1T2	0201 R453	10R
94	U1T3	R944	10R
95	U1T4	0201 R945	10R
96	U1U1	R452	10R
97	U1U2	0201 R451	10R
98	U1U3	R946	10R
99	U1U4	0201 R947	10R
100	U1V1	R450	10R
101	U1V2	0201 R449	10R
102	U1V3	R948	10R
103	U1V4	0201 R949	10R
104	U1W4	0201	0201

60	R224	10R
61	0201 R223	10R
62	R654	10R
63	0201 R655	10R
64	R232	10R
65	0201 R231	10R
66	R656	10R
67	0201 R657	10R
68	R220	10R
69	0201 R219	10R
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72	R218	10R
73	0201 R217	10R
74	R660	10R
75	0201 R661	10R
76	R216	10R
77	0201 R215	10R
78	R662	10R
79	0201 R663	10R
80	R214	10R
81	0201 R213	10R
82	R664	10R
83	0201 R665	10R
84	R212	10R
85	0201 R211	10R
86	R666	10R
87	0201 R667	10R
88	R210	10R
89	0201 R209	10R
90	R668	10R
91	0201 R669	10R
92	R208	10R
93	0201 R207	10R
94	R670	10R
95	0201 R671	10R
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99	0201 R673	10R
100	R204	10R
101	0201 R203	10R
102	R674	10R
103	0201 R675	10R
104	R202	10R
105	0201 R201	10R
106	R676	10R
107	0201 R677	10R
108	R200	10R
109	0201 R199	10R
110	R678	10R
111	0201 R679	10R
112	R198	10R
113	0201 R197	10R
114	R680	10R
115	0201 R681	10R
116	R196	10R
117	0201 R195	10R
118	R682	10R
119	0201 R683	10R
120	R194	10R
121	0201 R193	10R
122	R684	10R
123	0201 R685	10R

Zachs_200_E_end



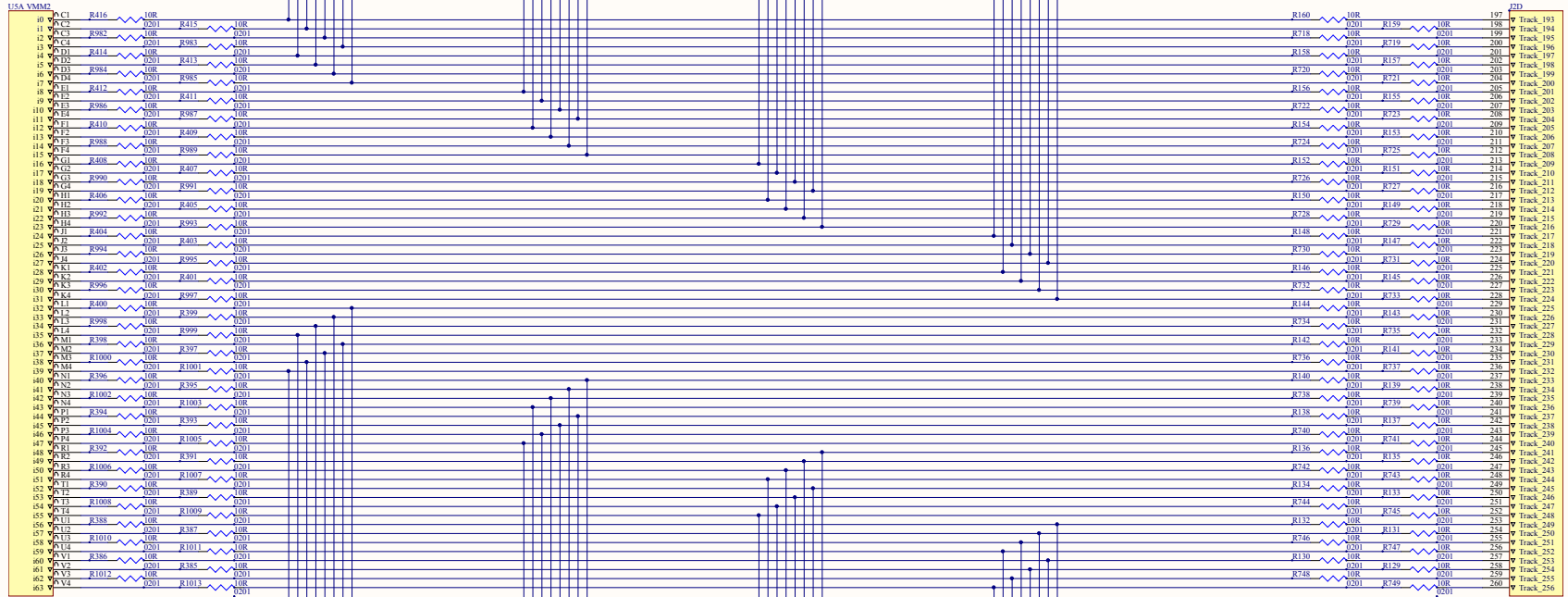
U6A VMM2

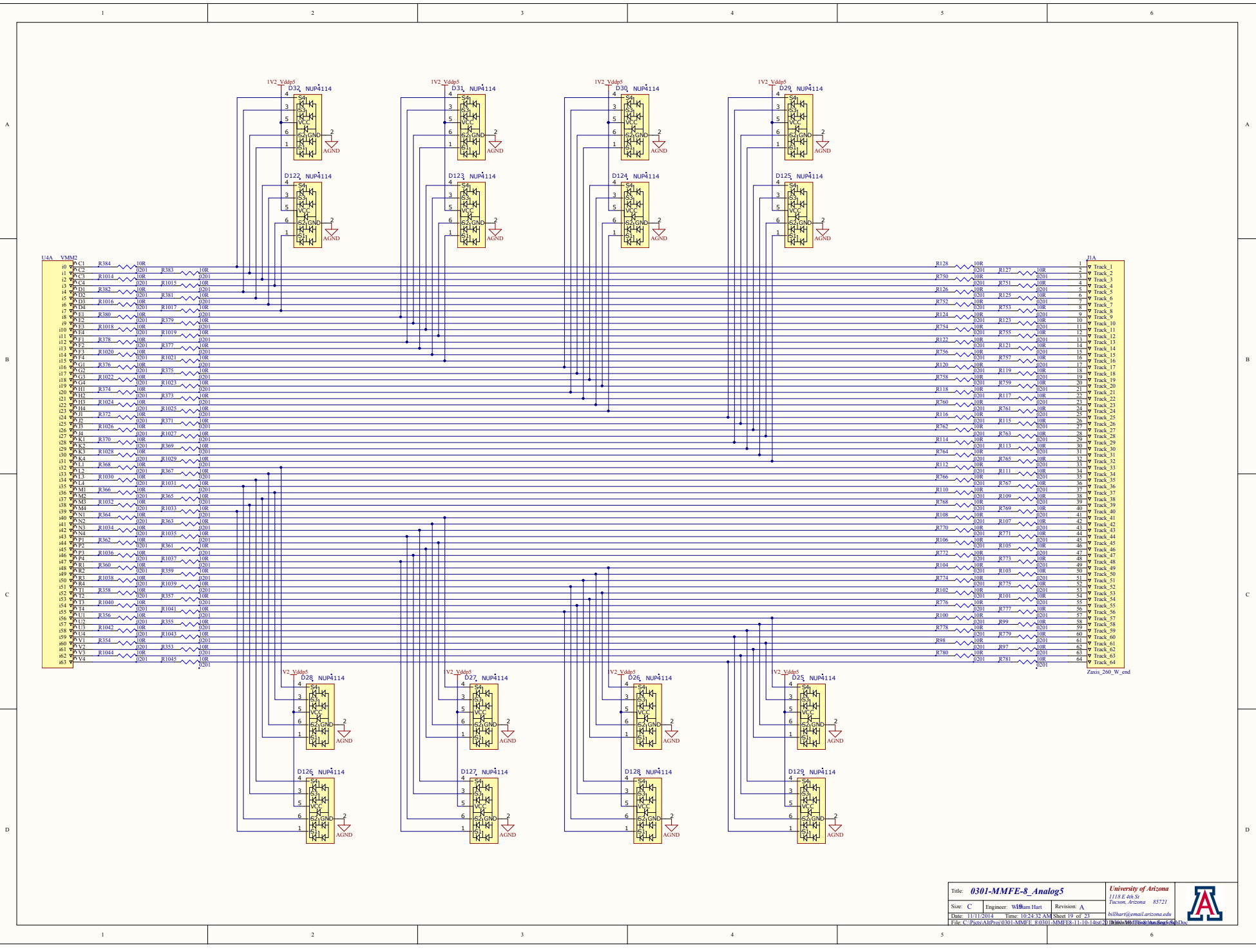


R192	10R		133	D2C
D201	R191	10R	134	Track 129
10R		D201	135	Track 130
R686	10R	D201	136	Track 131
D201	R687	10R	137	Track 132
R190	10R	D201	138	Track 133
D201	R189	10R	139	Track 134
R688	10R	D201	140	Track 135
D201	R689	10R	141	Track 136
R188	10R	D201	142	Track 137
D201	R187	10R	143	Track 138
R690	10R	D201	144	Track 139
D201	R691	10R	145	Track 140
R186	10R	D201	146	Track 141
D201	R185	10R	147	Track 142
R692	10R	D201	148	Track 143
D201	R693	10R	149	Track 144
R184	10R	D201	150	Track 145
D201	R183	10R	151	Track 146
R694	10R	D201	152	Track 147
D201	R695	10R	153	Track 148
R182	10R	D201	154	Track 149
D201	R181	10R	155	Track 150
R696	10R	D201	156	Track 151
D201	R697	10R	157	Track 152
R180	10R	D201	158	Track 153
D201	R179	10R	159	Track 154
R698	10R	D201	160	Track 155
D201	R699	10R	161	Track 156
R178	10R	D201	162	Track 157
D201	R177	10R	163	Track 158
R700	10R	D201	164	Track 159
D201	R701	10R	165	Track 160
R176	10R	D201	166	Track 161
D201	R175	10R	167	Track 162
R702	10R	D201	168	Track 163
D201	R703	10R	169	Track 164
R174	10R	D201	170	Track 165
D201	R173	10R	171	Track 166
R704	10R	D201	172	Track 167
D201	R705	10R	173	Track 168
R172	10R	D201	174	Track 169
D201	R171	10R	175	Track 170
R706	10R	D201	176	Track 171
D201	R707	10R	177	Track 172
R170	10R	D201	178	Track 173
D201	R169	10R	179	Track 174
R708	10R	D201	180	Track 175
D201	R709	10R	181	Track 176
R168	10R	D201	182	Track 177
D201	R167	10R	183	Track 178
R710	10R	D201	184	Track 179
D201	R711	10R	185	Track 180
R166	10R	D201	186	Track 181
D201	R165	10R	187	Track 182
R712	10R	D201	188	Track 183
D201	R713	10R	189	Track 184
R164	10R	D201	190	Track 185
D201	R163	10R	191	Track 186
R714	10R	D201	192	Track 187
D201	R715	10R	193	Track 188
R162	10R	D201	194	Track 189
D201	R161	10R	195	Track 190
R716	10R	D201	196	Track 191
D201	R717	10R	197	Track 192

Zaxis_260_E_end

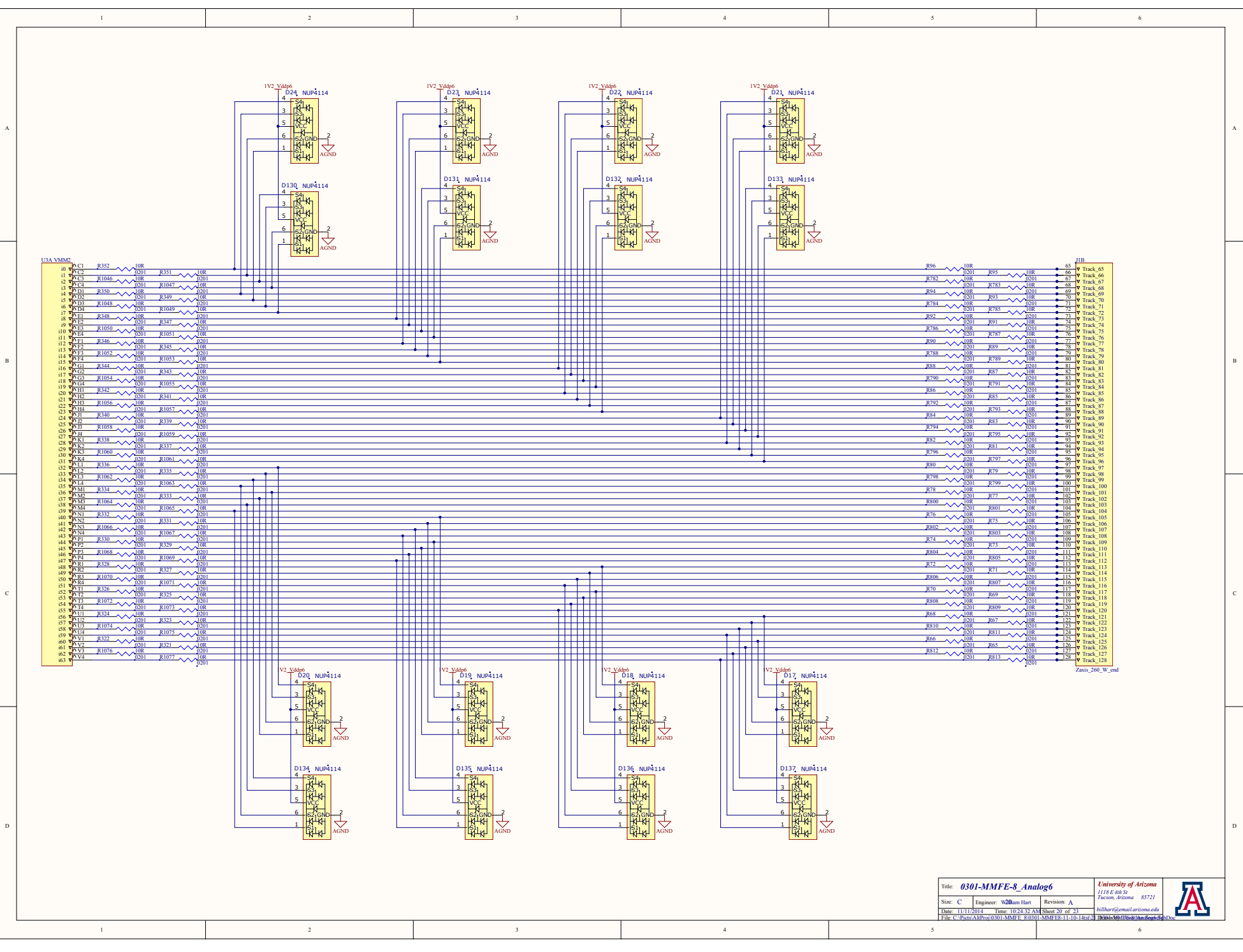






U1A VMM2						J1A	
P1	R384	10R				R128	10R
P2	D201	R383	10R			D201	R127
P3	R1014	10R				R750	10R
P4	D201	R1015	10R			D201	R751
P5	R382	10R				R126	10R
P6	D201	R381	10R			D201	R125
P7	R1016	10R				R752	10R
P8	D201	R1017	10R			D201	R753
P9	R380	10R				R124	10R
P10	D201	R379	10R			D201	R123
P11	R1018	10R				R754	10R
P12	D201	R1019	10R			D201	R755
P13	R378	10R				R122	10R
P14	D201	R377	10R			D201	R121
P15	R1020	10R				R756	10R
P16	D201	R1021	10R			D201	R757
P17	R376	10R				R120	10R
P18	D201	R375	10R			D201	R119
P19	R1022	10R				R758	10R
P20	D201	R1023	10R			D201	R759
P21	R374	10R				R118	10R
P22	D201	R373	10R			D201	R117
P23	R1024	10R				R760	10R
P24	D201	R1025	10R			D201	R761
P25	R372	10R				R116	10R
P26	D201	R371	10R			D201	R115
P27	R1026	10R				R762	10R
P28	D201	R1027	10R			D201	R763
P29	R370	10R				R114	10R
P30	D201	R369	10R			D201	R113
P31	R1028	10R				R764	10R
P32	D201	R1029	10R			D201	R765
P33	R368	10R				R112	10R
P34	D201	R367	10R			D201	R111
P35	R1030	10R				R766	10R
P36	D201	R1031	10R			D201	R767
P37	R366	10R				R110	10R
P38	D201	R365	10R			D201	R109
P39	R1032	10R				R768	10R
P40	D201	R1033	10R			D201	R769
P41	R364	10R				R108	10R
P42	D201	R363	10R			D201	R107
P43	R1034	10R				R770	10R
P44	D201	R1035	10R			D201	R771
P45	R362	10R				R106	10R
P46	D201	R361	10R			D201	R105
P47	R1036	10R				R772	10R
P48	D201	R1037	10R			D201	R773
P49	R360	10R				R104	10R
P50	D201	R359	10R			D201	R103
P51	R1038	10R				R774	10R
P52	D201	R1039	10R			D201	R775
P53	R358	10R				R102	10R
P54	D201	R357	10R			D201	R101
P55	R1040	10R				R776	10R
P56	D201	R1041	10R			D201	R777
P57	R356	10R				R100	10R
P58	D201	R355	10R			D201	R99
P59	R1042	10R				R778	10R
P60	D201	R1043	10R			D201	R779
P61	R354	10R				R98	10R
P62	D201	R353	10R			D201	R97
P63	R1044	10R				R780	10R
P64	D201	R1045	10R			D201	R781

Zaxis_200_W_end

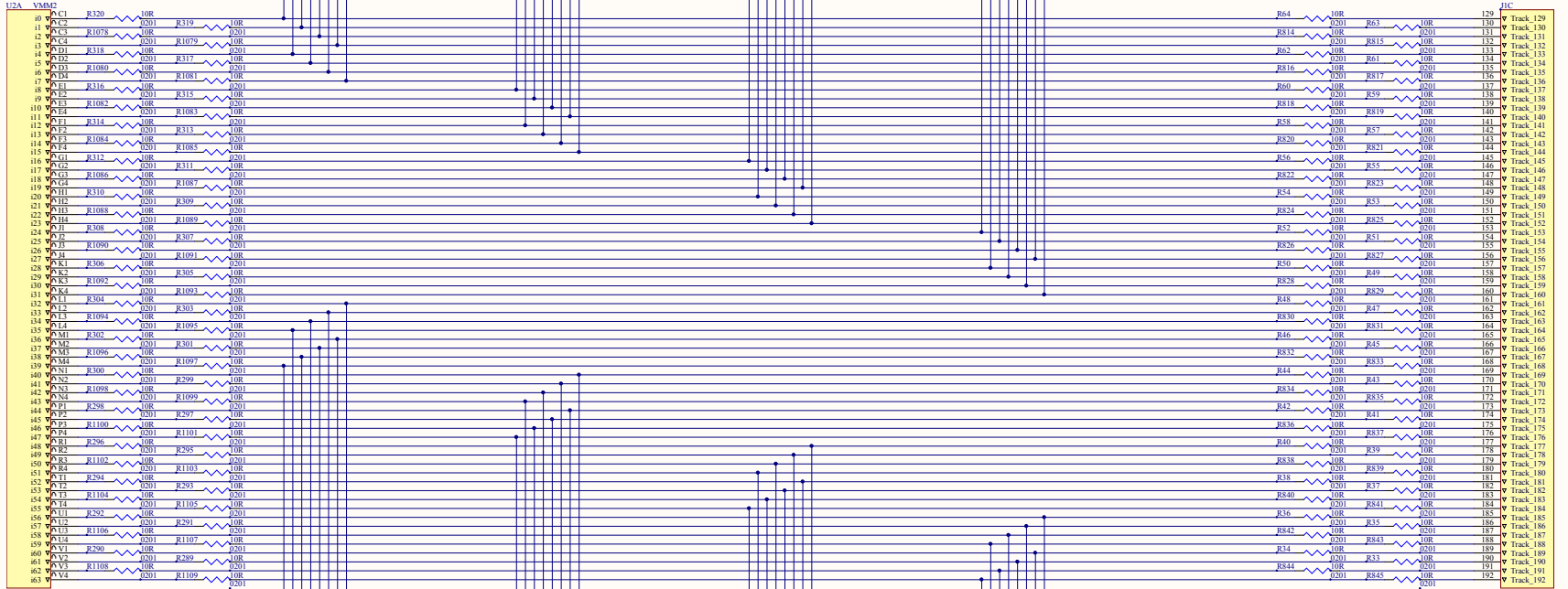


U3A VMME

J1B

U1	R352	10R								R96	10R		65	Track_65
U2	D201	R351	10R							R97	10R	D201	66	Track_66
U3	R1046	10R								R98	10R	D201	67	Track_67
U4	D201	R1047	10R							R99	10R	R783	68	Track_68
U5	R350	10R								R100	10R	D201	69	Track_69
U6	D201	R349	10R							R101	10R	D201	70	Track_70
U7	R1048	10R								R102	10R	R784	71	Track_71
U8	D201	R1049	10R							R103	10R	D201	72	Track_72
U9	R348	10R								R104	10R	D201	73	Track_73
U10	D201	R347	10R							R105	10R	D201	74	Track_74
U11	R1050	10R								R106	10R	R786	75	Track_75
U12	D201	R1051	10R							R107	10R	D201	76	Track_76
U13	R346	10R								R108	10R	D201	77	Track_77
U14	D201	R345	10R							R109	10R	D201	78	Track_78
U15	R1052	10R								R110	10R	R788	79	Track_79
U16	D201	R1053	10R							R111	10R	D201	80	Track_80
U17	R344	10R								R112	10R	D201	81	Track_81
U18	D201	R343	10R							R113	10R	R787	82	Track_82
U19	R1054	10R								R114	10R	D201	83	Track_83
U20	D201	R1055	10R							R115	10R	D201	84	Track_84
U21	R342	10R								R116	10R	D201	85	Track_85
U22	D201	R341	10R							R117	10R	R790	86	Track_86
U23	R1056	10R								R118	10R	D201	87	Track_87
U24	D201	R1057	10R							R119	10R	R791	88	Track_88
U25	R340	10R								R120	10R	D201	89	Track_89
U26	D201	R339	10R							R121	10R	D201	90	Track_90
U27	R1058	10R								R122	10R	R794	91	Track_91
U28	D201	R1059	10R							R123	10R	D201	92	Track_92
U29	R338	10R								R124	10R	D201	93	Track_93
U30	D201	R337	10R							R125	10R	R796	94	Track_94
U31	R1060	10R								R126	10R	D201	95	Track_95
U32	D201	R1061	10R							R127	10R	D201	96	Track_96
U33	R336	10R								R128	10R	D201	97	Track_97
U34	D201	R335	10R							R129	10R	R798	98	Track_98
U35	R1062	10R								R130	10R	D201	99	Track_99
U36	D201	R1063	10R							R131	10R	D201	100	Track_100
U37	R334	10R								R132	10R	R78	101	Track_101
U38	D201	R333	10R							R133	10R	D201	102	Track_102
U39	R1064	10R								R134	10R	D201	103	Track_103
U40	D201	R1065	10R							R135	10R	R800	104	Track_104
U41	R332	10R								R136	10R	D201	105	Track_105
U42	D201	R331	10R							R137	10R	D201	106	Track_106
U43	R1066	10R								R138	10R	D201	107	Track_107
U44	D201	R1067	10R							R139	10R	R802	108	Track_108
U45	R330	10R								R140	10R	D201	109	Track_109
U46	D201	R329	10R							R141	10R	D201	110	Track_110
U47	R1068	10R								R142	10R	R804	111	Track_111
U48	D201	R1069	10R							R143	10R	D201	112	Track_112
U49	R328	10R								R144	10R	D201	113	Track_113
U50	D201	R327	10R							R145	10R	R772	114	Track_114
U51	R1070	10R								R146	10R	D201	115	Track_115
U52	D201	R1071	10R							R147	10R	R806	116	Track_116
U53	R326	10R								R148	10R	D201	117	Track_117
U54	D201	R325	10R							R149	10R	D201	118	Track_118
U55	R1072	10R								R150	10R	R808	119	Track_119
U56	D201	R1073	10R							R151	10R	D201	120	Track_120
U57	R324	10R								R152	10R	D201	121	Track_121
U58	D201	R323	10R							R153	10R	D201	122	Track_122
U59	R1074	10R								R154	10R	D201	123	Track_123
U60	D201	R1075	10R							R155	10R	R810	124	Track_124
U61	R322	10R								R156	10R	D201	125	Track_125
U62	D201	R321	10R							R157	10R	D201	126	Track_126
U63	R1076	10R								R158	10R	R812	127	Track_127
U64	D201	R1077	10R							R159	10R	D201	128	Track_128

Zaxis_260_W_end



Zachs_260_W_end



U1A VMM2

40 P1 C1 R288 10R

41 P1 C2 0201 R287 10R

42 P1 C3 R1110 10R

43 P1 C4 0201 R1111 10R

44 P1 D1 R286 10R

45 P1 D2 0201 R285 10R

46 P1 D3 R1112 10R

47 P1 D4 0201 R1113 10R

48 P1 E1 R284 10R

49 P1 E2 0201 R283 10R

50 P1 E3 R1114 10R

51 P1 E4 0201 R1115 10R

52 P1 F1 R282 10R

53 P1 F2 0201 R281 10R

54 P1 F3 R1116 10R

55 P1 F4 0201 R1117 10R

56 P1 G1 R280 10R

57 P1 G2 0201 R279 10R

58 P1 G3 R1118 10R

59 P1 G4 0201 R1119 10R

60 P1 H1 R278 10R

61 P1 H2 0201 R277 10R

62 P1 H3 R1120 10R

63 P1 H4 0201 R1121 10R

64 P1 I1 R276 10R

65 P1 I2 0201 R275 10R

66 P1 I3 R1122 10R

67 P1 I4 0201 R1123 10R

68 P1 J1 R274 10R

69 P1 J2 0201 R273 10R

70 P1 J3 R1124 10R

71 P1 J4 0201 R1125 10R

72 P1 K1 R272 10R

73 P1 K2 0201 R271 10R

74 P1 K3 R1126 10R

75 P1 K4 0201 R1127 10R

76 P1 M1 R270 10R

77 P1 M2 0201 R269 10R

78 P1 M3 R1128 10R

79 P1 M4 0201 R1129 10R

80 P1 N1 R268 10R

81 P1 N2 0201 R267 10R

82 P1 N3 R1130 10R

83 P1 N4 0201 R1131 10R

84 P1 P1 R266 10R

85 P1 P2 0201 R265 10R

86 P1 P3 R1132 10R

87 P1 P4 0201 R1133 10R

88 P1 Q1 R264 10R

89 P1 Q2 0201 R263 10R

90 P1 Q3 R1134 10R

91 P1 Q4 0201 R1135 10R

92 P1 R1 R262 10R

93 P1 R2 0201 R261 10R

94 P1 R3 R1136 10R

95 P1 R4 0201 R1137 10R

96 P1 T1 R260 10R

97 P1 T2 0201 R259 10R

98 P1 T3 R1138 10R

99 P1 T4 0201 R1139 10R

100 P1 V1 R258 10R

101 P1 V2 0201 R257 10R

102 P1 V3 R1140 10R

103 P1 V4 0201 R1141 10R

104 P1 V4

R32 10R

R30 10R

R346 10R

R30 10R

R348 10R

R28 10R

R850 10R

R26 10R

R852 10R

R24 10R

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R22 10R

R856 10R

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R868 10R

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R870 10R

R6 10R

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R4 10R

R874 10R

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R876 10R

R31 10R

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253 10R

254 10R

255 10R

256 10R

257 10R

258 10R

259 10R

260 10R

Detector ID 1

Detector ID 2

Detector ID 3

Detector ID 4

Detector ID 5

Detector ID 6

Detector ID 7

Zaxxa_260_W_end

