

ABCD

B

C

Accessories

CBL1
CBL-miniSAS-36
miniSAS 4i 36 ckt

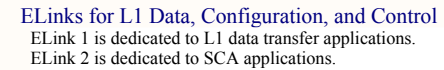
CBL2
CBL-miniSAS-36
miniSAS 4i 36 ckt

D

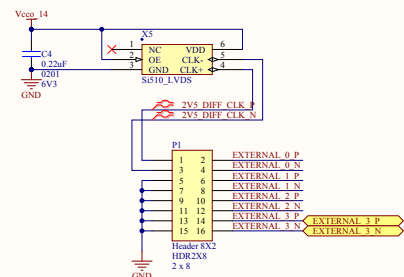
All paired routing is 100 Ohm Differential and length matched TBD
All un-paired routing is 50 Ohm single ended.



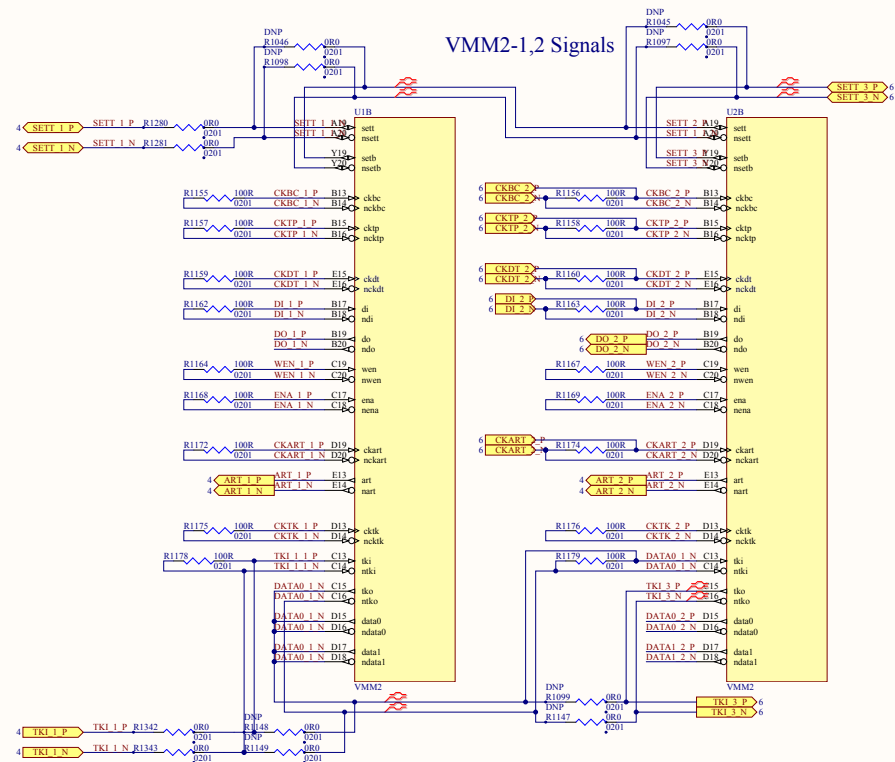
It is unclear whether DIFF_TERM will work correctly.
All non-clock pairs may be pin-swapped as pairs within the bank.
Clock indicated nets are routed to clock input where possible.



Bank Voltage is at 2.5V, not adjustable due to PHY.
Vref is handled internally by INTERNAL_VREF and pins are available for IO.
DCI is not available in HR banks.
It is unclear whether DIFF_TERM will work correctly.
All non-clock pairs may be pin-swapped as pairs within the bank.
Clock indicated nets are routed to clock input where possible.



Sufficient 1.2V Differential IO for part of a VMM, 1 uHDMI, 2 Ext IO pairs.
8 Differential Analog Inputs
All paired routing is 100 Ohm Differential and length matched TBD
All un-paired routing is 50 Ohm single ended.
Bank Voltage is at 1.2V.
Vref is handled internally by INTERNAL_VREF and pins are available for IO
DCI is not available in HR banks.
It is unclear whether DIFF_TERM will work correctly.
All non-clock pairs may be pin-swapped as pairs within the bank.
Clock indicated nets are routed to clock input where possible.



Clock indicated nets are routed to clock input where possible.

clktx:	token clock
data0:	flag and first data line (flag and address in analog mode)
data1:	second data line
ckart:	ART clock
art:	ART output
ckdtx:	configuration (data input), data output and 6-bit ADC clock
setb:	ch63 neighbor trigger

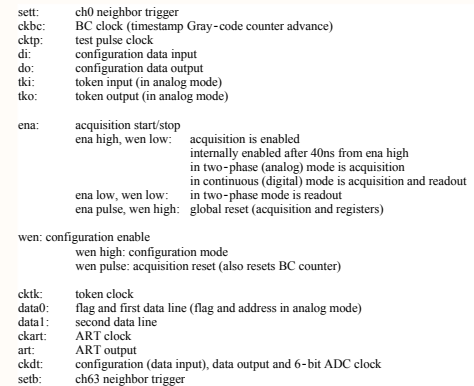


LED is intended as a USER indicator.

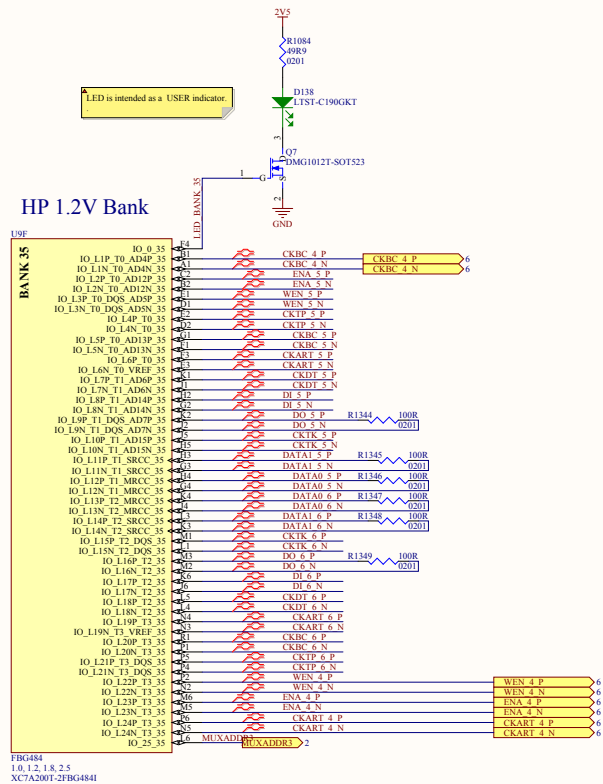
U9E



VMM2-7,8 Signals



HP Bank 34:
Sufficient 1.2V Differential IO for 2 VMMs.
All paired routing is 100 Ohm Differential and length matched THD
All un-paired routing is 50 Ohm single ended.
Bank Voltage is at 1.2V.
Vref is handled internally by INTERNAL_VREF and pins are available for IO.
DCI is available in HP banks.
It is unclear whether DMF_TERM will work correctly.
All non-clock pairs may be pin-swapped as pairs within the bank.
Clock indicated nets are routed to clock input where possible.

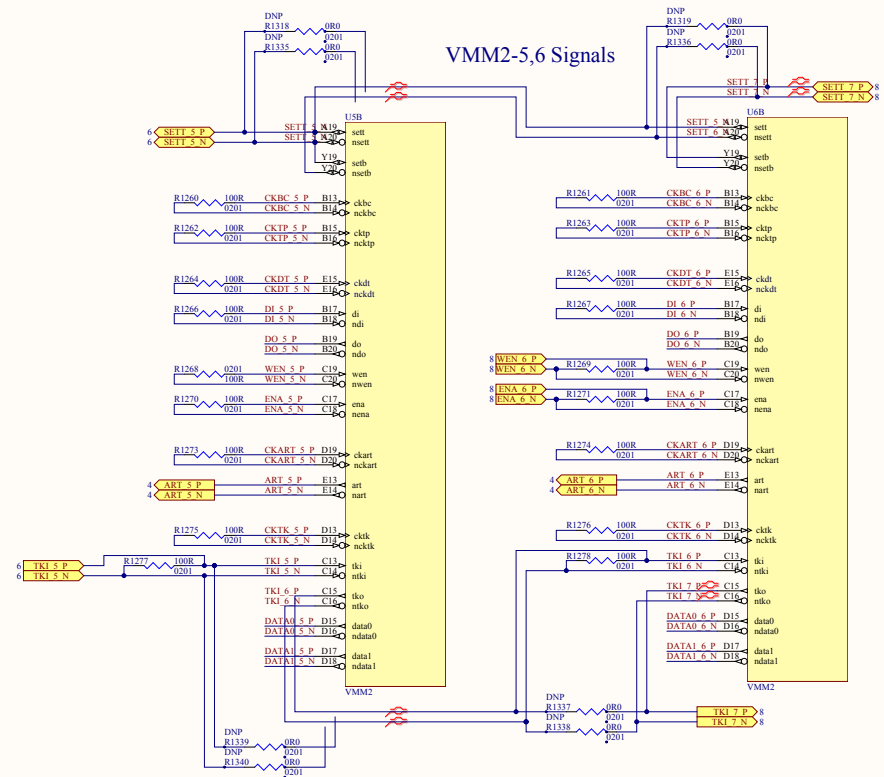


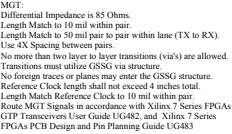
setb: ch0 neighbor trigger
ckbc: BC clock (timestamp Gray-code counter advance)
cktp: test pulse clock
di: configuration data input
do: configuration data output
tki: token input (in analog mode)
tko: token output (in analog mode)

ena: acquisition start/stop
ena high, wen low: acquisition is enabled
internally enabled after 40ns from ena high
in two-phase (analog) mode is acquisition
in continuous (digital) mode is acquisition and readout
ena low, wen low: in two-phase mode is readout
ena pulse, wen high: global reset (acquisition and registers)

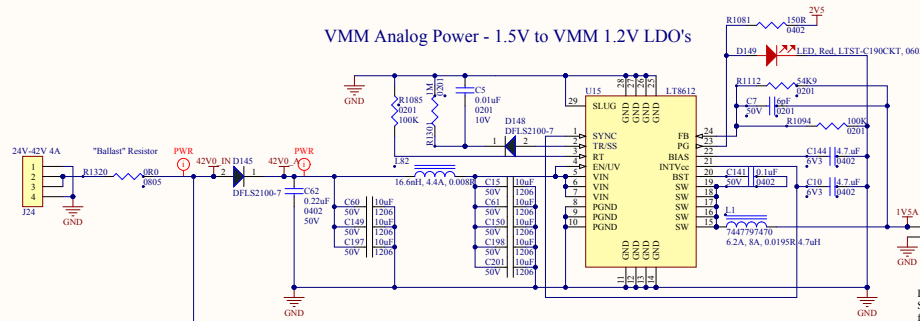
wen: configuration enable
wen high: configuration mode
wen pulse: acquisition reset (also resets BC counter)

cktk: token clock
data0: flag and first data line (flag and address in analog mode)
data1: second data line
ckart: ART clock
art: ART output
ckdt: configuration (data input), data output and 6-bit ADC clock
setb: ch63 neighbor trigger



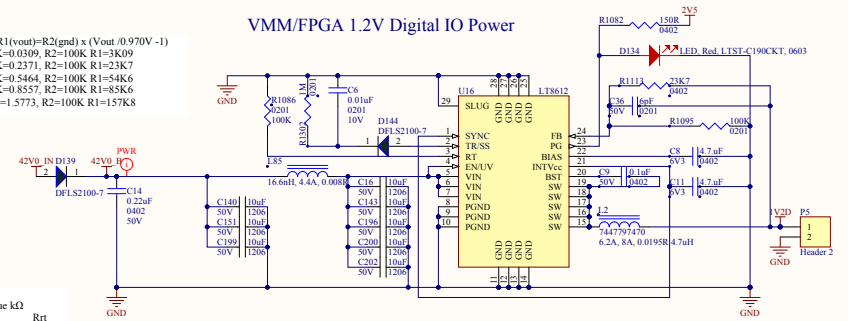


VMM Analog Power - 1.5V to VMM 1.2V LDO's



LT8612: R1(vout)=R2(gnd) x (Vout/0.970V -1)
 1.0V => K=0.0309, R2=100K R1=3K09
 1.2V => K=0.2371, R2=100K R1=23K7
 1.5V => K=0.5464, R2=100K R1=54K6
 1.8V => K=0.8557, R2=100K R1=85K6
 2.5V=> K=1.5773, R2=100K R1=157K8

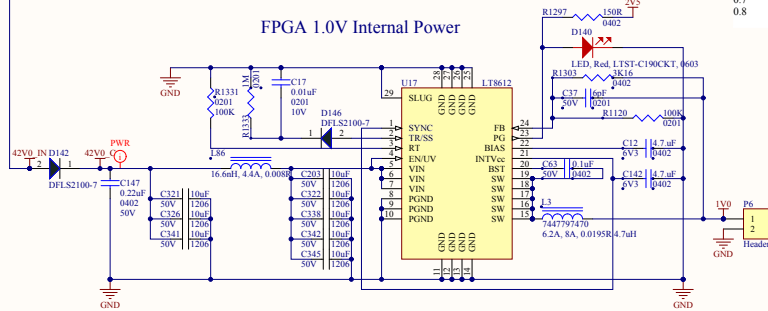
VMM/FPGA 1.2V Digital IO Power



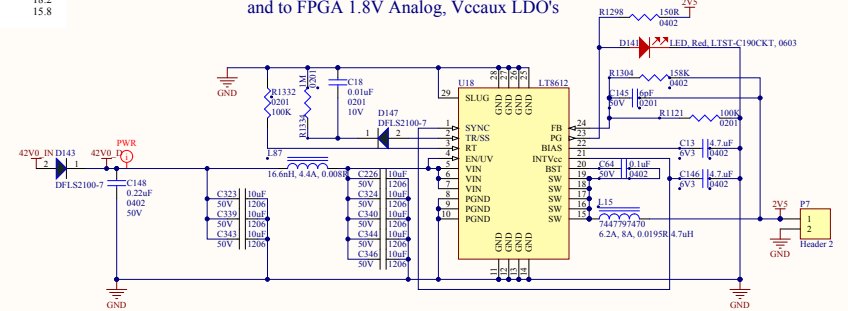
LT8612 Table 1.
 SW Freq MHz vs RT Value kΩ

fsw	Rrt	fsw	Rrt
0.2	232	1.0	41.2
0.3	150	1.2	33.2
0.4	110	14	28.0
0.5	88.7	1.6	23.7
0.6	71.5	1.8	20.5
0.7	60.4	2.0	18.2
0.8	52.3	2.2	15.8

FPGA 1.0V Internal Power



FPGA 2.5V Power - Supply to MGT 1.2V, MGT 1.0V LDO's and to FPGA 1.8V Analog, Vccaux LDO's



Power Estimates:

LT8612 #1 1.5Vanlg
 $I_{avg18} = 8 \times 0.42 I_{avg12} = 3.4A + \text{losses}$ (via ADP1755ACPZ-1-8)

LT8612 #2 1.2Vdgtl
 $I_{dgt12} = 8 \times 1.50 A_{idgt12} = 1.821A + \text{losses}$

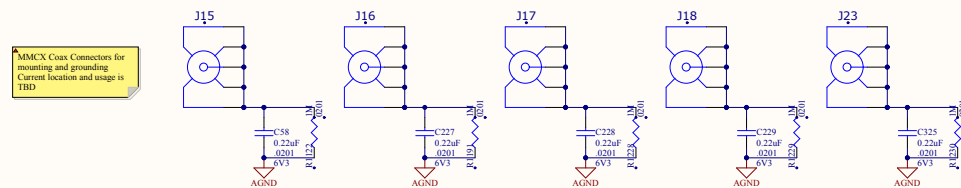
LT8612 #3 1.0Vfpga
 $I_{fpga10} = 3.15 A_{icent} + 0.100 A_{icram} = 3.65A + \text{losses}$

LT8612 #4 2.5Vfpga
 $I_{fpga25} = 0.621 A_{icco25} + 0.511 A_{imgtavecc10} + 36 A_{imgtvt} + 0.32 A_{ccaux} = 1.8A + \text{losses}$ (via ADP1755ACPZ-9)

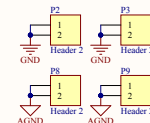
Note:
 $I_{ccaux}(\text{Vaux Quiescent}) = 7mA$
 $1.8V \text{ LVCMOS25 or 33} = 2-2.4mA \text{ per pin}$

1.2V SSTL / HSTL 8mA per pin max

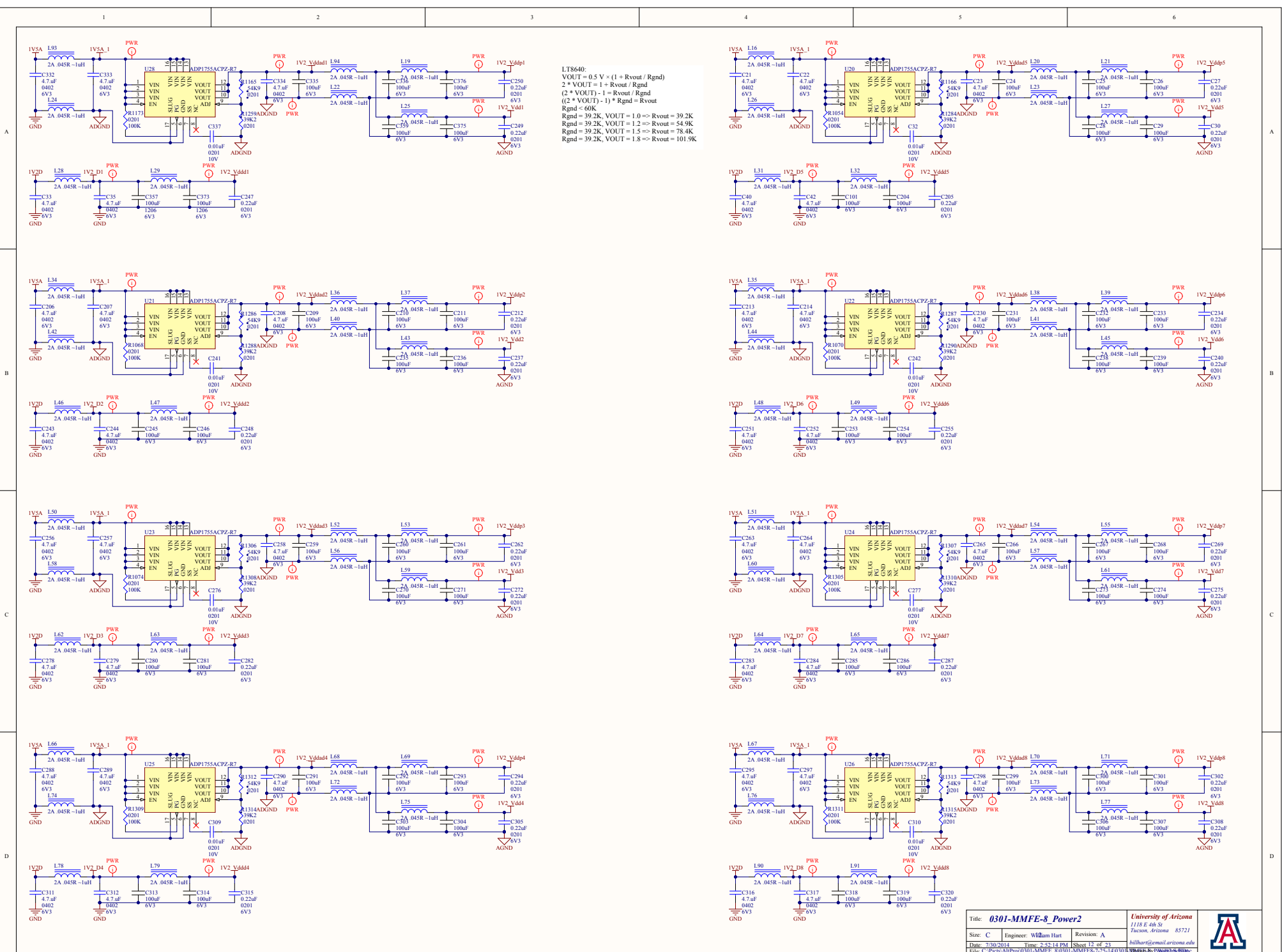
When laying out power, please route point to point first, with trace width sufficient to carry the required current.
 Pours or splits can then be instantiated afterwards, without fear of islands or choke points.
 This is especially critical for FPGA power distribution, and makes verification easier.



Ground Reference for Probes

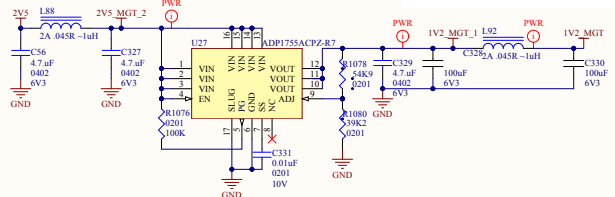
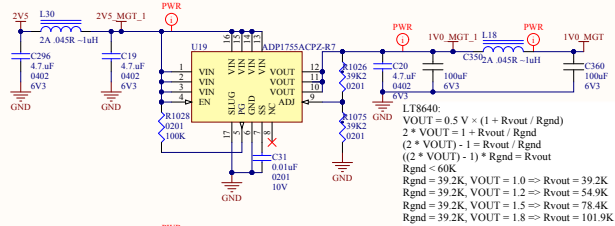


ESR:
 $DF = \tan(\phi) = ESR / X_c = 0.1 \text{ for CC}$
 $ESR = DF \times X_c = DF / (2\pi f \times C) = X_c / Q = \tan(\phi) \times X_c$
 $Z = (ESR^2 + (X_L - X_C)^2)^{0.5}$
 $f = 1 / (2\pi \times \sqrt{LC})^{0.5}$
 Spec for Al and Film caps @100kHz
 Spec for Al and Tant @120kHz
 $ESR = \text{Radiated}(30MHz) = \text{Rmetal}(30-300MHz)$
 $ESR2 = ESR1 \times (2/f1)^{0.5}$
 ESR calculations for ceramic caps use DF of 10%, mean/d @ 120 Hz, used @ 1MHz = 0.005Ohms worst case.

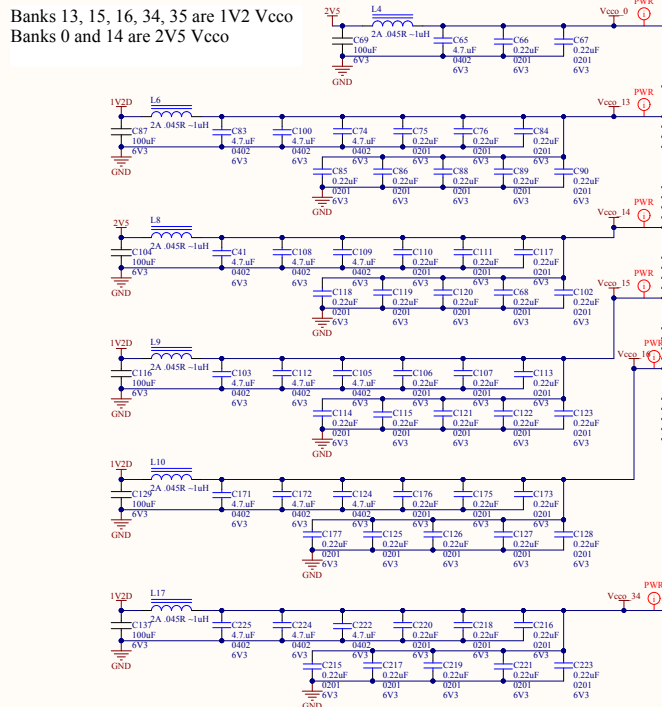


LT8640:
 $V_{OUT} = 0.5 V \times (1 + R_{out} / R_{gnd})$
 $2 \times V_{OUT} = 1 + R_{out} / R_{gnd}$
 $(2 \times V_{OUT}) - 1 = R_{out} / R_{gnd} = R_{out}$
 $R_{gnd} < 60K$
 $R_{gnd} = 39.2K, V_{OUT} = 1.0 \Rightarrow R_{out} = 39.2K$
 $R_{gnd} = 39.2K, V_{OUT} = 1.2 \Rightarrow R_{out} = 54.9K$
 $R_{gnd} = 39.2K, V_{OUT} = 1.5 \Rightarrow R_{out} = 78.4K$
 $R_{gnd} = 39.2K, V_{OUT} = 1.8 \Rightarrow R_{out} = 101.9K$

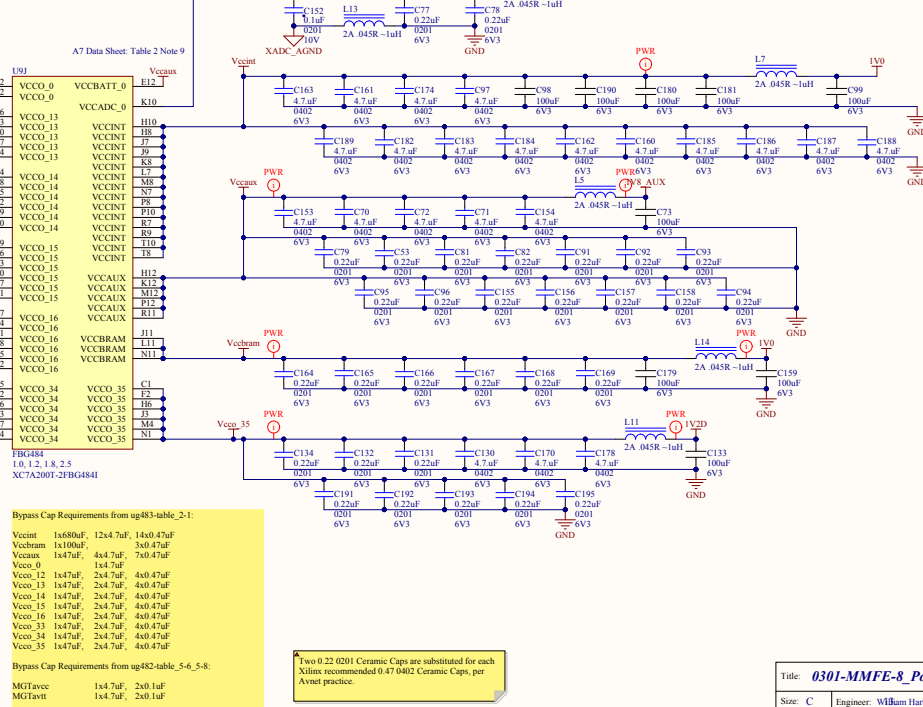




Banks 13, 15, 16, 34, 35 are 1V2 Vcco
 Banks 0 and 14 are 2V5 Vcco



A7 Data Sheet, Table 2 Note 9



Bypass Cap Requirements from ug483-table 2-1:

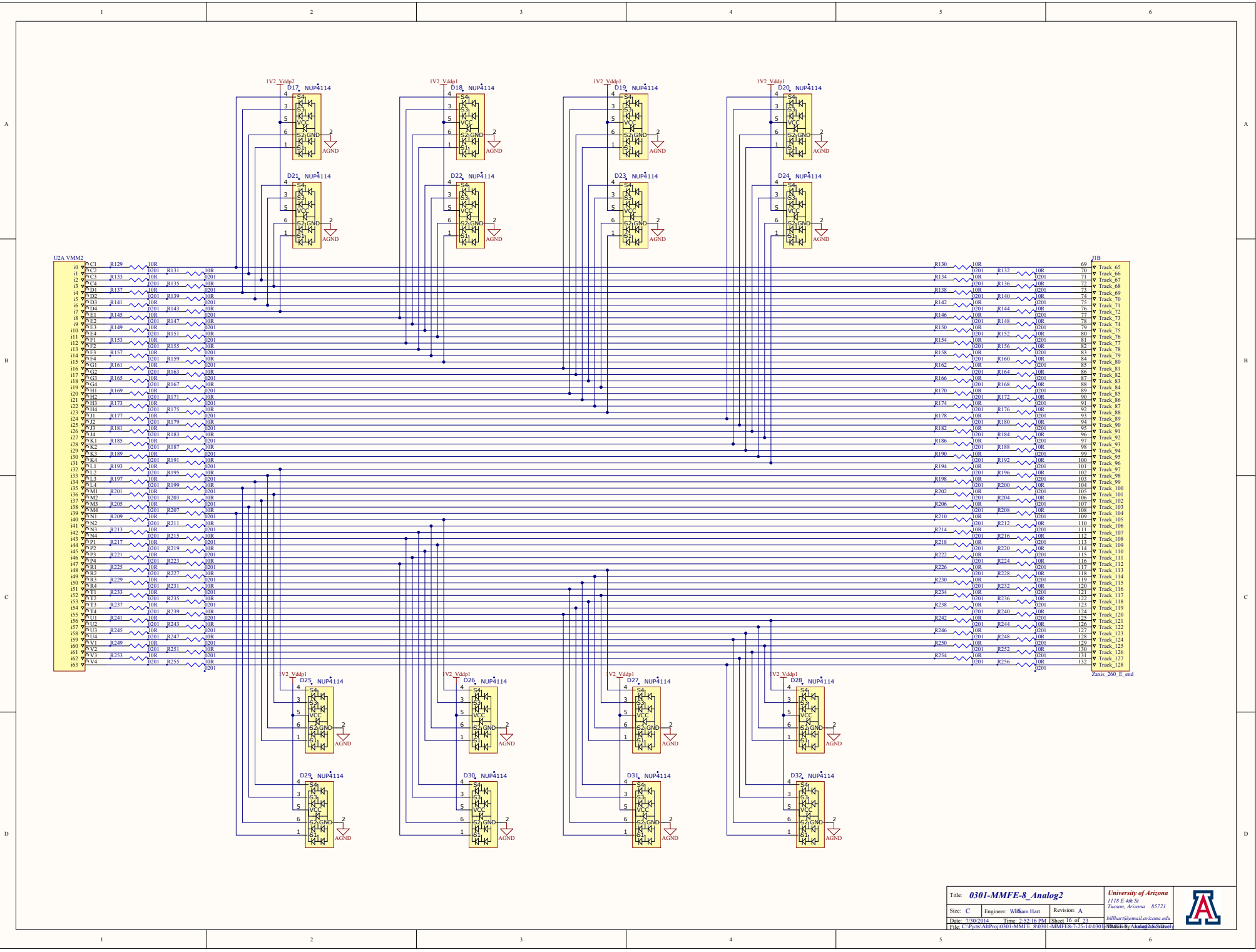
Vccin	1x680uF	12x4.7uF	1x40.47uF
Vccbram	1x100uF	3x0.47uF	
Vccaux	1x47uF	4x4.7uF	7x0.47uF
Vcco_0	1x47uF	1x4.7uF	
Vcco_12	1x47uF	2x4.7uF	4x0.47uF
Vcco_13	1x47uF	2x4.7uF	4x0.47uF
Vcco_14	1x47uF	2x4.7uF	4x0.47uF
Vcco_15	1x47uF	2x4.7uF	4x0.47uF
Vcco_16	1x47uF	2x4.7uF	4x0.47uF
Vcco_34	1x47uF	2x4.7uF	4x0.47uF
Vcco_35	1x47uF	2x4.7uF	4x0.47uF

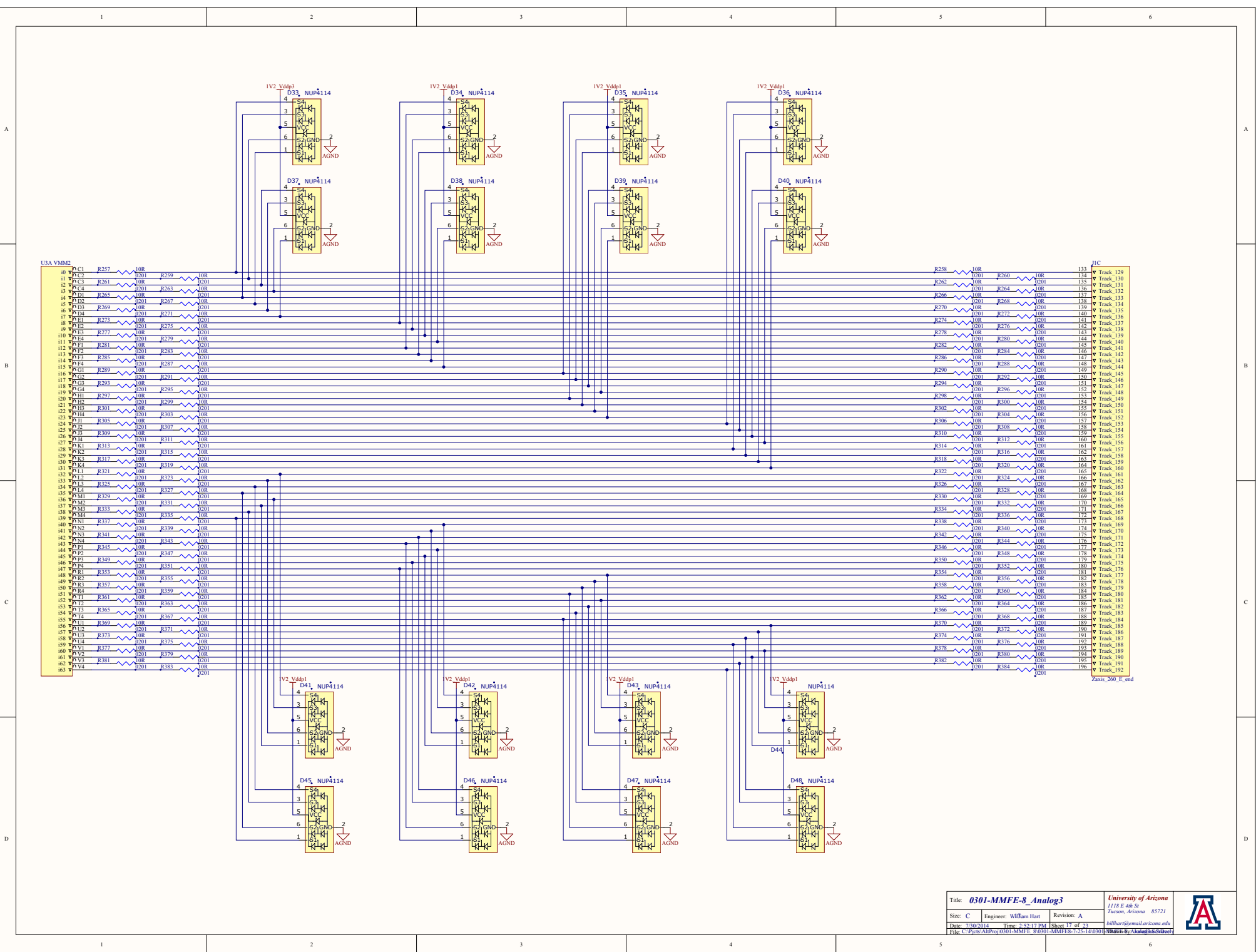
Bypass Cap Requirements from ug482-table 5-4, 5-8:

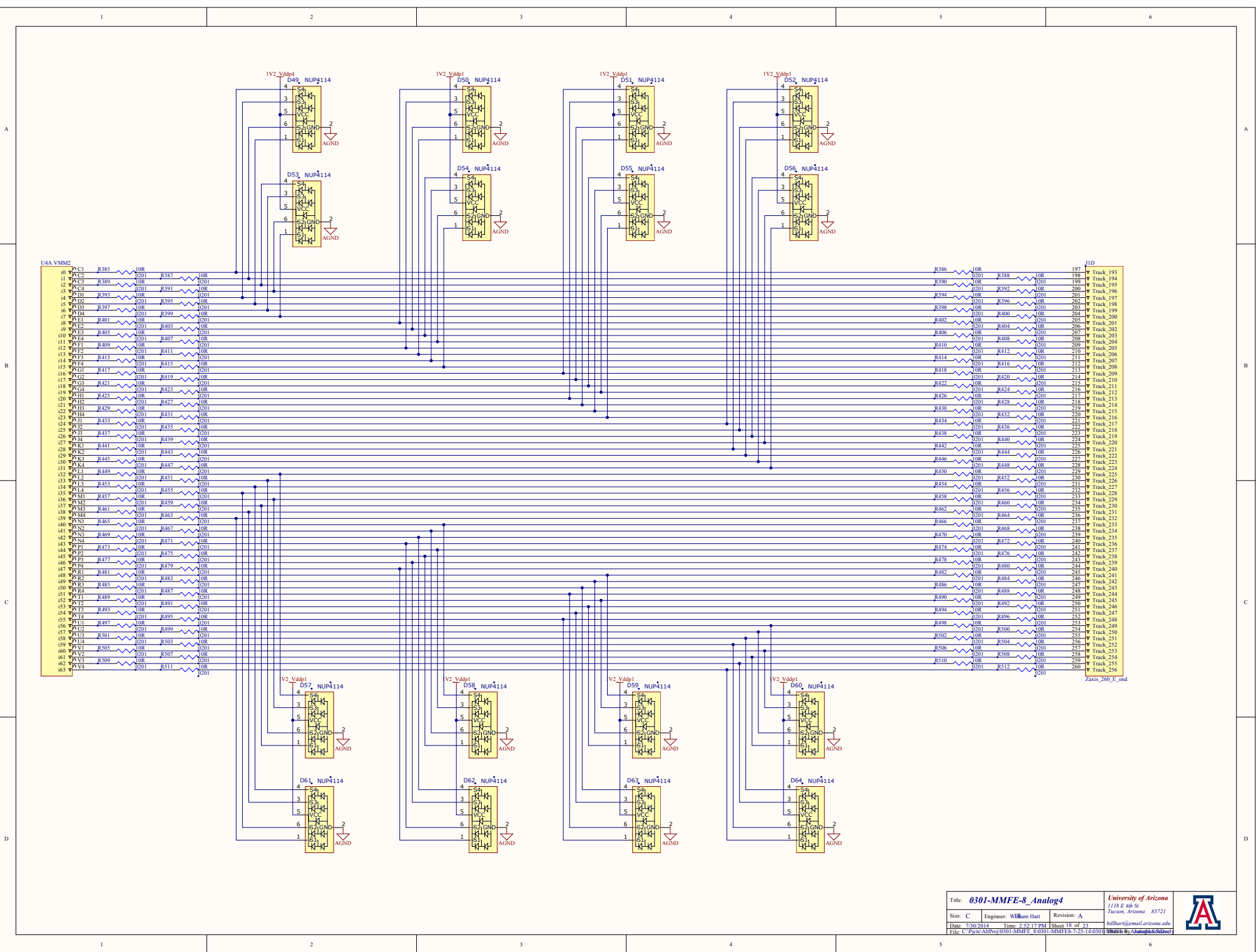
MGTAve	1x4.7uF	2x0.1uF
MGTAvt	1x4.7uF	2x0.1uF

Bypass Cap Requirements from ug480:

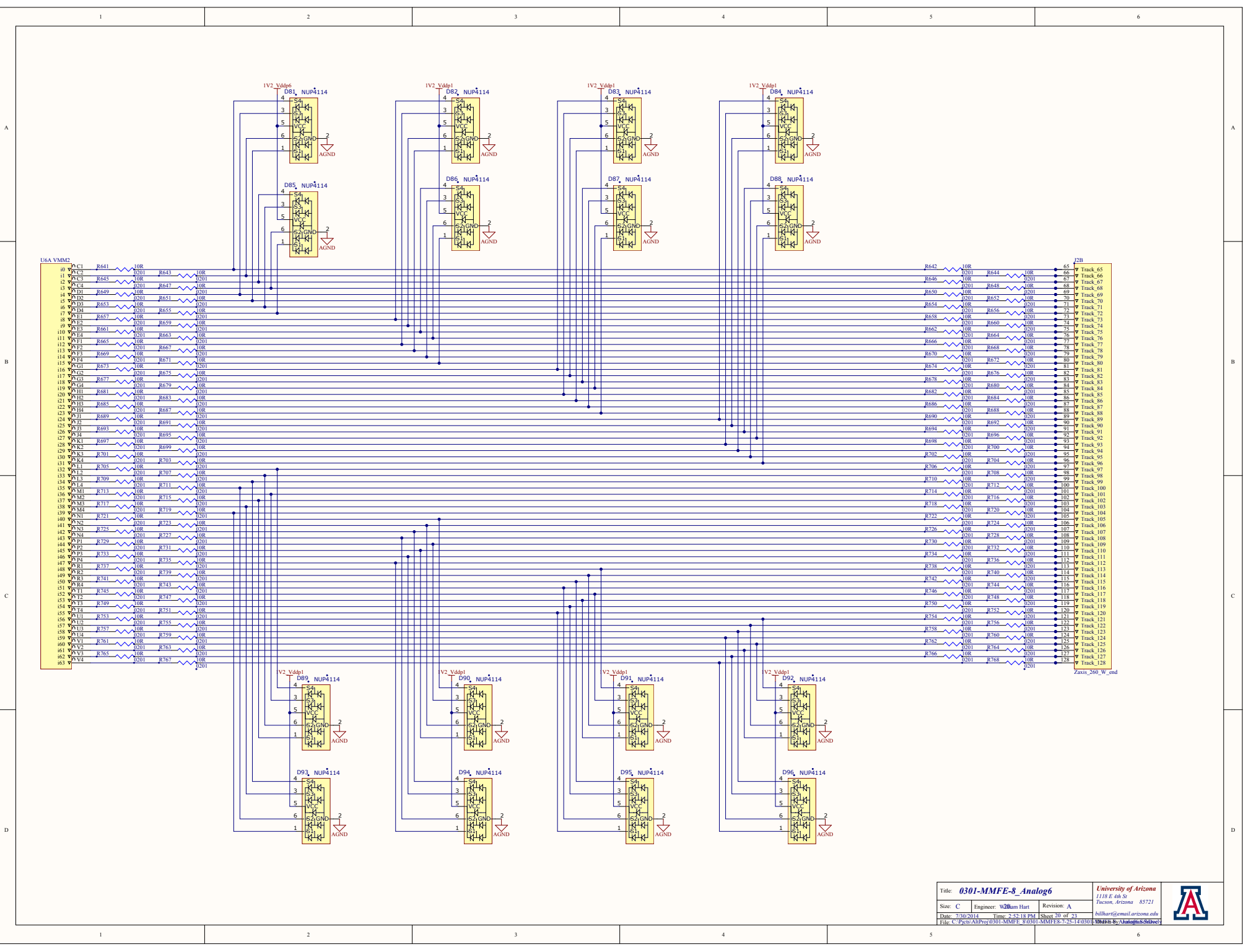
A2	GND	H7
A3	GND	H9
A4	GND	H11
A5	GND	H12
A6	GND	H13
A7	GND	H14
A8	GND	H15
A9	GND	H16
A10	GND	H17
A11	GND	H18
A12	GND	H19
A13	GND	H20
A14	GND	H21
A15	GND	H22
A16	GND	H23
A17	GND	H24
A18	GND	H25
A19	GND	H26
A20	GND	H27
A21	GND	H28
A22	GND	H29
A23	GND	H30
A24	GND	H31
A25	GND	H32
A26	GND	H33
A27	GND	H34
A28	GND	H35
A29	GND	H36
A30	GND	H37
A31	GND	H38
A32	GND	H39
A33	GND	H40
A34	GND	H41
A35	GND	H42
A36	GND	H43
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A38	GND	H45
A39	GND	H46
A40	GND	H47
A41	GND	H48
A42	GND	H49
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A45	GND	H52
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A380	GND	H387
A381	GND	H388
A382	GND	H389
A383	GND	H390
A384	GND	H391
A385	GND	H392
A386	GND	H393
A387	GND	H394
A388	GND	H395
A389	GND	H396
A390	GND	H397
A391	GND	H398
A392	GND	H399
A393	GND	H400
A394	GND	H401
A395	GND	H402
A396	GND	H403
A397	GND	H404
A398	GND	H

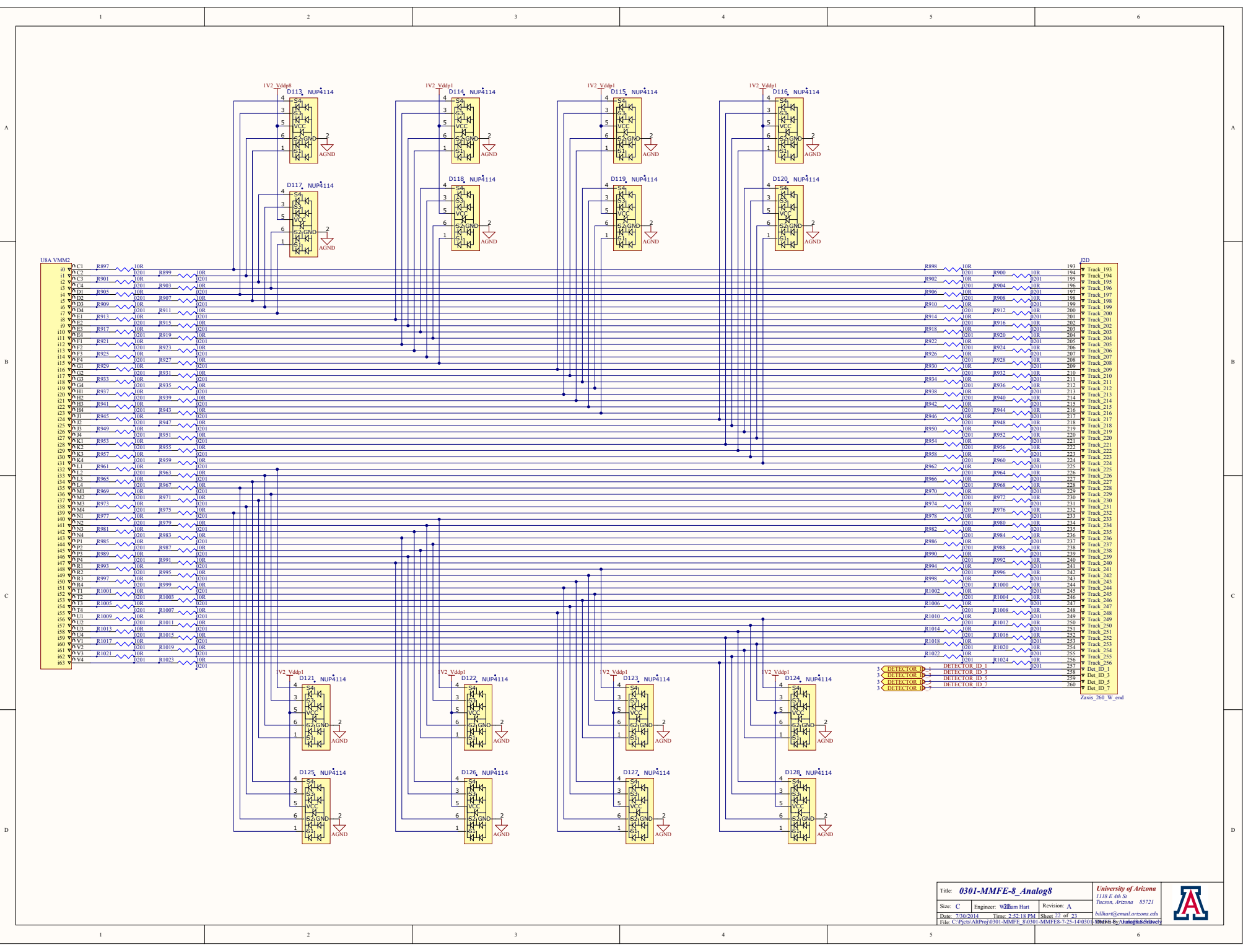






Xaxis: 260.0 E_end





[illegible]

