Contents

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5-22-2014

Figures

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1. Introduction

1.1. Theory of operation

Something here about how the unit operates, block diagrams, etc.

1.2. Relevant Documents

Schematic, board layout, etc. (Put hyperlinks here)

1.3. Production Forecast:

1.3.1. Demonstrator

5-10 units

Schedule dates

1.3.2. Prototype

5-10 units

HALT on 1 unit. Designed experiments on a few cards to determine ESS guidelines

1.3.3. LRIP

200 units

Partial ESS Screen- 10%.

1.3.4. Full Production

4700 units

Full ESS Screen on a QA sample

Final test Limits to be determined after LRIP via SPC analysis

2. Electrical Interfaces:

2.1. Pinout

2.2. Electrical Stimulus Requirements

2.2.1. Input Power Forms

2.2.2. Loads

2.2.3. Serial Interfaces

L1DDC Data/TTC Interface:

The DUT uses a bidirectional 80Mb/s serial interface to provide Level 1 readout data uplinks to the L1DDC card. The DUT also receives trigger, timing and control (TTC) downlinks on this interface.

L1DDC SCA Interface:

The DUT uses a bidirectional 80Mb/s serial interface to facilitate calibration, configuration, and monitoring downlinks and uplinks to and from the L1DDC card.

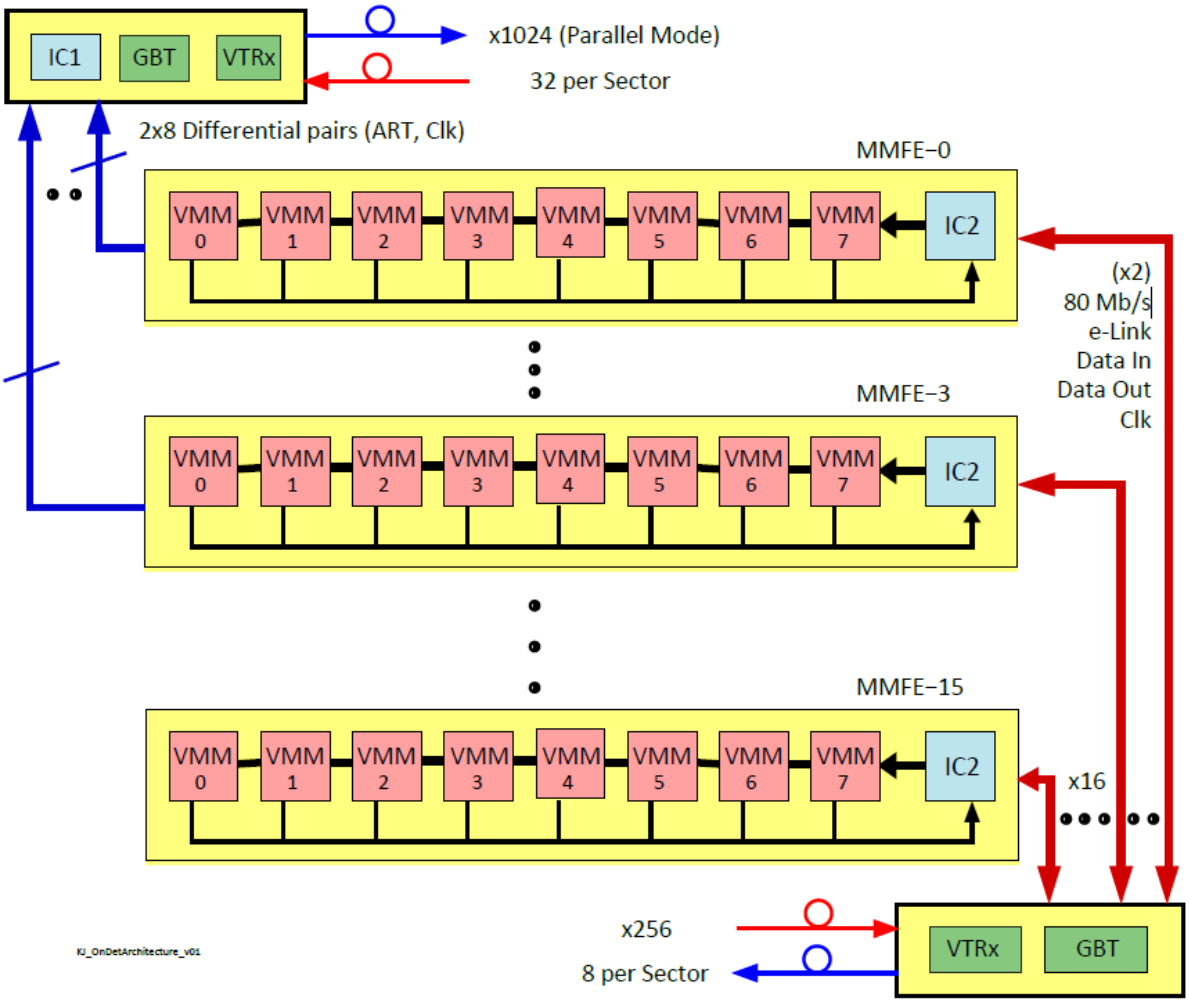

Figure 1: ***MM Front-end Level-1 data and trigger readout boards***

ART Data Interface 1-8:

The DUT uses 8 unidirectional interfaces to provide address and real time (ART) data uplinks to the ADDC card. Each interface consists of an ART data differential pair and a clock differential pair.

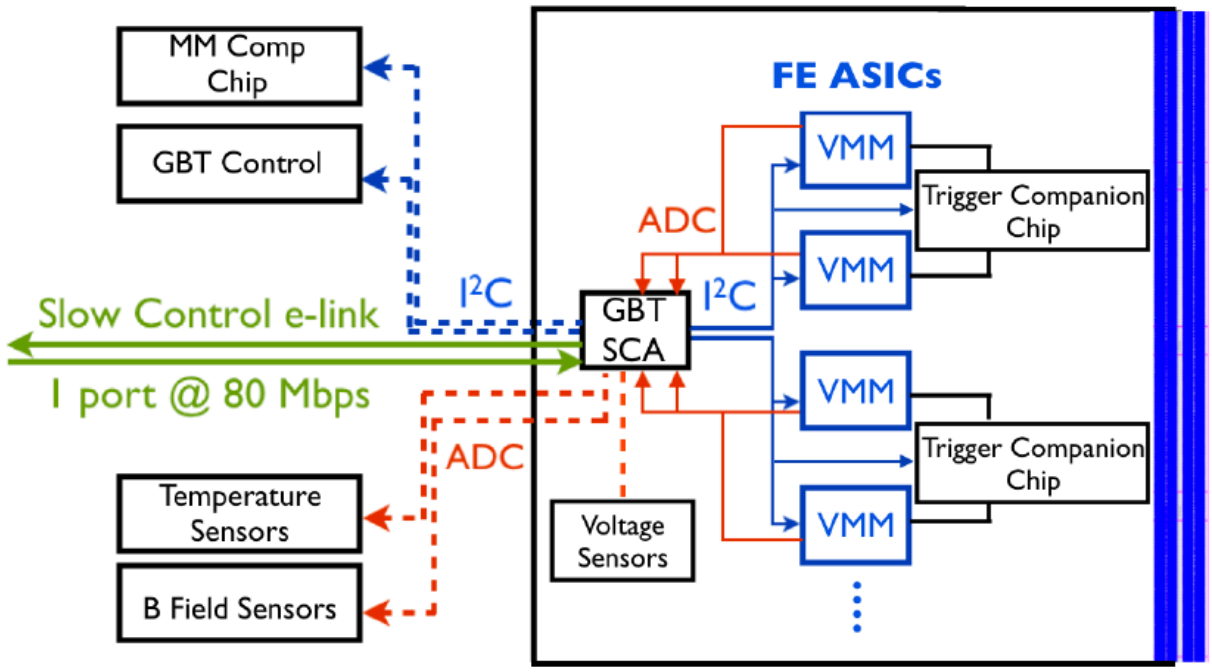

Figure 2: ***SCA Connections on the MMFE8 and to External Systems***

MORE DETAIL NEEDED

2.2.4. Analog Inputs

3. Tests:

3.1. Initial Powerup

3.1.1. Test # XXXX: +24V Initial Input Current

USL: TBD Adc

Nom: TBD Adc

LSL: TBD Adc

Description: Measure current on +24V power form > 1s after the first application of power forms in 2.2.1.

3.1.2. Test # XXXX: Configure FPGA

USL: N/A

Nom: TBD

LSL: N/A

Description: Load FPGA through ??? interface. Readback checksum and compare with expected value.

3.2. Power Form Tests

3.2.1. Test # XXXX: +24V Input Current

USL: TBD Adc

Nom: TBD Adc

LSL: TBD Adc

Description: Measure current on +24V power form > 1s after application of FPGA configuration.

3.2.2. Test # XXXX: 1p8Va Output Voltage

USL: +5%

Nom: +1.8Vdc

LSL: -5%

Description: Measure voltage on 1p8Va power form >1s after application of power forms in 2.2.1.

3.2.3. Test # XXXX: 1p8Vd Output Voltage

USL: +5%

Nom: +1.8Vdc

LSL: -5%

Description: Measure voltage on 1p8Vd power form > 1s after application of power forms in 2.2.1.

3.2.4. Test # XXXX: 1p0V Output Voltage

USL: +5%

Nom: +1.0Vdc

LSL: -5%

Description: Measure voltage on 1p0V power form > 1s after application of power forms in 2.2.1.

3.2.5. Test # XXXX: 2p5V Output Voltage

USL: +5%

Nom: +2.5Vdc

LSL: -5%

Description: Measure voltage on 2V5 power form > 1s after application of power forms in 2.2.1.

3.3. Test # XXXX: ASIC Configuration

USL: N/A

Nom: N/A

LSL: N/A

Description: All ASICs on the DUT must configure successfully

3.4. VMM Configuration

3.4.1. Test # XXXX: Configure VMM 1

USL: N/A

Nom: N/A

LSL: N/A

Description: Load a configuration stream to VMM1. Read back the configuration stream and verify that it matches the loaded stream.

3.4.2. Test # XXXX: Configure VMM 2

USL: N/A

Nom: N/A

LSL: N/A

Description: Load a configuration stream to VMM2. Read back the configuration stream and verify that it matches the loaded stream.

3.4.3. Test # XXXX: Configure VMM 3

USL: N/A

Nom: N/A

LSL: N/A

Description: Load a configuration stream to VMM3. Read back the configuration stream and verify that it matches the loaded stream.

3.4.4. Test # XXXX: Configure VMM 4

USL: N/A

Nom: N/A

LSL: N/A

Description: Load a configuration stream to VMM4. Read back the configuration stream and verify that it matches the loaded stream.

3.4.5. Test # XXXX: Configure VMM 5

USL: N/A

Nom: N/A

LSL: N/A

Description: Load a configuration stream to VMM5. Read back the configuration stream and verify that it matches the loaded stream.

3.4.6. Test # XXXX: Configure VMM 6

USL: N/A

Nom: N/A

LSL: N/A

Description: Load a configuration stream to VMM6. Read back the configuration stream and verify that it matches the loaded stream.

3.4.7. Test # XXXX: Configure VMM 7

USL: N/A

Nom: N/A

LSL: N/A

Description: Load a configuration stream to VMM7. Read back the configuration stream and verify that it matches the loaded stream.

3.4.8. Test # XXXX: Configure VMM 8

USL: N/A

Nom: N/A

LSL: N/A

Description: Load a configuration stream to VMM8. Read back the configuration stream and verify that it matches the loaded stream.

3.5. MMFE Functional Tests: VMM Pulsar Set 1- Configuration 1

3.5.1. Test # XXXX: Amplitude Set 1, Configuration 1, [Channel X]

USL: +5%

Nom: TBD

LSL: -5%

Description:

Configure the test pulse DAC to 1V and the global threshold DAC to 0.5V. Configure the channel gain to TBD mV/fC and connect the channel self test capacitor. Enable the VMM internal pulsar for approximately TBD ms.

Pull the channel amplitude data via a L1 Accept. Calculate the mean of the amplitude data and compare to specification data.

3.5.2. Test # XXXX: Time Set 1, Configuration 1, [Channel X]

USL: +5%

Nom: TBD

LSL: -5%

Description: Using the VMM internal pulsar to test ¼ of available channels verify the time of a detected pulse.

3.5.3. Test # XXXX: Crosstalk Amplitude Set 1, Configuration 1, [Channel X]

USL: 50% of Nominal Amplitude

Nom: 0

LSL: N/A

Description:

Configure the MMFE in neighbor trigger mode. Configure the VMM global test pulse DAC to TBD and the global threshold DAC to TBD. Configure the channel gain to TBD mV/fC and connect the channel self test capacitor. Enable the VMM internal pulsar for approximately TBD ms.

Perform a L1 Accept to collect the detected amplitude of the neighboring channels. Determine the mean amplitudes of the detected pulses on the neighboring channels. Compare largest amplitude mean to limit.

3.6. Test # XXXX: FEB Generated System Clock

USL: N/A

Nom: N/A

LSL: N/A

Description: A system clock is established on the DUT via a clock sent from the Test Bench board

3.7. FEB ART Uplink Tests

3.7.1. Test # XXXX: FEB ART Uplink 1

USL: N/A

Nom: N/A

LSL: N/A

Description: Configure channel 1 of the MMFE to trigger on a 1V signal from VMM1's internal pulsar. Enable the internal pulsar. Verify that the received ART data indicates that Channel 1 triggered.

3.7.2. Test # XXXX: FEB ART Uplink 2

USL: N/A

Nom: N/A

LSL: N/A

Description: Configure channel 65 of the MMFE to trigger on a 1V signal from VMM2's internal pulsar. Enable the internal pulsar. Verify that the received ART data indicates that Channel 65 triggered.

3.7.3. Test # XXXX: FEB ART Uplink 3

USL: N/A

Nom: N/A

LSL: N/A

Description: Configure channel 129 of the MMFE to trigger on a 1V signal from VMM3's internal pulsar. Enable the internal pulsar. Verify that the received ART data indicates that Channel 129 triggered.

3.7.4. Test # XXXX: FEB ART Uplink 4

USL: N/A

Nom: N/A

LSL: N/A

Description: Configure channel 193 of the MMFE to trigger on a 1V signal from VMM4's internal pulsar. Enable the internal pulsar. Verify that the received ART data indicates that Channel 193 triggered.

3.7.5. Test # XXXX: FEB ART Uplink 5

USL: N/A

Nom: N/A

LSL: N/A

Description: Configure channel 257 of the MMFE to trigger on a 1V signal from VMM5's internal pulsar. Enable the internal pulsar. Verify that the received ART data indicates that Channel 257 triggered.

3.7.6. Test # XXXX: FEB ART Uplink 6

USL: N/A

Nom: N/A

LSL: N/A

Description: Configure channel 321 of the MMFE to trigger on a 1V signal from VMM6's internal pulsar. Enable the internal pulsar. Verify that the received ART data indicates that Channel 321 triggered.

3.7.7. Test # XXXX: FEB ART Uplink 7

USL: N/A

Nom: N/A

LSL: N/A

Description: Configure channel 385 of the MMFE to trigger on a 1V signal from VMM7's internal pulsar. Enable the internal pulsar. Verify that the received ART data indicates that Channel 385 triggered.

3.7.8. Test # XXXX: FEB ART Uplink 8

USL: N/A

Nom: N/A

LSL: N/A

Description: Configure channel 449 of the MMFE to trigger on a 1V signal from VMM8's internal pulsar. Enable the internal pulsar. Verify that the received ART data indicates that Channel 449 triggered.

3.8. Test # XXXX: Outlier Channel Count

USL: TBD

Nom: N/A

LSL: N/A

Description:

Configure the global test pulse DAC to 1V and the global threshold DAC to 0.5V. Set all channel gains to TBD mV/fC and connect all self test capacitors. Enable the test pulsar for approximately TBD seconds. Pull hit data from the MMFE via a L1 Accept. Calculate mean and standard deviation for the count data for all channels. Count all outliers that are greater than the mean by more than 3 sigma. The number of outliers detected in this step will be referred to as A_Counts.

Disable the channels described above as outliers. Re-enable the test pulsar for approximately TBD seconds. Calculate mean and standard deviation for the count data with the previously identified outlier channels excluded. Count all channels with amplitudes that are greater than 2 sigma from the mean of all non-outlier channels. This channel count will referred to as B_Counts.

Compare A_Counts+B_Counts to specification.

ADD MEAN CHECK

3.9. Test # XXXX: FEB L1 Accept Uplink

USL: N/A

Nom: N/A

LSL: N/A

Description: L1 Accept data is transmitted from the DUT to TE and the received data is equal to the expected data.

3.10. Test # XXXX: Flash Configuration

USL: N/A

Nom: TBD

LSL: N/A

Description: If all other tests have passed, load configuration file into flash memory through ??? interface. Readback the checksum and compare against the expected value.

3.11. Test # XXXX: Continuity

USL: N/A

Nom: N/A

LSL: N/A

Description: Placeholder for continuity tests

4. Environmental Tests

4.1. HALT Test

A highly accelerated life test will be performed on one prototype DUT. This test will expose design flaws that impact the reliability of the DUT and enable characterization of safe operating temperatures of the DUT. The results of this test will be used to set the test temperatures to be used during environmental stress screening (ESS).

4.2. Burn-in Characterization

A designed experiment will be performed on 5-10 DUTs during LRIP to determine appropriate burn-in conditions (burn-in time, ambient temperature, etc.). This burn-in will be used to screen the first lot of hardware during LRIP. Significant failures during burn-in may necessitate a burn-in testing of DUTs during full production. Lack of failures may cause burn-in to be omitted from QA screens of production DUTs.

4.3. ESS

Environmental stress screens of all hardware will be performed during LRIP.

4.3.1. Temperature Screens

DUTs will be tested at elevated and depressed temperatures. The temperatures that the DUT will be subjected to will be determined by HALT testing in the prototype phase.

4.3.2. Vibration Tests

DUTs may be subjected to random vibration. The vibration levels that the DUT will be subjected to will be determined by HALT testing in the prototype phase.

4.4. QA Screens

Burn-in and ESS tests will be performed on a random sampling of each lot. The size of the sample will be determined so as to not impact the production rate.

5. Acronyms

ADDC- ART Data Driver Card

ART- Address and Real Time Data

ASIC- Application Specific Integrated Circuit

DUT- Device Under Test

FEB- Front End Board

ESS- Environmental Stress Screen

HALT- Highly Accelerated Life Test

LRIP- Low Rate Initial Production

L1DDC- Level 1 Data Driver Card

QA- Quality Assurance

SCA- Slow Control ASIC

TE- Test Equipment

TTC- Trigger Timing Control