Preliminary MMFE-8 Specification

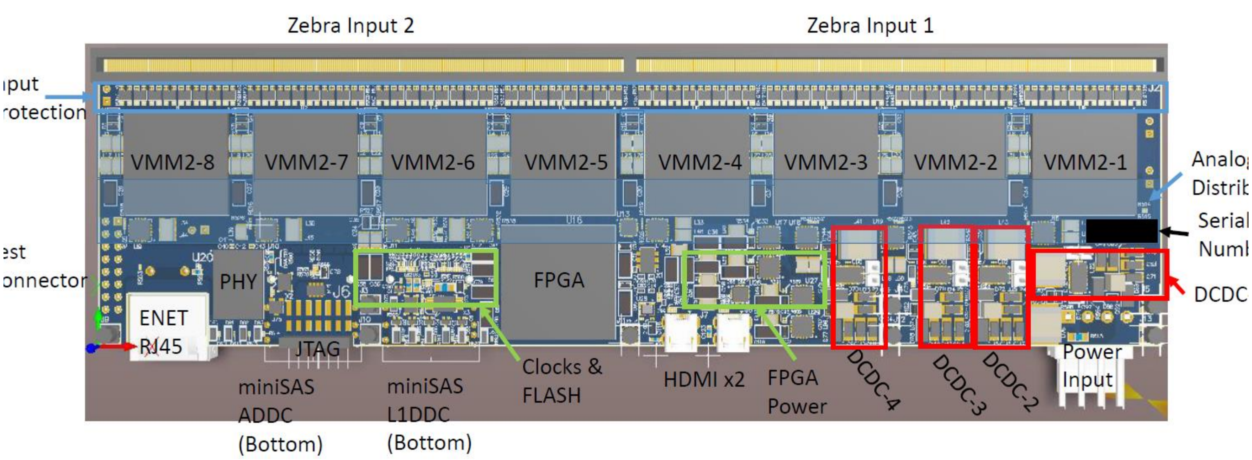
Introduction

The MMFE-8 board is the front-end electronics for ATLAS Micromegas (MM) detectors. It is the interface between the MM detectors and the trigger (ADDC) and data acquisition (L1DDC) electronics. The “-8” refers to the fact that the front-end card contains eight VMM ASIC’s. The VMM ASIC performs amplification and shaping, peak finding and digitization of the MM detector signal. In this document we distinguish between the MMFE-8 Demonstrator board and the MMFE-8 Production board. The former uses an FPGA (Xilinx Artix XC7A200T-2FBG484I) for VMM configuration, control, readout and GbEthernet output. The latter uses two companion ASIC’s, the SCA (Slow Control ASIC) and ROC (ReadOut Companion) in place of the FPGA and there is no GbEthernet output.

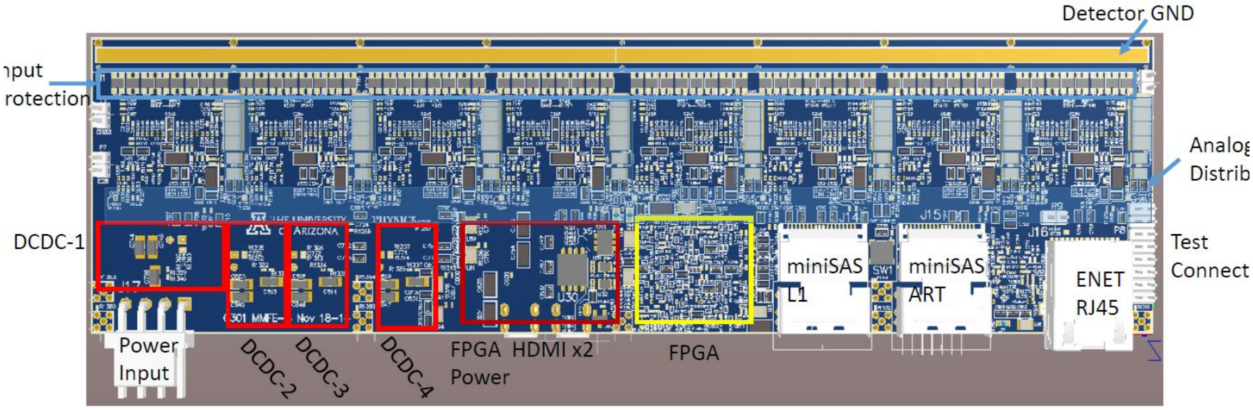
The first part of this document describes the MMFE-8 Demonstrator and the second part briefly describes the MMFE-8 Production board. The latter is less well-defined because the specifications for the Production VMM, SCA and ROC are still being developed. The Production power scheme is also under active R&D.

We don’t have the nice, detailed block diagrams typically associated with CERN electronics. We do however provide the schematics for the MMFE-8 Demonstrator that show all the signals and connections. The schematics and layout can be at https://svnweb.cern.ch/cern/wsvn/NSWELX/MMFE-8/0301-MMFE8-DEMO-V1-PDF/?#a3619990a76a8df81732ed9291b1b657c

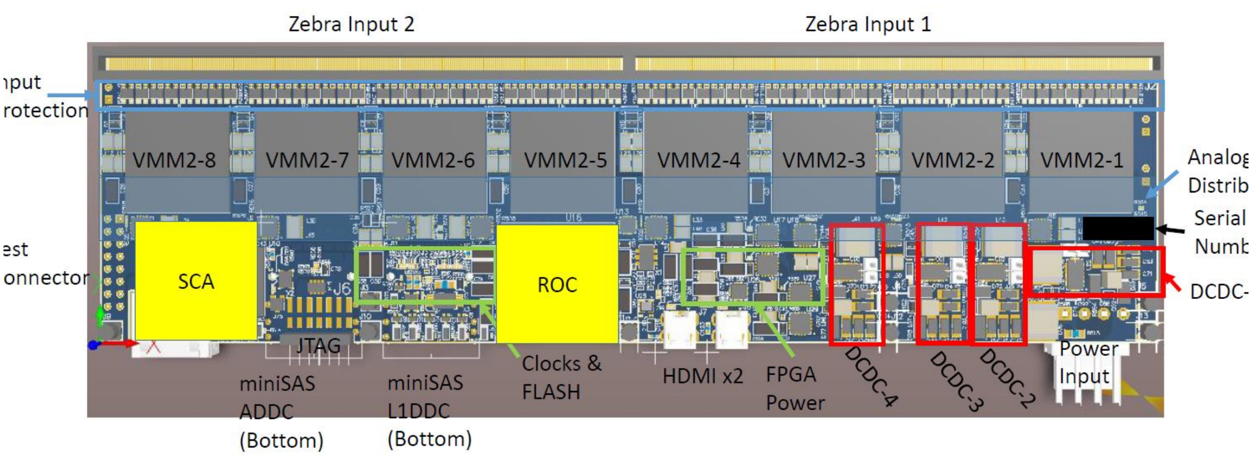
A top parts placement view of the MMFE-8 Demonstrator board is shown in Figure 1 below.



A bottom parts placement view of the MMFE-8 Demonstrator is shown in Figure 2 below.



A cartoon parts placement view of the MMFE-8 Production board is shown in Figure 3 below.



Mechanical considerations

Size: 215mm x 60mm x 2.54mm

Layers: 14

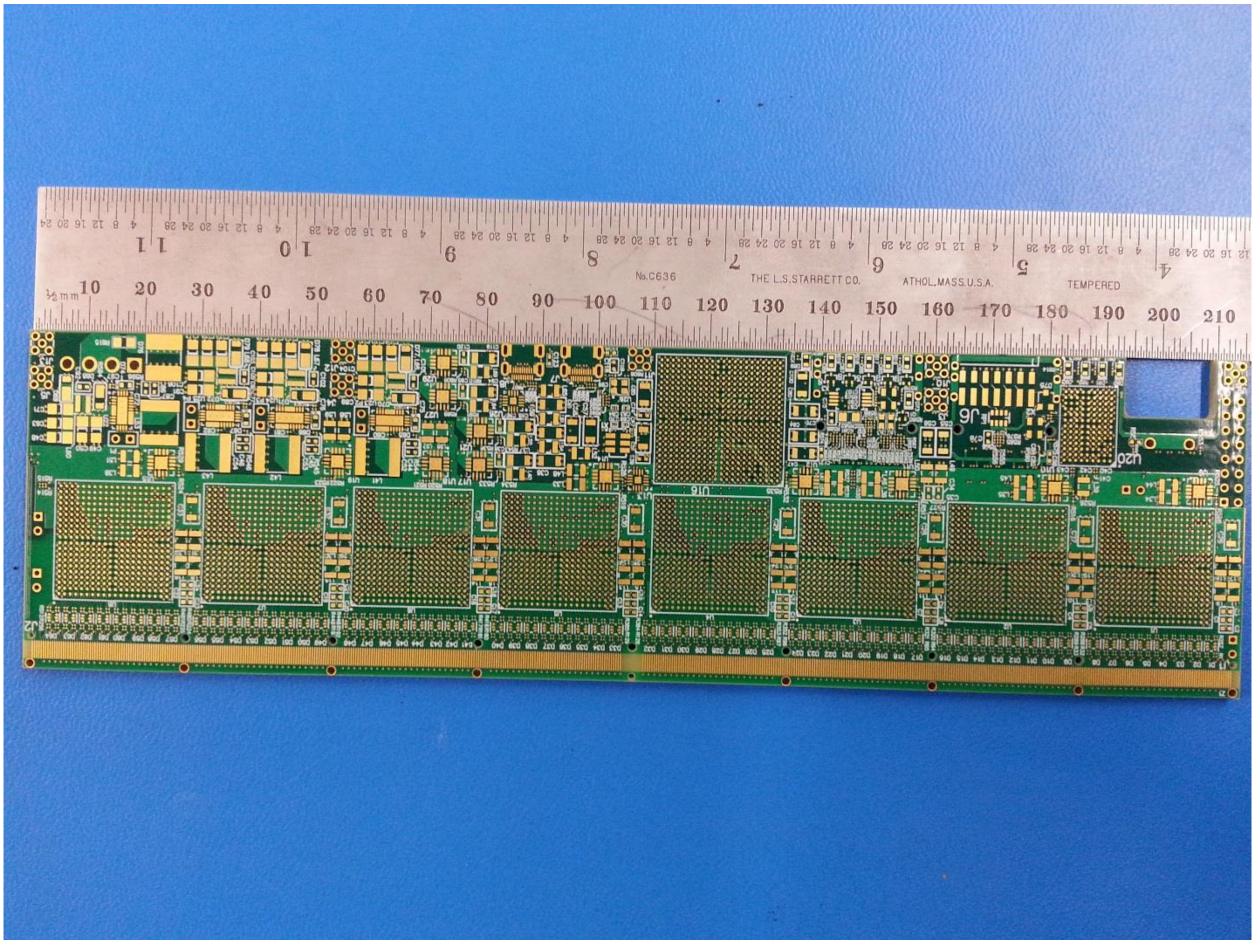
Components that must be cooled are placed on the ASIC side (defined as the top of the board). Cooling will not be covered in this document.

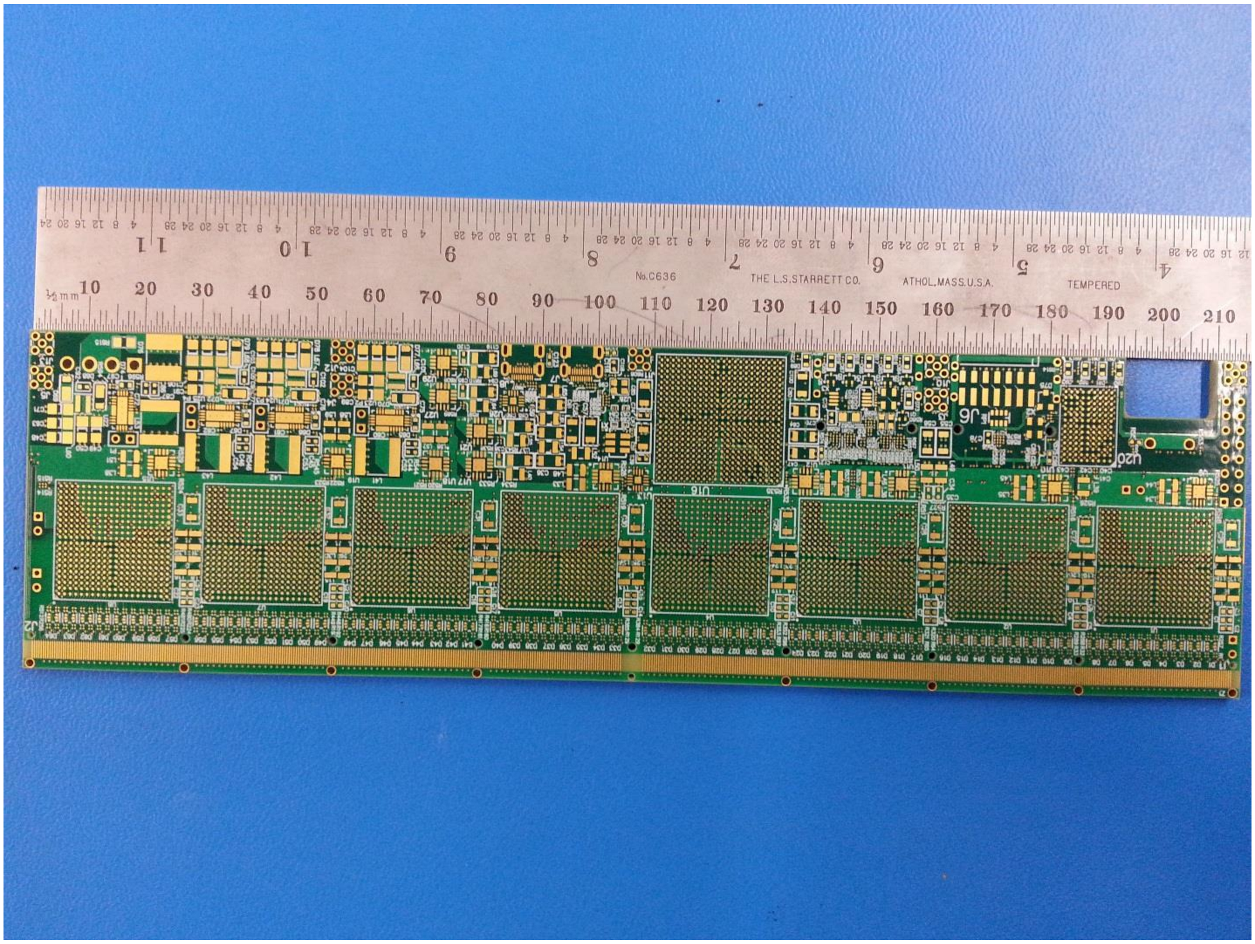
Two Zebra connectors and holders are located on the top of board. The Zebra connectors themselves are 110 mm x 6.30 mm x 2.50 mm. The wire pitch is 100 um and the wire width is 50 um, which can be compared to the MM pad pitch of 400 um and pad width of 200 um.   Each Zebra connector mates to 256 MM channels. There are four additional channels on each Zebra connector that are used for MM ID. The MM ID is determined by shorting the ID lines to ground on the detector side. There is an internal pull-up on the FPGA side. Significant R&D work remains to be carried out investigating the robustness of these connectors.

A detector GND pad of size of 215 mm x 10 mm exists on the bottom of MMFE-8 board under the Zebra connector (which is on the top of the board).

Components requiring access like switches, connectors, LED's, power side chip inductors (used for measuring current) are generally placed on the bottom of the board.

Pictures of the unpopulated MMFE-8 Demonstrator PCB (V1) are shown in Figures 4 and 5 below.





Power

This section describes the power scheme for the MMFE-8 Demonstrator only.

A proposal for the power for the MMFE-8 Production board is described in a separate document by the University of Michigan (UM). Their proposal uses a design based on the FEAST ASIC from CERN for DC-DC conversion. This is because UM has found that neither the LT8612 nor the ADP1755 are robust against proton radiation. In the proposal, additional filtering is used to compensate for the loss of the ADP1755 LDO’s, which are also not robust against proton radiation.

The Demonstrator power is shown on sheets 11-14 of the schematic.

The input connector is a standard 4 pin male with 0.156” centers.

Over voltage protection is provided by ST TVS_STIEC45-24AS 48/24V clamping diodes.

The input DC voltage can be 3.4-42V, 6A.

DCDC voltage conversion is done using the LT8612. The voltages for the DCDC converters are:

1V – FPGA Core Power

1.2V – VMM Digital Power, FPGA IO Power

1.5V – VMM Analog Power (for 1.2V LDO's)

2.5V – Miscellaneous FPGA Power (for 1.8V, 1.2V and 1.0V LDO's)

Low dropout linear regulators are used to provide the specific voltages needed by the VMM and FPGA. There are 12 of them and they are ADP1755 devices.

8 for VMM analog power, providing isolation.

4 for miscellaneous FPGA power including ADC and MGT.

Power estimates:

Here are some calculations related to the power estimates for the LT81612.

LT8612 #1 $1.5V_{anlg}$

I_{anlg15} = 8*0.427A i_{anlg12} (via ADP1755ACPZ-1-8)

= 3.4A + losses

Note: 0.427A may be low! (but 8612 should have sufficient reserve)

LT8612 #2 $1.2V_{dgtl}$

I_{dgtl12} = 8*.150A i_{dig12} + 0.621A i_{cco12} = 1.821A + losses

LT8612 #3 $1.0V_{fpga}$

I_{fpga10} = 3.15A i_{ccint}

+ 0.100A i_{ccbram} = 3.65A + losses

LT8612 #4 $2.5V_{fpga}$

I_{fpga25} = 0.621A i_{cco25}

+ 0.511A $i_{mgtavcc10}$ (viaADP1755ACPZ-9)

+ .36A $i_{mgtavtt}$ (viaADP1755ACPZ-10)

+ 0.32A i_{ccaux}

=1.8A + losses

Notes:

I_{ccauxq} (Vaux Quiescent) = 7mA

1.8V LVCMOS25 or 33 = 2-24mA per pin

1.2V SSTL / HSTL 8mA per pin max

Here are worst case VMM power estimates that were used initially, but need to be measured.

V_{ddp}: 150mA

V_{dd}: 400mA

V_{ddad}: 200mA

V_{ddd}: 100mA (all channels active at maximum speed)

Filter circuits are used on the output of the LDOs. Filtering estimates were performed using http://sim.okawa-denshi.jp/en/RLCtool.php. Here are parameters relevant to those estimates.

LT8612 Ripple Frequency: 1.32MHz

LT8612 Ripple Amplitude: 20mV p-p

ADP1755ACPZ-R7 Ripple Frequency:1.32MHz

ADP1755ACPZ-R7 PSRR: -50db

Target noise is 20uVRMS = -60db

Using an RLC LPF calculator:

R=1.5, L=.22uH, C=100uF, Fc=1MHz

Attenuation > 30db

R=.01, L=1uH, C=100uF, Fc=1MHz

Attenuation > 30db

R=.01, L=1uH, C=100uF, Fc=1MHz

Attenuation > 45db

Grounding

We have tried to comply with the requirements of the grounding plan that is given here:

https://edms.cern.ch/edmsui/#!master/navigator/document?D:1032271270:1032271270:subDocs

The relevant VMM supplies and associated bypass caps are:

Vddp, Vss (AGND)
This is the most sensitive supply. It is connected to the source of the input transistors. It has to be kept far from any digital signals, digital supply, and digital ground.
Note: the plane surrounding (shielding) the input lines i0-i63 should be Vddp. The impedance should be kept as small as possible.
Bypass caps used are: 5x4.7uF, 5x1.0uF, 5x0.1uF, 5x0.01uF

Vdd, Vss
These are the analog supply and ground, and are the next most sensitive after Vddp. They should be kept away from the digital signals, digital supply and digital ground. The analog outputs PDO, TDO, MO should be shielded by these planes.
Bypass Caps: 5x4.7uF, 5x1.0uF, 5x0.1uF, 5x0.01uF

Vddad, Vssad
These are the mixed-signal (analog ADC) supply and ground. They should be treated as sensitive as well. They should be kept away from the digital signals, digital supply and digital ground. The impedance should be kept as small as possible, as for Vddp.
Bypass Caps: 3x4.7uF, 3x1.0uF, 3x0.1uF, 3x0.01uF

Vddd, Vssd (GND)
These are the digital supply and ground. All digital I/O should be shielded by these planes.
Bypass Caps: 4x4.7uF, 4x1.0uF, 4x0.1uF, 4x0.01uF

The MMFE load presented to the power distribution supply and return might vary significantly from full load (1-2A at 24V) to off. This will be aggravated at lower supply voltages (10V) where the 1-2A will become 2-4A. If ballast resistors of 200mOhm are used, this could be an active variance of up to 800mV or higher, in addition to the line and connector contributions in the power distribution.

The MMFE (Analog) AGND is tied to the MMFE (Digital) GND via EMI inductors. The MMFE (Digital) GND is tied directly to the LV return. AGND is tied directly to the Detector GND (the pad below the Zebra connector). Thus the MMFE (Digital) GND is tied to the

Detector GND via EMI inductors. The HV return appears to be tied directly to Detector GND. Thus the LV and HV returns are tied directly to each other through AGND via EMI inductors. Further, the LV and HV returns appear to have separate routing to the Experiment ground (called Chamber ground in the grounding document).

A worry is that this system ties the LV and HV grounds together at the most sensitive point, the MMFE AGND. Further it is unknown what the routing for the LV and HV returns is or how they are tied to the Experiment (chamber) GND.

Inputs

MM input

The MM inputs are via Zebra connectors. **These are found on sheets 15-22 of the schematic**.

Overvoltage protection is provided by the NUP4114 TVS device. A 10 ohm series resister is used as a current limiter.

Trace impedance on the MM detector appears to be ~13 ohms, which is not realizable on MMFE PCB due to trace width and dielectric height and value constraints. Since we cannot match impedance, the PCB inputs are designed for minimum capacitance by removing all but inner planes underneath the input traces. The input traces are referenced to Vddp, which sandwiches the innermost AGND. Calculations related to the MM detector capacitance are included.

MM Detector Impedance Values				
Kapton Thickness	0.06	mm	2.36	mil
Er Kapton	3.4			
Honeycomb Thickness	9	mm	354.33	mil
Er Argon - CO2	1			
Trace Width	0.3	mm	11.81	mil
Trace Pitch	0.45	mm	17.72	mil

MM Impedance Calc

Single Ended Microstrip			**Differential Microstrip**	
Target Impedance	Detector	FEB	Detector	FEB
Model Impedance	13.12	48.57	26.22	107.80
Trace width	11.81	7.00	11.81	4.00
Dielectric Er	3.4	4.3	3.4	4.3
Dielectric height	2.36	4.00	2.36	4.00
Trace thickness	0.7	0.7	0.7	0.7
Differential Spacing			17.72	4.00

Not Valid at large height

Single Ended Asymetric Stripline			**Differential Asymetric Stripline**	
Target Impedance	Detector	FEB	Detector	FEB

Model Impedance	0.67	48.75	0.72	68.54
Trace width	11.81	4.00	11.81	4.00
Dielectric Er	3.4	4.3	3.4	4.3
Dielectric height (near)	2.36	4.00	2.36	4.00
Dielectric height (far)	354.33	8.00	354.33	8.00
Trace thickness	0.7	0.7	0.7	0.7
Differential Spacing			17.72	4.00

Trace capacitance calculation	FEB
Total Number of Layers	14
Intervening Number of Layers	5
Board thickness	100
Trace Thickness	0.7
Dialectric Height	35.71429
Trace Width	7.00
Trace Length (mil)	40.00
Dielectric Er	4.3
C0 (pF/in)	1.085791
C (pF)	0.043432

The formulas used here are taken from the *Design Guide for Electronic Packaging Utilizing High-Speed Techniques* (4th Working Draft, IPC-2251, February 2001

THESE FORMULAS ARE APPROXIMATIONS! They should not be used when a high degree of accuracy is required.

L1DDC I/O

The I/O from/to the L1DDC are via a 36 pin MiniSAS connector. **This is shown on Sheet 3 of the schematic.** The signals are all “VMM LVDS”, called custom LVDS in the VMM specification document. The data and clocks correspond to three e-links.

E-link 1 is actually two data e-links but with only one RX pair and one clock pair from the LDDC. TTC data are carried by the RX pair. L1Data (data sent in response to an L1 Accept) is carried by two TX pairs. Note there is no explicit clock accompanying the TX data. A 40 MHz clock can be derived from the e-link clock sent from the L1DDC to the FPGA. For the Production MMFE board, the ROC replaces the FPGA. The data format is presumably given in the L1DDC specifications.

E-link 2 is used for configuration and status data. The RX pair is used to send VMM configuration data from the L1DDC to the FPGA. The TX pair is used to send status data (if any) from the FPGA to L1DDC. Note there is no explicit clock accompanying the TX data. For the Production MMFE board, the SCA replaces the FPGA. The data format is defined in the SCA specifications but we have not documented this.

Optionally, all inputs (including spares) can be AC coupled, but default uses a 0 Ohm resistor.

ADDC I/O

The I/O from/to the ADDC are via a 36 pin MiniSAS connector. **This is shown on Sheet 3 of the schematic.** The signals are all “VMM LVDS”, called custom LVDS in the VMM specification document.

Outputs to the ADDC are eight ART data lines, one from each VMM.

There is also one pair of clock lines from FPGA/ROC to the ADDC and one pair of clock lines to the FPGA/ROC from the ADDC. It is TBD whether the individual clock lines from FPGA/ROC to each VMM (ckart) are derived from a master on the ROC or ADDC.

Optionally, clock inputs (including spare) can be AC coupled, but the default is a 0 Ohm resistor.

Optionally, the clock inputs can be input protected but currently they are DNP.

Presently, the spare ART IO can be tied to the spare L1DDC IO and to the FPGA.

MiniSAS cables

MiniSAS cables are used to connect the MMFE and L1DDC and ADDC. The cable has been shown to provide good signal transmission over several meters beyond 200 MHz. Some early measurements are included in the supporting material (folder). The MiniSAS cable is in operation with the Altera Cyclone IV and Xilinx Spartan 6 FPGA.

The shield ground is capacitively coupled to the VMM digital ground (GND).

Ethernet output (Demonstrator)

The Ethernet interface is given on Sheet 9 of the schematic. The MDIO data and clock control the configuration of the Marvel Phy 88-1111. A reset and interrupt also exist. The interface to the FPGA is TX/RX through SGMII pairs. A set of configuration resistors exist that will hopefully preclude the need to set register through the MDIO.

Clocks

ckart_out: This clock qualifies the ART data from the eight VMM’s. Its source is the FPGA on the Demonstrator and the ROC on the Production board. Because the ART data is sent in response to the ART clock, the qualifying clock may be identical to ckart_N or slightly delayed with respect to these clocks.

ckart_in: This clock comes from the ADDC to the FPGA/ROC and may be used to generate ckart_N. Or it could be ignored. The clock frequency is 160 MHz DDR.

ckart_N (where N is 1-8): This clock is sent from the FGPA/ROC to the VMM to transfer ART data from the VMM.

elink_clk_1: This clock comes from the L1DDC card to the FPGA/ROC and qualifies the e-link data from the L1DDC. The clock frequency is TBD. This clock can also be used to derive the ATLAS system clock. It may have to be phase adjusted at the L1DDC or on the FGPA/ROC.

elink_clk1_2: Same as elink_clk_1.

TCK: FGPA JTAG configuration clock (programmable, with a frequency of a few-20 MHz)

FPGA_CCLK: FGPA configuration clock from FGPA to configuration flash. The frequency is < 50 MHz.

EM_CCLK (50 MHz): This clock is used to generate FPGA_CCLK. It is generated by an oscillator.

2V5_diff_clk: This is an oscillator clock at 200.395 (5 x LHC clock).   This is a utility clock that could be used as an FPGA system clock.

ckbc_N: BC clock from the FPGA/ROC to the VMM's. The frequency is 40.079 MHz.

cktk_N: Token clock for VMM configuration and readout from the FPGA/ROC to each VMM. The frequency is variable.

ckdt_N: Data readout clock from FPGA/ROC to each VMM. The frequency could be 160 or 200 or 320 MHz. Tests are still needed to determine the maximum frequency.

cktp_N: Pulser clock from FPGA/ROC to each VMM. The frequency is variable.

XTAL1, XTAL2: 25 MHz clock from a crystal oscillator used for the Ethernet PHY.

MDC_SCL: 2.5 MHz programmable I2C clock from the FPGA to the Ethernet PHY for clocking MDIO data.

MGTREFCLK0: 125 MHz clock from a jitter cleaner driven by 25 MHz clock. It is used for the SGMII interface to the PHY.

MGTREFCLK1: 200 MHz clock oscillator for general purpose use.

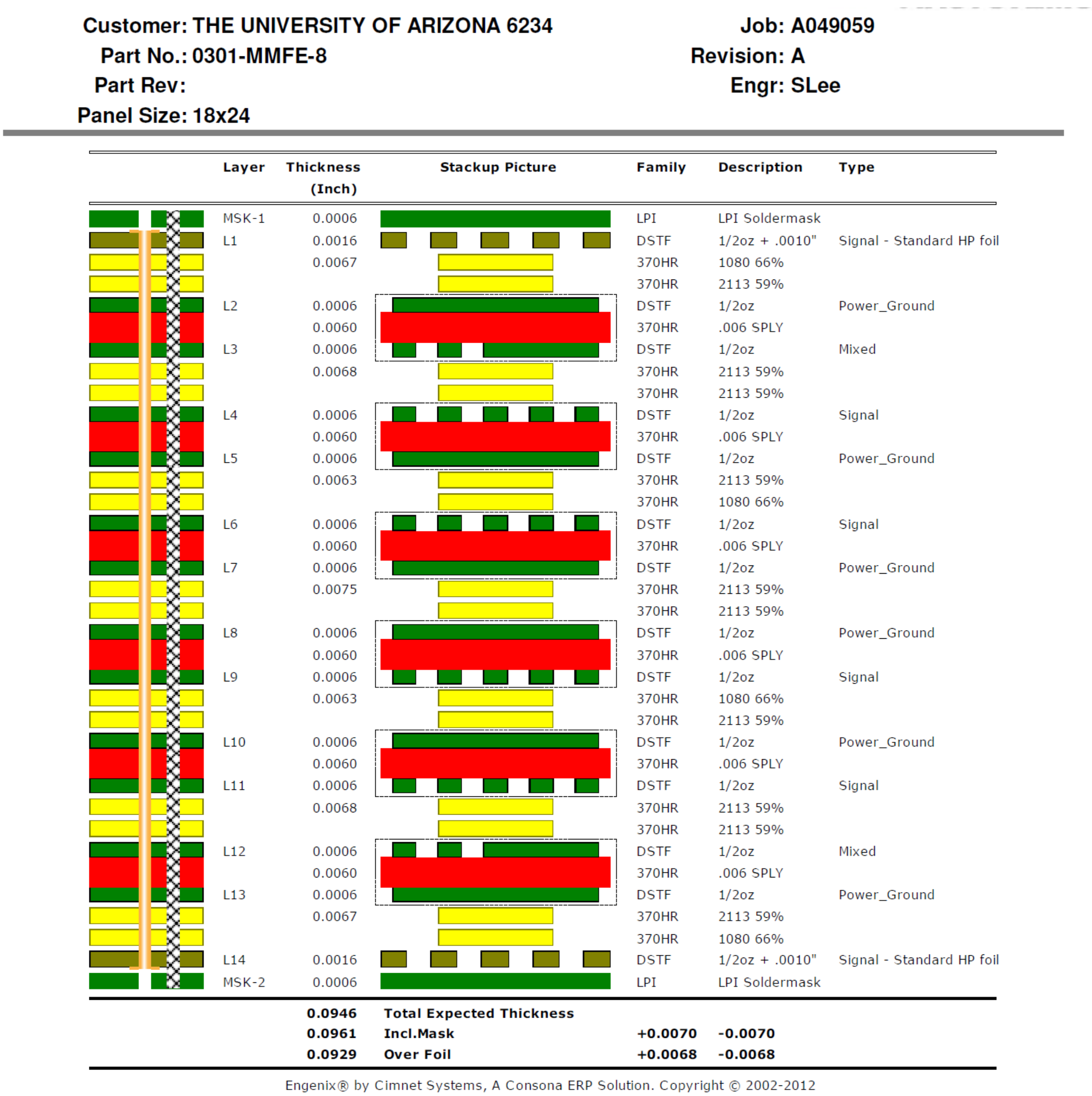
Token:

tki – comes from the FPGA to first VMM and then tko from this first VMM goes to tki of second VMM. The tko from the eighth VMM returns to the FPGA.

Design and layout

Stackup

The MMFE Demonstrator stackup from ViasSystems is given in Figure 6 below. It includes trace widths and structure information to facilitate a controlled impedance design. The board is ~100 mil thick, and is comprised of 14 electrical layers separated by FR4. Differential 80, 90, and 100 ohm traces are to be routed on the internal layers as 3 layer pairs, and 40, and 50 ohm single ended pairs are routed on the outer layers. Eight planes are intentionally voided in the analog section to reduce capacitance. , The outer layers are used for routing analog signals, then 4 voided layers on each side, followed by one Vddp layer on each side sandwiching a pair of analog ground planes. All this is done to reduce the capacitance of the 512 analog signals feeding the board. The outer analog reference layers should be tied to 1V2_VddX, and the inner layers to AGND. The planes for the remainder of the board may be utilized as appropriate. Note: Analog planes should not overlap Digital planes.



Customer: THE UNIVERSITY OF ARIZONA 6234 **Job:** A049059
Part No.: 0301-MMFE-8 **Revision:** A
Part Rev: **Engr:** SLee
Panel Size: 18x24

Layer	Thickness (Inch)	Stackup Picture	Family	Description	Type
MSK-1	0.0006		LPI	LPI Soldermask	
L1	0.0016		DSTF	1/2oz + .0010"	Signal - Standard HP foil
	0.0067		370HR	1080 66%	
			370HR	2113 59%	
L2	0.0006		DSTF	1/2oz	Power_Ground
	0.0060		370HR	.006 SPLY	
L3	0.0006		DSTF	1/2oz	Mixed
	0.0068		370HR	2113 59%	
			370HR	2113 59%	
L4	0.0006		DSTF	1/2oz	Signal
	0.0060		370HR	.006 SPLY	
L5	0.0006		DSTF	1/2oz	Power_Ground
	0.0063		370HR	2113 59%	
			370HR	1080 66%	
L6	0.0006		DSTF	1/2oz	Signal
	0.0060		370HR	.006 SPLY	
L7	0.0006		DSTF	1/2oz	Power_Ground
	0.0075		370HR	2113 59%	
			370HR	2113 59%	
L8	0.0006		DSTF	1/2oz	Power_Ground
	0.0060		370HR	.006 SPLY	
L9	0.0006		DSTF	1/2oz	Signal
	0.0063		370HR	1080 66%	
			370HR	2113 59%	
L10	0.0006		DSTF	1/2oz	Power_Ground
	0.0060		370HR	.006 SPLY	
L11	0.0006		DSTF	1/2oz	Signal
	0.0068		370HR	2113 59%	
			370HR	2113 59%	
L12	0.0006		DSTF	1/2oz	Mixed
	0.0060		370HR	.006 SPLY	
L13	0.0006		DSTF	1/2oz	Power_Ground
	0.0067		370HR	2113 59%	
			370HR	1080 66%	
L14	0.0016		DSTF	1/2oz + .0010"	Signal - Standard HP foil
MSK-2	0.0006		LPI	LPI Soldermask	
	0.0946	**Total Expected Thickness**			
	0.0961	**Incl.Mask**	**+0.0070**	**-0.0070**	
	0.0929	**Over Foil**	**+0.0068**	**-0.0068**	

VMM length matching priority

1. All clocks to each VMM
    a. ckbc_1 == ckbc_2 ==…==ckbc_8
    b. cktp_1 == cktp_2 ==…==cktp_8
    c. ckdt_1 == ckdt_2 ==…==ckdt_8
    d. ckart_1 == ckart_2 ==…==ckart_8
    e. cktk_1 == cktk_2 ==…==cktk_8
2. VMM Data lines to Data Clock
    a. cktk_1 == data0_1 == data1_1 … cktk_8 == data0_8 == data1_8
    b. ckart_out == art_1 == art_2 ==…==art_8
    c. ckdt == di_1 == di_2 == … == di_8
3. VMM Data lines
    a. do_1 == do_2 == … == do_8
    b. tki_1 == tki_2 == … == tki_8 == tko_8
    c. sett_1 == sett_2 == … == sett_8 == setb_8
4. VMM Control lines
    a. wen_1 == wen_2 == … == wen_8
    b. ena_1 == ena_2 == … == ena_8

VMM digital routing

- Differential impedance is 100 Ohms
- Length match to 40 mil within pair
- Length match to 100 mil pair to pair
- Use 4X spacing between pairs
- Place parallel term resistor near receiver

Note: The LVDS I/O pads developed for VMM are not current driven, but they are voltage driven and the output voltage doesn't depend on the load resistance. If you terminate with 100 ohms you will get 600mV +/-150mV. The receiver is designed to receive 600 +/-150mV and it is capable to receive 200 +/-200mV but it doesn't work with 1200 +/-200mV signals. The LVDS pads also work without termination resistors. The VMM LVDS can drive 15mA.

VMM analog input routing

- SE impedance is low capacitance, low inductance
- Trace width is 7 mil, outer layers only
- No other signals may be routed in this space
- Remove power planes under these traces down to the innermost four layers
- Signals to be referenced to the outer two of four analog planes tied to 1V2_VddX
- Inner two layers of four tied to AGND

VMM analog output routing

- SE Impedance is 50 Ohms
- Referenced to XADC_AGND

FPGA length matching priority and routing

MGT:

- Differential impedance is 85 Ohms
- Length match to 10 mil within pair
- Length match to 50 mil pair to pair within lane (TX to RX)
- Use 4X spacing between pairs
- No more than two layer to layer transitions (via's) are allowed
- Transitions must utilize GSSG via structure
- No foreign traces or planes may enter the GSSG structure
- Reference clock length shall not exceed 4 inches total
- Length match reference clock to 10 mil within pair
- Route MGT signals in accordance with Xilinx 7 Series FPGAs GTP Transceivers User Guide UG482, and Xilinx 7 Series FPGAs PCB Design and Pin Planning Guide UG483

Ethernet:

MD Interface:

- Trace impedance = 40 Ohms
- Length match to < 385 mil
- Spacing is 10 mil for short runs, 4 mils for parallel runs < 500 mils
- Place series term resistor close to transmitter

Twisted Pair Interface:

- Differential Impedance is 100 Ohms
- Route pairs apart by 3X trace height from plane
- Match lengths as close as possible
- Do not use serpentines to make traces match
- Symmetry is important

SGMII:

- AC coupling caps
- Remove (cut-out) reference plane directly underneath capacitor body and pads
- Do not route traces under this cutout between the reference plane cutout and the next plane
- Value is per VC707 rather than 0.1 from UG482

General rules

- Place pads on all unused pins
- Pin swap is allowed within identical FPGA banks
- Pin swap is not allowed between ASICs
- Pin swap is allowed between FPGA Banks 16,13, 15, 34, 35
- Preference is to keep clocks on global clock pins

Power Routing

A functional design has been created for the LT8612. Please follow the design recommendations in the datasheet.

When laying out power, it is recommended to route point to point with trace width sufficient to carry the required current. Pours or splits can then be instantiated, without fear of islands or choke points. This is especially critical for FPGA power distribution.

Power Planes

It is encouraged to place power planes next to ground planes to increase capacitive coupling. For this layout it is probably required to route on power planes and add power and ground planes to signal layers.

FPGA Power Planes:

Bypass Cap Requirements from UG483-Table_2-1:

Vccint	1x680uF,	12x4.7uF,	14x0.47uF
Vccbram	1x100uF,		3x0.47uF
Vccaux	1x47uF,	4x4.7uF,	7x0.47uF
Vcco_0		1x4.7uF	
Vcco_12	1x47uF,	2x4.7uF,	4x0.47uF
Vcco_13	1x47uF,	2x4.7uF,	4x0.47uF
Vcco_14	1x47uF,	2x4.7uF,	4x0.47uF
Vcco_15	1x47uF,	2x4.7uF,	4x0.47uF
Vcco_16	1x47uF,	2x4.7uF,	4x0.47uF
Vcco_33	1x47uF,	2x4.7uF,	4x0.47uF

Vcco_34	1x47uF,	2x4.7uF,	4x0.47uF
Vcco_35	1x47uF,	2x4.7uF,	4x0.47uF

Bypass Cap Requirements from UG482-Table_5-6_5-8:

MGTavcc	1x4.7uF,	2x0.1uF
MGTavtt	1x4.7uF,	2x0.1uF

Two 0.22 0201 Ceramic Caps are substituted for each Xilinx recommended 0.47 0402 Ceramic Caps, per Avnet practice.

MMFE-8 Production Board

As mentioned in the introduction, the differences between the MMFE-8 Production and Demonstrator boards are: The SCA and ROC ASIC replace the FPGA, the power scheme will be changed to one that is radiation tolerant and there is no Ethernet output.

Connection between VMM and SCA

The SCA (Slow Control ASIC) is used in the Production version of the MMFE-8. The SCA is primarily used to configure, calibrate and monitor the VMM ASIC's. Our SCA contact at CERN is Kostas Kloukinas.

It is unclear how future versions of the VMM will be configured. At one time it was proposed to switch to I2C for VMM configuration but SPI could be used as well. In the case of SPI, one would need to add an SS input to the VMM for slave selection.

Packaging and pinout of the SCA exist as does a preliminary specification manual. However the electrical specification section of that manual is blank. It is our understanding the present SCA operates at 1.5V. It is our understanding that the SCA uses DVDD and DVSS (periphery power and ground), VDD and GND (digital power and ground) and AVDD and AGND (analog power and ground). Thus we need to supply these voltages (which is not desirable). We assume for the moment that these voltages must be supplied separately and that they are at 1.5V.

There are two problems associated with configuring the VMM via the SCA. One is that the SPI or I2C signals on the SCA are single-ended while the VMM requires differential signals. The second is that the SCA is a 1.5V device while the VMM is a 1.2V device. The ideal solution would have the SCA operate (at least I2C section) at 1.2V and have the VMM accept single-ended inputs for configuration. However the details here are not settled and need additional discussions with the SCA and VMM teams. Some sort of test rig connecting the SCA to VMM to verify a new configuration scheme is a critical need.

A preliminary list of signals between the VMM and SCA are given in an accompanying spreadsheet below.   These signals include eight lines of MM ID which connect the SCA to the MM detector via the Zebra connector.

Connection between VMM and ROC

A preliminary high level diagram exists for the ROC and is given in the supplemental material (folder). The ROC is a 1.2V device like the VMM.   A preliminary list of signals between the VMM and ROC are given in an accompanying spreadsheet below. A side note is that if VMM configuration occurs via the SCA and VMM and readout occurs via the ROC, then an additional signal will have to be implemented on the VMM.   This is because cktk is currently used for both configuration and readout.

SCA	VMM	ROC	L1DDC	ADDC	comment
sda_pad(8x1)	di(8x1) -new				change from diff to se
sda_pad(8x1)??	do(8x1) - new				change from diff to se
scl_pad(8x1)	ckcfg(8x1) - new				change from diff to se
	data0(8x2)	data0(8x2)			
	data1(8x2)	data1(8x2)			
	ckdt(8x2)	ckdt(8x2)			
	cktk(8x2)	cktk(8x2)			
	cktp(8x2)	cktp(8x2)			
	art(8x2)			art(8x2)	
	ckart(8x2)	ckart(8x2)			
adc_in _pad(8x1)	pdo(8x1)				
adc_in_pad(8x1)	tdo(8x1)				
	mo(8x1)				sent through pdo
adc_in_pad(8x1)					various voltages
	wen(8x2)	wen(8x2)			
	ena(8x2)	ena(8x2)			
		ckartout (1x2)		ckartout (1x2)	to qualify art data
		elink0 - tx(2x2)	elink0 - tx(2x2)		l1data
		elink0 - rx(2x2)	elink0 - rx(2x2)		ttc
		elink0 - clk(2x2)	elink0 - clk(2x2)		40? MHz clock
		elink1 - tx(2x2)	elink1 - tx(2x2)		l1data
tx_sd(2x2)			elink2 - tx(2x2)		status up
rx_sd(2x2)			elink2 - rx(2x2)		config down
link_clk(2x2)			elink2 - clk(2x2)		clock
scl_pad(1x1)		scl_pad(1x1)			roc config and mm id
sda_pad(1x1)		sda_pad(1x1)			roc config and mm id
	ckbc(8x2)	ckbc(8x2)			
	bcr(8x2)	bcr(8x2)			
	l1 acc (8x2)?	l1 acc (8x2)?			
	test pulse (8x2)?	test pulse (8x2)?			same as cktp?
gpio_pad(8x1)					mm id via zebra

Other Issues

The MMFE-8 must operate in an environment of modestly high radiation and magnetic field. At the inner rim of the New Small Wheel, the values of TID (Total Ionizing Dose), NIEL(Non-Ionizing Energy Loss) and B field are estimated to be 340 kRad, 8 x 10^{14}/cm^2, and 1 kG. At the outer rim of the New Small Wheel, the values of TID, NIEL and B field are estimated to be 9 kRad, $8x10^{14}/cm^2$ and 6 kG. The program to qualify components to operate in these conditions is not discussed here.

Outstanding technical concerns and risk assessment

VMM noise

Integration and cooling with production MM chambers

Lack of beam tests and other tests of the MMFE-8 with production MM chambers

Robustness of Zebra connectors

Convergence on SCA and ROC specifications, pinouts and package

Schedule

A snapshot of the schedule is given below.

	duration	start	stop	comments
vmm2, fpga				
mmfe demo v1 design				
mmfe demo v1 layout				
mmfe demo v1 initial fabrication				
mmfe demo v1 initial assembly	30	1/15/2015	2/14/2015	
mmfe demo v1 initial testing	21	2/14/2015	3/7/2015	
mmfe demo v1 small design changes	14	3/7/2015	3/21/2015	
mmfe demo v1 final fabrication	14	3/21/2015	4/4/2015	
mmfe demo v1 final assembly	14	4/4/2015	4/18/2015	
mmfe demo v1 final testing	21	4/18/2015	5/9/2015	
vmm3, fpga				
mmfe demo v2 design	15	7/1/2015	7/16/2015	us atlas schedule has design start 3/12/15
mmfe demo v2 layout	21	7/16/2015	8/6/2015	
mmfe demo v2 initial fabrication	14	8/6/2015	8/20/2015	
mmfe demo v2 initial assembly	14	8/20/2015	9/3/2015	
mmfe demo v2 initial testing	21	9/3/2015	9/24/2015	
mmfe demo v2 small design changes	14	9/24/2015	10/8/2015	
mmfe demo v2 final fabrication	14	10/8/2015	10/22/2015	
mmfe demo v2 final assembly	14	10/22/2015	11/5/2015	
mmfe demo v2 final testing	21	11/5/2015	11/26/2015	us atlas schedule has test start 6/30/15
vmm3, sca1, roc1				
mmfe prod v1 design	60	7/1/2015	8/30/2015	us atlas schedule has design start 6/30/15
mmfe prod v1 layout	45	8/30/2015	10/14/2015	
mmfe prod v1 initial fabrication	14	10/14/2015	10/28/2015	
mmfe prod v1 initial assembly	14	10/28/2015	11/11/2015	
mmfe prod v1 initial testing	40	11/11/2015	12/21/2015	
mmfe prod v1 small design changes	14	12/21/2015	1/4/2016	
mmfe prod v1 final fabrication	14	1/4/2016	1/18/2016	
mmfe prod v1 final assembly	21	1/18/2016	2/8/2016	
mmfe prod v1 final testing	40	2/8/2016	3/19/2016	us atlas schedule has test start 4/18/16
vmm4, sca2, roc2				
mmfe prod v2 design	55	6/17/2016	8/11/2016	approximate us atlas schedule
mmfe prod v2 layout	42	8/11/2016	9/22/2016	
mmfe prod v2 initial fabrication	14	9/22/2016	10/6/2016	
mmfe prod v2 initial assembly	14	10/6/2016	10/20/2016	
mmfe prod v2 initial testing	40	10/20/2016	11/29/2016	
mmfe prod v2 buffer	14	11/29/2016	12/13/2016	
mmfe prod v2 final fabrication	14	12/13/2016	12/27/2016	
mmfe prod v2 final assembly	40	12/27/2016	2/5/2017	
mmfe prod v2 final testing	105	2/5/2017	5/21/2017	
vmm4, sca2, roc3				
mmfe prod v2 design	30	4/12/2017	5/12/2017	approximate us atlas schedule
mmfe prod v2 layout	25	5/12/2017	6/6/2017	
mmfe prod v2 prepare for fab and assy	30	6/6/2017	7/6/2017	
mmfe prod v2 final fabrication	35	7/6/2017	8/10/2017	
mmfe prod v2 final assembly	45	8/10/2017	9/24/2017	
mmfe prod v2 qa/qc	30	9/24/2017	10/24/2017	
mmfe prod v2 final testing	105	10/24/2017	2/6/2018	