5/22/15

At this moment, our firmware changes daily. It is not as advanced as the sophisticated firmware used with the SRS system. Our firmwarew was written by Charlie Armijo, Rick Columbo, Andy Dowd, Bill Hart and Ken Johns. At some point we will try to make it professional like the firmware for the SRS system, but that is a lower priority. That is, at the moment, the firmware is not very modular since we are focused more on functionality.

This and other information is posted on the NSW Electronics twiki.

**What exists:**

Ethernet with A7 (Artix-7) – A working project exists with many registers defined that one can R/W using our host PC software. The host software is simple and can be used by other host software. This is available to ATLAS. Note that many institutions and collaborations (SLAC and RD-51) put proprietary constraints on their software, we do not. Less easy is subsequently using those registers in the VHDL but we have figured this out.

Global reset and configuration without Ethernet (Artix-7) – A working project exists that can do a global reset and configure each VMM via a GUI on a host PC software exists. Actually it does a bit more but if institutions are interested in these functions alone, we can easily make it.

Global reset, configuration and acquisition mode (Data0 and Data1 readout) into a FIFO without Ethernet (Artix-7) – A working project exists that performs these functions. There is no Ethernet interface and the FIFO is controlled via VIO. Clock width and frequency are also controlled via VIO. However the FIFO is just for one VMM.

Global reset, configuration, data acquisition into a FIFO integrated into the Ethernet project (Artix-7). This exists and works but the FIFO is not yet connected to the axi_registers for readout.

Untested VHDL code that latches a BCID associated with an external trigger. This is in response to the criticism of Giora Mickenberg.

XADC firmware for the PDO (monitor) out. Standalone code exists and has been tested.

**What does not exist**:

An Ethernet project that reads the FIFO for one VMM into a register that can be read by the host PC software. This is our highest priority. I am working on this now.

An Ethernet project that reads FIFO's for all eight VMM's. It is unclear how useful this mode is and how to implement it.

An Ethernet project that reads FIFO's in response to an external trigger. We have untested firmware (leaky bucket) that can be used for this purpose. This is our second highest priority.

XADC firmware that is integrated into the Ethernet project. This will be done next week by Andy.

Multiple user registers set by our GUI. There are a number of registers that are hardwired in the VHDL. We are migrating these so they can be set by the GUI and the registers used by the HDL. This is ongoing and being done by Charlie.

We only have skeleton host PC software for the FIFO readout once it is connected to the axi_registers. This can be done quickly though so it should be done about the same time as the HDL section.