Xilinx Spartan 6 - FPGA Mezzanine Card	
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THE UNIVERSITY OF ARIZONA®

Physics Department
Spartan 6 - FMC RevA
5/4/2014
9:09:00 PM

PCB1
PCB_Layout
PCB Layout

PCB2
PCB_Manufacture
PCB Manufacture

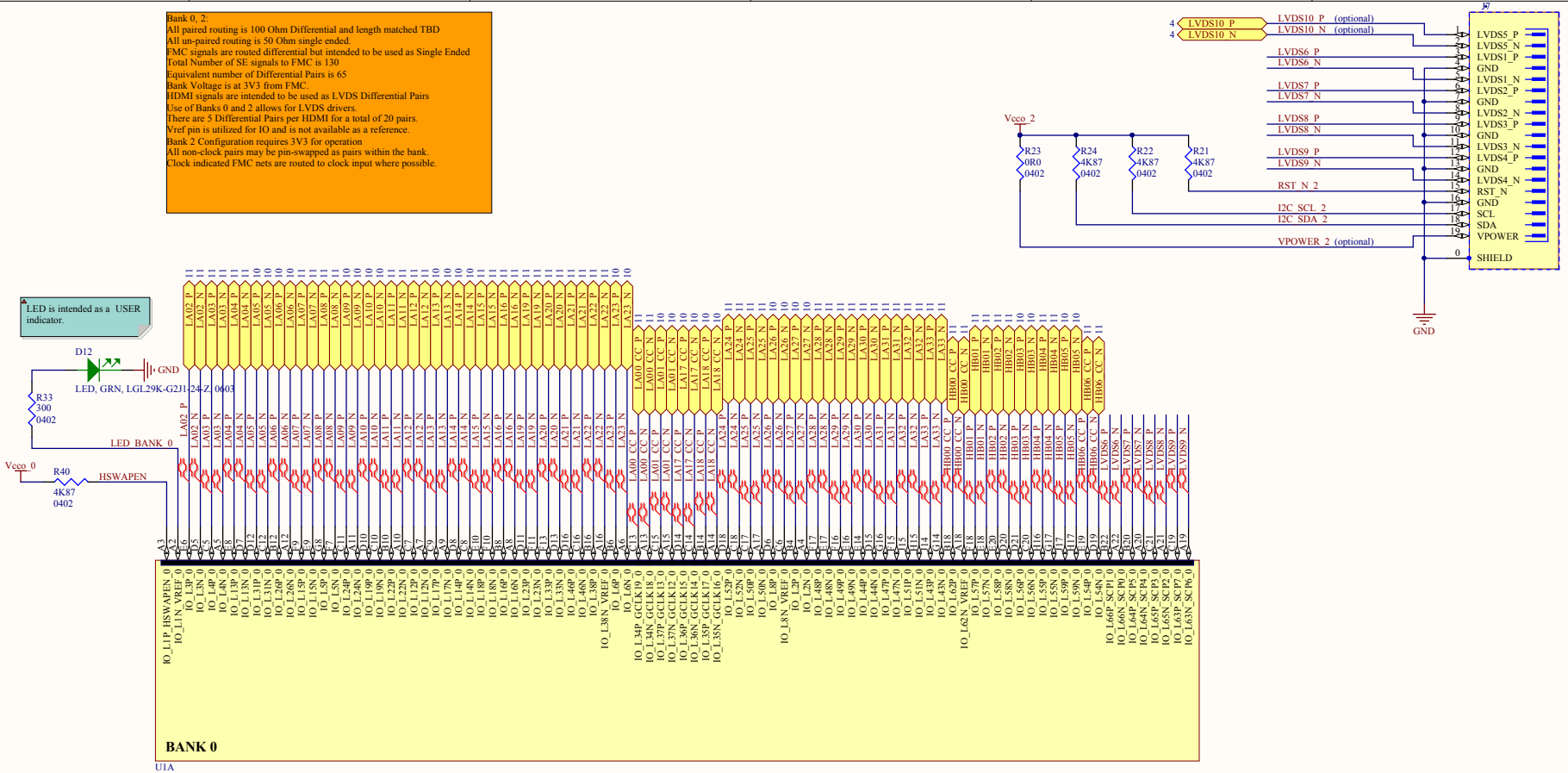
PCB3
PCB_Assemble
PCB Assemble

CBL
PKG
miniSAS 8i 68 ckts

Title: *S6 FMC*			*University of Arizona* 1118 E 4th St Tucson, Arizona 85721 billhart@email.arizona.edu
Size: B	Engineer: William Hart	Revision: A	
Date: 5/4/2014	Time: 9:09:00 PM	Sheet 1 of 11	Drawn By: Karen Palmer
File: C:\Pjcts\AltProj\0300-S6 FMC\0300-S6 FMC\S6-FMC TitleSheet.Sch.Doc			

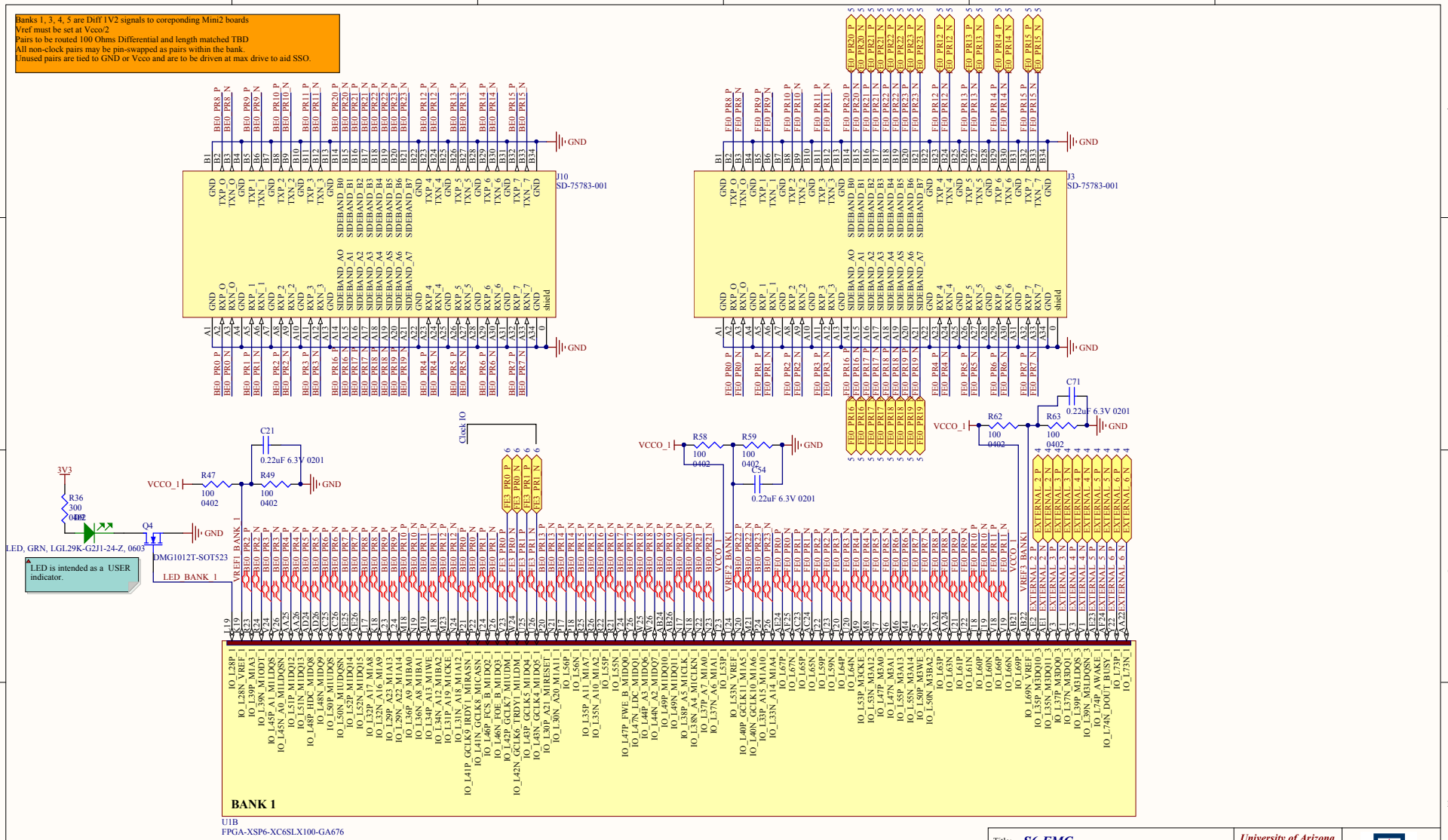
Bank 0, 2:
All paired routing is 100 Ohm Differential and length matched TBD
All un-paired routing is 50 Ohm single ended.
FMC signals are routed differential but intended to be used as Single Ended
Total Number of SE signals to FMC is 130
Equivalent number of Differential Pairs is 65
Bank Voltage is at 3V3 from FMC.
HDMI signals are intended to be used as LVDS Differential Pairs
Use of Banks 0 and 2 allows for LVDS drivers.
There are 5 Differential Pairs per HDMI for a total of 20 pairs.
Vref pin is utilized for IO and is not available as a reference.
Bank 2 Configuration requires 3V3 for operation
All non-clock pairs may be pin-swapped as pairs within the bank.
Clock indicated FMC nets are routed to clock input where possible.

LED is intended as a USER indicator.



Title: **S6 FMC**			*University of Arizona*
Size: B	Engineer: William Hart	Revision: A	*1118 E 4th St*
Date: 5/4/2014	Time: 9:09:00 PM	Sheet 2 of 11	*Tucson, Arizona 85721*
File: C:\Pjcts\AltProj\0300-S6 FMC\0300-S6 FMC\S6 Bank0.SchDoc		Drawn by: Karen Palmer	*billhart@email.arizona.edu*

Banks 1, 3, 4, 5 are Diff 1V2 signals to coreponding Mini2 boards
Vref must be set at Vcco/2
Pairs to be routed 100 Ohms Differential and length matched TBD
All non-clock pairs may be pin-swapped as pairs within the bank.
Unused pairs are tied to GND or Vcco and are to be driven at max drive to aid SSO.



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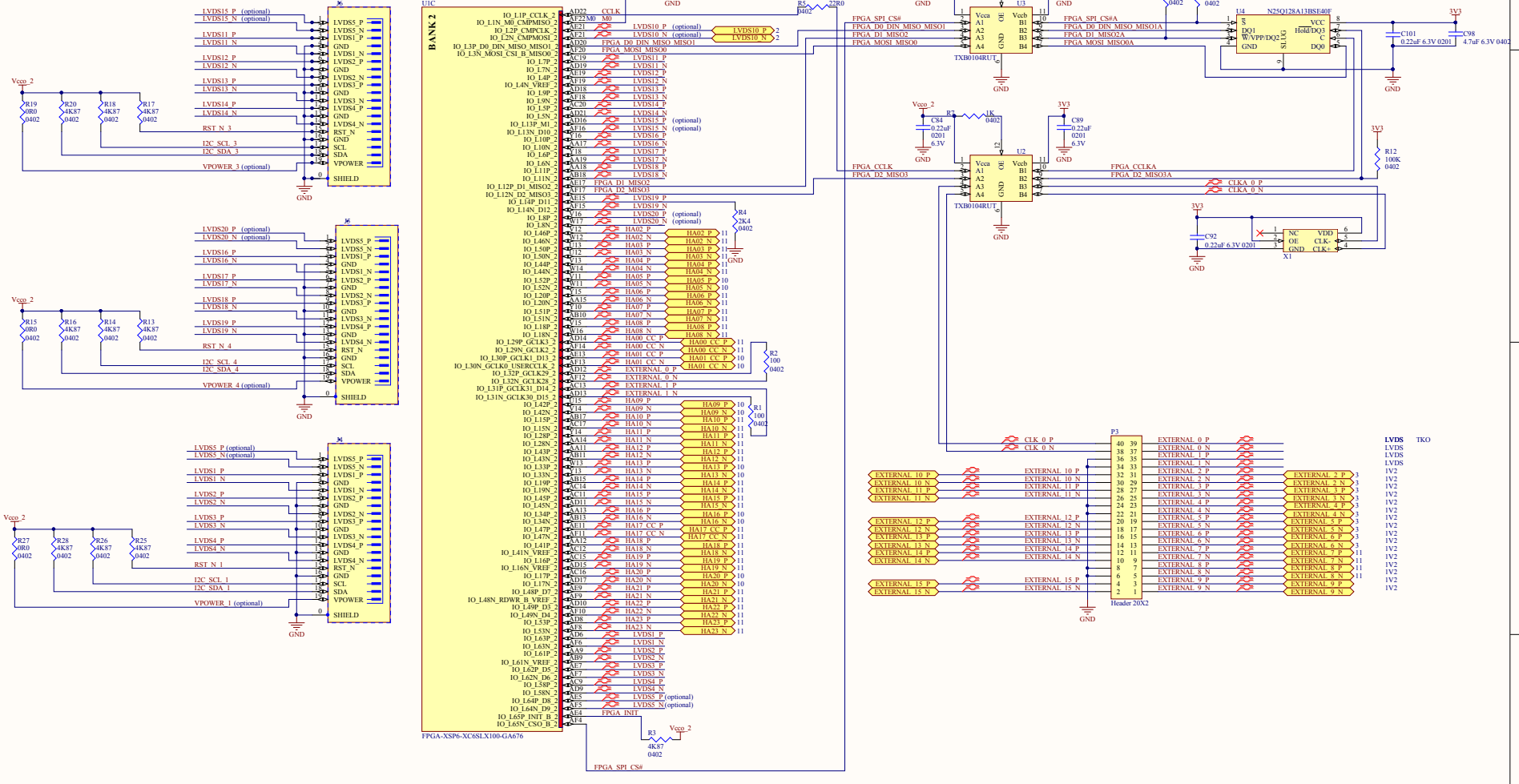
Size: B	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 5/4/2014 Time: 9:09:00 PM		Sheet 3 of 11	
File: C:\Pjcts\AltProj\0300-S6 FMC\0300-S6 FMC\S6 Bank1.SchDoc			Drawn by: Karen Palmer

Bank 0, 2:
All paired routing is 100 Ohm Differential and length matched TBD
All un-paired routing is 50 Ohm single ended.
FMC signals are routed differential but intended to be used as Single Ended
Total Number of SE signals to FMC is 130
Equivalent number of Differential Pairs is 65
Bank Voltage is at Vadj (0 to 3V3) from FMC.
HDMI signals are intended to be used as LVDS Differential Pairs
Use of Banks 0 and 2 allows for LVDS drivers.
There are 5 Differential Pairs per HDMI for a total of 20 pairs.
Vref pin is utilized for IO and is not available as a reference.
Bank 2 Configuration requires 3V3 for operation
All non-clock pairs may be pin-swapped as pairs within the bank.
Clock indicated FMC nets are routed to clock input where possible.

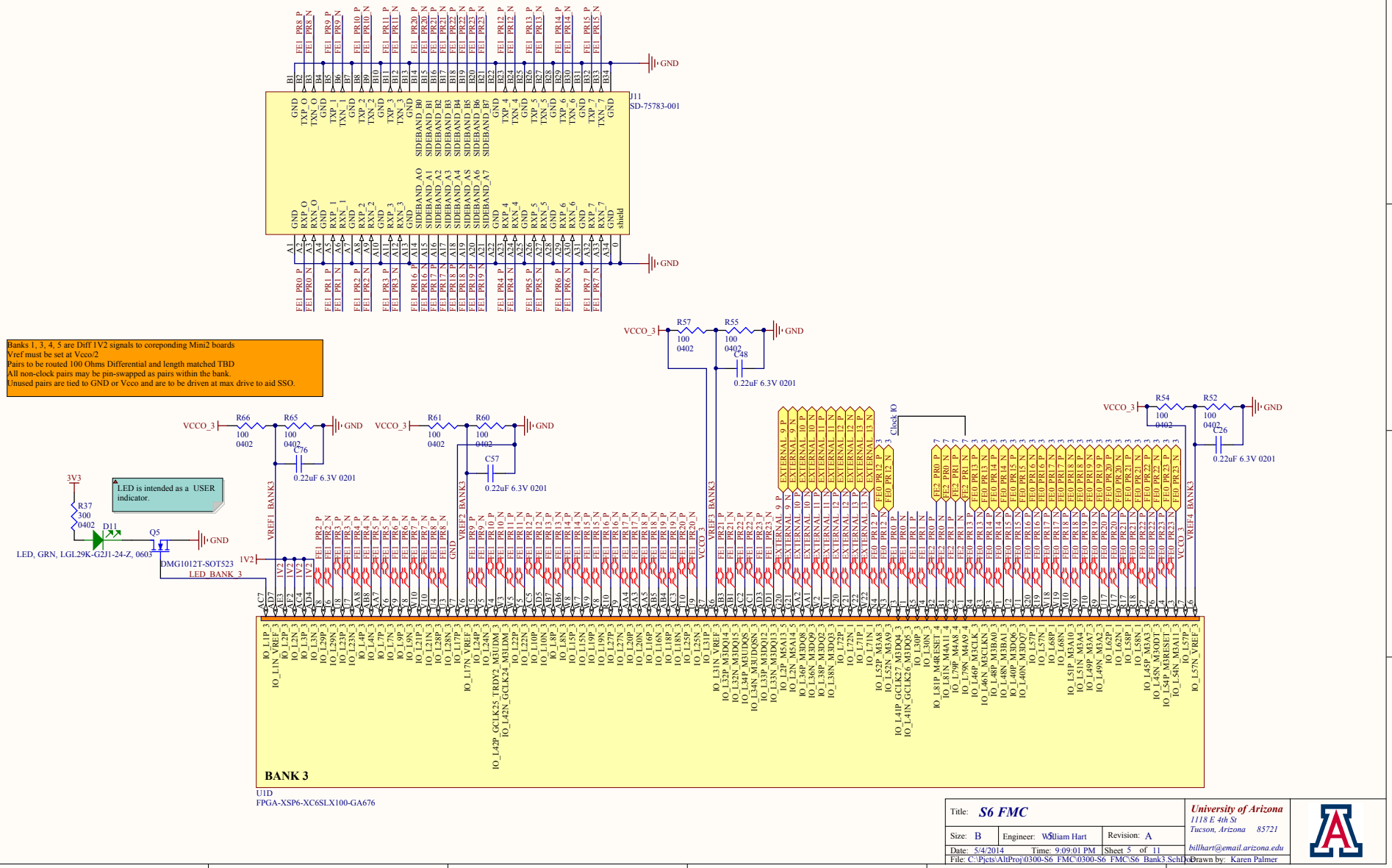
LED is intended as a USER indicator.

Place serial termination resistor close to the FPGA

SPI Flash ROM Signal / Pin Equivalences
C = Clock = Input
DQ0 = Serial Data In = Input
DQ1 = Serial Data Out = Output
S_N = CS = Input



Title: S6 FMC			University of Arizona, 1118 E 4th St, Tucson, Arizona 85721
Size: C	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 5/4/2014	Time: 9:09:01 PM	Sheet 4 of 11	
File: C:\Projects\AltProj\0300-S6 FMC\0300-S6 FMC\S6 Bank2.SchDoc		Drawn by: Karen Palmer	



Title: **S6 FMC**

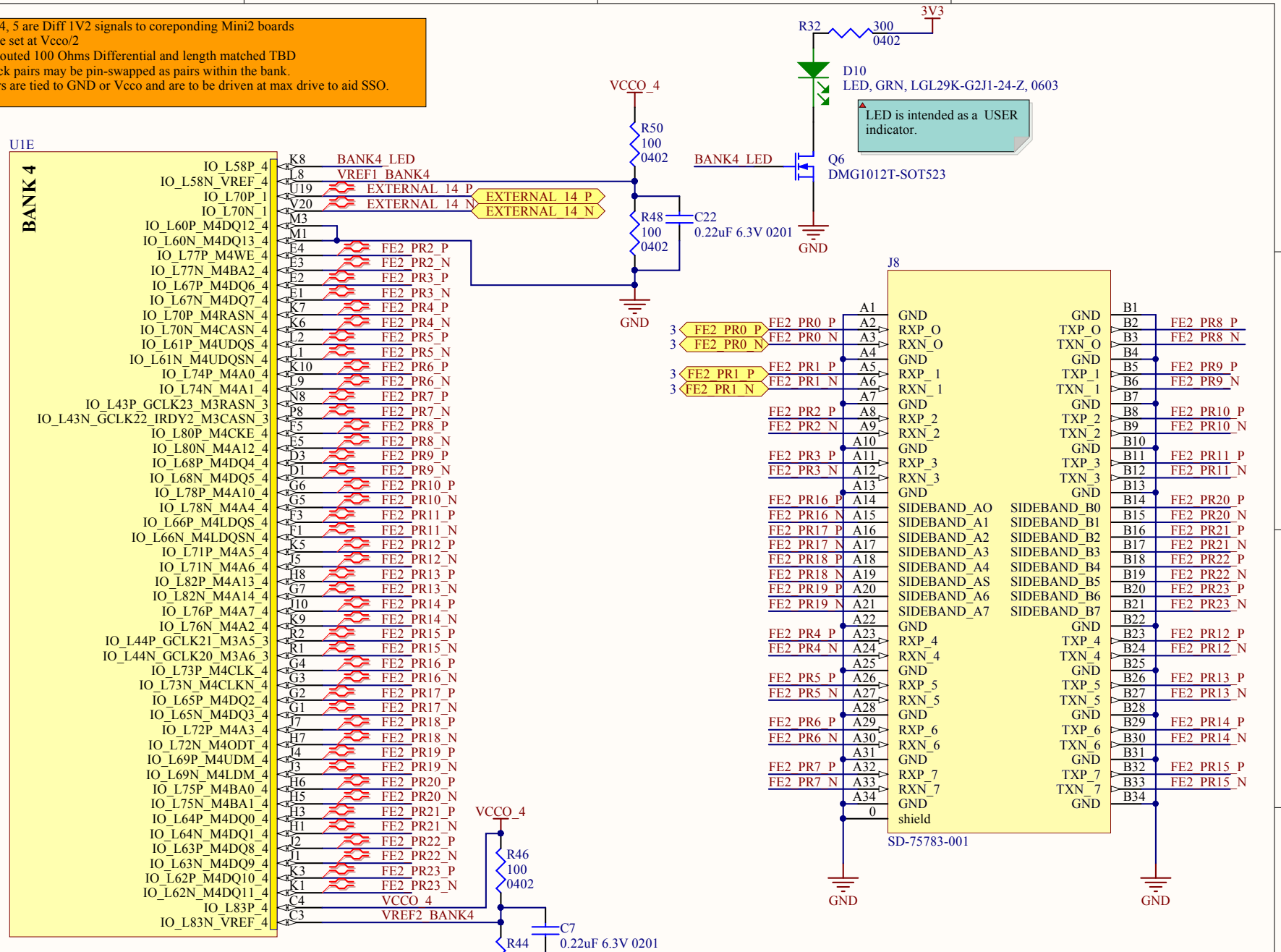
Size: B | Engineer: William Hart | Revision: A

Date: 5/4/2014 Time: 9:09:01 PM | Sheet 5 of 11

File: C:\Pjcts\AltProj\0300-S6 FMC\0300-S6 FMC\S6 Bank3.SchDoc | Drawn by: Karen Palmer

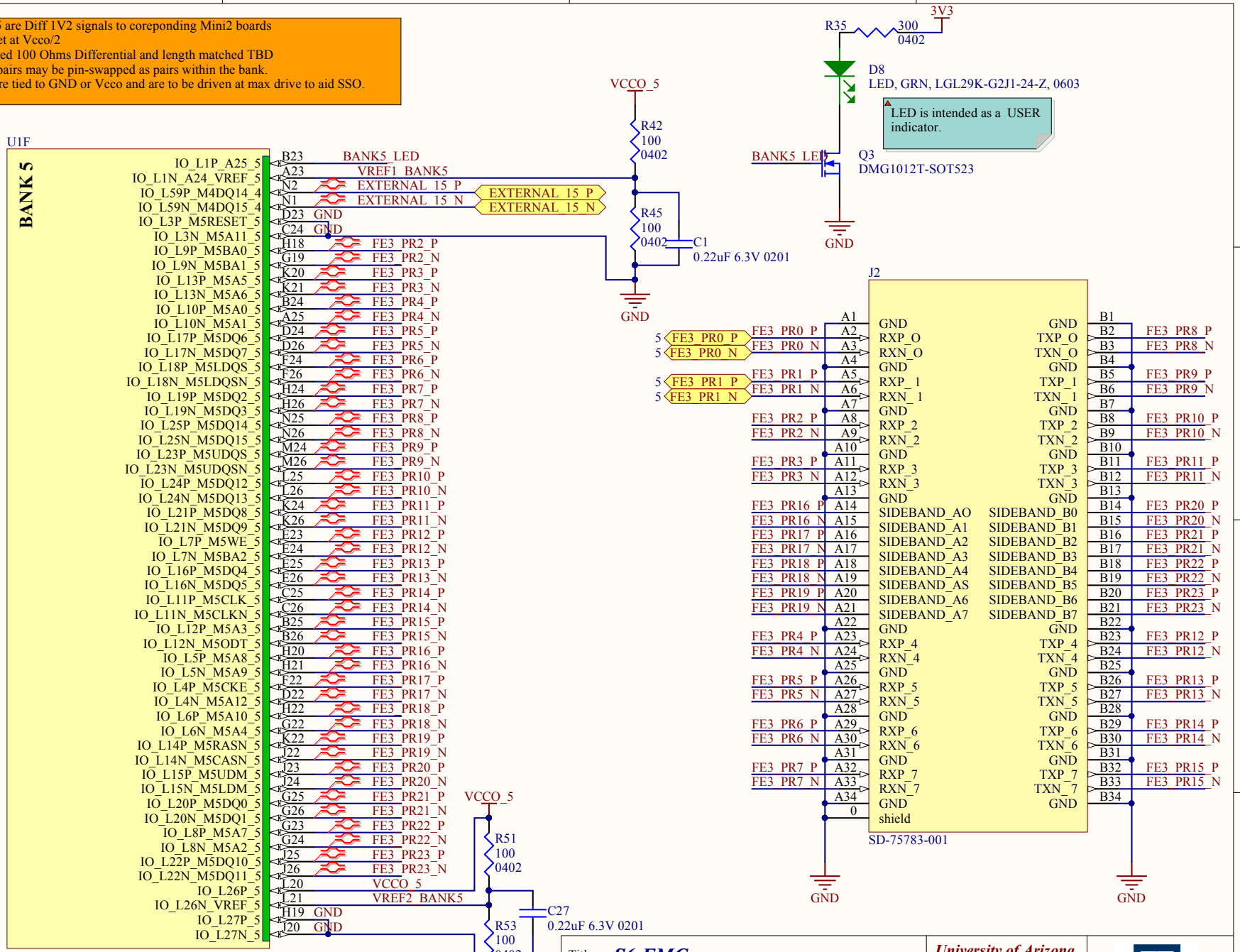
University of Arizona
1118 E 4th St
Tucson, Arizona 85721
billhart@email.arizona.edu

Banks 1, 3, 4, 5 are Diff 1V2 signals to coreponding Mini2 boards
Vref must be set at Vcco/2
Pairs to be routed 100 Ohms Differential and length matched TBD
All non-clock pairs may be pin-swapped as pairs within the bank.
Unused pairs are tied to GND or Vcco and are to be driven at max drive to aid SSO.

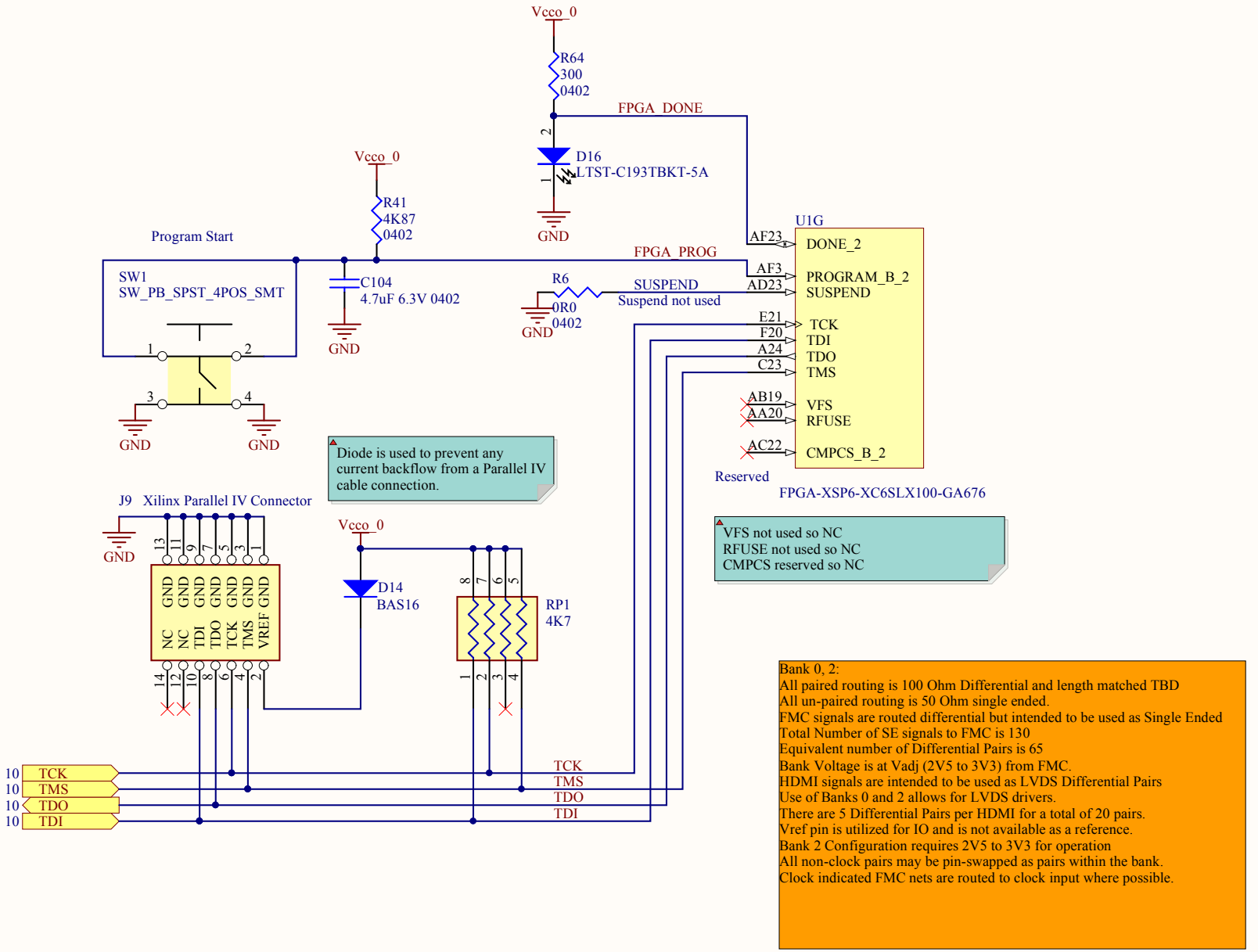


Title: **S6 FMC**			University of Arizona, 1118 E 4th St, Tucson, Arizona 85721
Size: A	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 5/4/2014	Time: 9:09:01 PM	Sheet 6 of 11	
File: C:\Pjcts\AltProj\0300-S6_FMC\0300-S6_FMC\S6_Bank4.SchDoc		Drawn by: Karen Palmer	

Banks 1, 3, 4, 5 are Diff 1V2 signals to coreponding Mini2 boards
Vref must be set at Vcco/2
Pairs to be routed 100 Ohms Differential and length matched TBD
All non-clock pairs may be pin-swapped as pairs within the bank.
Unused pairs are tied to GND or Vcco and are to be driven at max drive to aid SSO.



Title: **S6 FMC**			University of Arizona, 1118 E 4th St, Tucson, Arizona 85721
Size: A	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 5/4/2014	Time: 9:09:01 PM	Sheet 7 of 11	
File: C:\Pjcts\AltProj\0300-S6_FMC\0300-S6_FMC\S6_Bank5.SchDoc			Drawn by: Karen Palmer



Bank 0, 2:
All paired routing is 100 Ohm Differential and length matched TBD
All un-paired routing is 50 Ohm single ended.
FMC signals are routed differential but intended to be used as Single Ended
Total Number of SE signals to FMC is 130
Equivalent number of Differential Pairs is 65
Bank Voltage is at Vadj (2V5 to 3V3) from FMC.
HDMI signals are intended to be used as LVDS Differential Pairs
Use of Banks 0 and 2 allows for LVDS drivers.
There are 5 Differential Pairs per HDMI for a total of 20 pairs.
Vref pin is utilized for IO and is not available as a reference.
Bank 2 Configuration requires 2V5 to 3V3 for operation
All non-clock pairs may be pin-swapped as pairs within the bank.
Clock indicated FMC nets are routed to clock input where possible.

Title: **S6 FMC**			University of Arizona, 1118 E 4th St, Tucson, Arizona 85721
Size: A	Engineer: William Hart	Revision: A	billhart@email.arizona.edu
Date: 5/4/2014	Time: 9:09:01 PM	Sheet 8 of 11	
File: C:\Pjcts\AltProj\0300-S6_FMC\0300-S6_FMC\S6_Config.SchDoc			Drawn by: Karen Palmer

Supply MaxCapLoad	Range	Pins	Amps	Tolerance	
VADJ	0 - – 3.3V	4	4	+/- 5%	1000 uF
VIO_B_M2C	0 - VADJ	2	1.15	+/- 5%	500 uF
VREF_A_M2C	0 - VADJ	1	1mA	+/- 2%	10 uF
VREF_B_M2C	0 - - VIO_B_M2C	1	1mA	+/- 2%	10 uF
3P3VAUX	3.3V	1	20mA	+/- 5%	150 uF
3P3V	3.3V	4	3	+/- 5%	1000 uF
12P0V	12V	2	1	+/- 5%	1000 uF

Table 11. Power Supply Voltages for HPC connector

VOUT = RSET • 10µA
Use gaurd ring for Rset to min leakage
Tie gaurd ring to OUT.
RC Startup delay may be increased using Cset
Vctrl Dropout is 1.2 to 1.35V

LT3080's may be paralleled to obtain higher output current.
The SET pins are tied together and the IN pins are tied together. This is the same whether it's in three terminal mode or has separate input supplies. The outputs are connected in common using a small piece of PC trace as a ballast resistor to equalize the currents. PC trace resistance in milliohms/inch is shown in Table 1. Only a tiny area is needed for ballasting.

Table 1. PC Board Trace Resistance

WEIGHT (oz)	10 mil WIDTH	20 mil WIDTH
1	54.3	27.1
2	27.1	13.6

Trace resistance is measured in mOhms/inText

Vadj can be 3.3V (Avnet), 2.5V (Avnet, Glib, Kintex), or 1.8V max(Virtex)
V7 max on HP banks is 1V8, these are used by V707 FMC, so max Vadj for V7 is 1V8 ->
We can use Vadj on bank 0
Min S6 config voltage is 1V8
Max S6 config voltge is 5V0
bank2 must use 1V8-3V3 Flash
No 128b spi flash exists at 2.5V
Banks 0 and 2 carry the LVDS which can be 3V3, 2V5, should rcv ok at 1V8
Banks 0 and 2 carry FMC HA, HB, and LA lines which correspond to VAdj, carrier Vcco.

If we must operate bank2 at 1V8
Must generate 1V8 for bank2 when using K7, A7, V6
Could use Vadj for bank 2 with V7, but not safe for other setups.
S6 requires 2V5 on Vccaux if 1.8V is used on Bank 2.
Must generate 2V5 for Vccaux when using V7, else use Vadj.
Vadj must be set for 2V5 except for V7.
Low LVDS etc out on bank 2 always.
Low LVDS etc out on bank 0 with V7.

Better solution, use Voltge Translation on SPI Flash. Use Vadj on Bank 2.
Use STI1.05 to provide 2V5 to Vccaux.

Other banks operate at 1V2 provided from regulators from 3V3 or Vadj
Can use LT3080 since drop > 1.2V

Bypass Cap Requirements from ug393-tanle_2-1:

Vccint	1x100uF,	2x4.7uF,	4x0.47uF
Vccaux	2x100uF,	3x4.7uF,	6x0.47uF
Vcco_0	1x100uF,	1x4.7uF,	3x0.47uF
Vcco_1	1x100uF,	1x4.7uF,	3x0.47uF
Vcco_2	1x100uF,	1x4.7uF,	3x0.47uF
Vcco_3	1x100uF,	1x4.7uF,	3x0.47uF
Vcco_4	1x100uF,	1x4.7uF,	2x0.47uF
Vcco_5	1x100uF,	1x4.7uF,	2x0.47uF

Banks 1, 3, 4, 5 are 1V2 Vcco
Bank 0 is Vadj
Bank 2 is Vadj

Two 0.22 0201 Ceramic Caps are substituted for each Xilinx recommended 0.47 0402 Ceramic Caps.

S6 Data Sheet: Table 2 Note 11

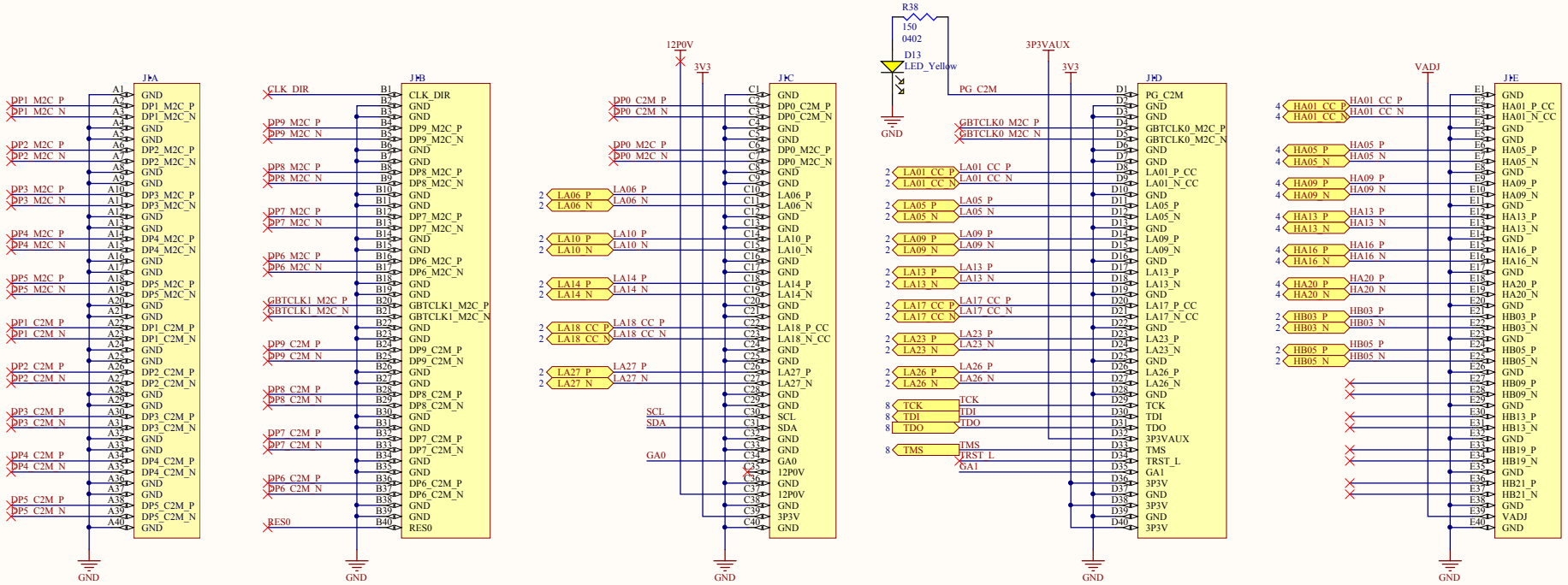
Iccintq (Vccint Quiescent) = 36mA
Iccoq (Vcco Quiescent) = 4mA *4=16@1V2 + 4 + 4 + 4 = 24mA
Iccauxq (Vaux Quiescent) = 7mA
LVCMOS25 or 33 = 2-24mA per pin => 100mA max/bank
SSTL / HSTL 0.8mA per pin

Thus:
1.2V => 4*100mA + 24mA + ?? + 36mA +?? = 460mA +
Vadj => 2*100mA +
2.5V => 9mA + 100mA?
3.3V => 8*10mA(led) + 20mA (flash) + 10mA(osc) + 460mA
(1.2) + 100mA(2.5)

FPGA-XSP6-XC6SLX100-GA676

FPGA-XSP6-XC6SLX100-GA676

Title:	S6 FMC			University of Arizona 1118 E 4th St Tucson, Arizona 85721	
Size: C	Engineer: William Hart		Revision: A	billhart@email.arizona.edu	
Date: 5/4/2014	Time: 9:09:01 PM	Sheet 9 of 11			
File: C:\Pjcts\AltProj\0300-S6 FMC\0300-S6 FMC\S6 Power.SchDoc			Drawn by: Karen Palmer		



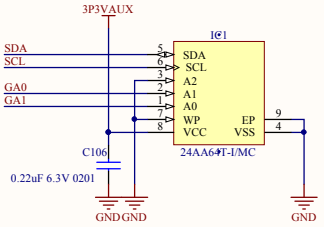
FMC Net Name Nomenclature:

C2M:	Carrier to Mezzanine
DP:	Multi Gigabit Transceiver Data Pair
HA:	High Pin Count "A" Bus
HB:	High Pin Count "B" Bus
HPC:	High Pin Count
LA:	Low Pin Count "A" Bus
LPC:	Low Pin Count
M2C:	Mezzanine to Carrier
MGT:	Multi Gigabit Transceiver
PG:	Power Good
RES:	Reserved
VADJ:	Carrier Supplied Programmable Voltage, 2V5 to 3V3.

CC-ended lines are renamed, because Altium Designer treats only P and N ended line names as a differential pairs.

Warning!
Following the VITA 57.1 standard:
GA0 goes to A1
GA1 goes to A0

24AA64T	= 1 0 1 0 0 GA0 GA1
MCP9801	= 1 0 0 1 0 GA0 GA1



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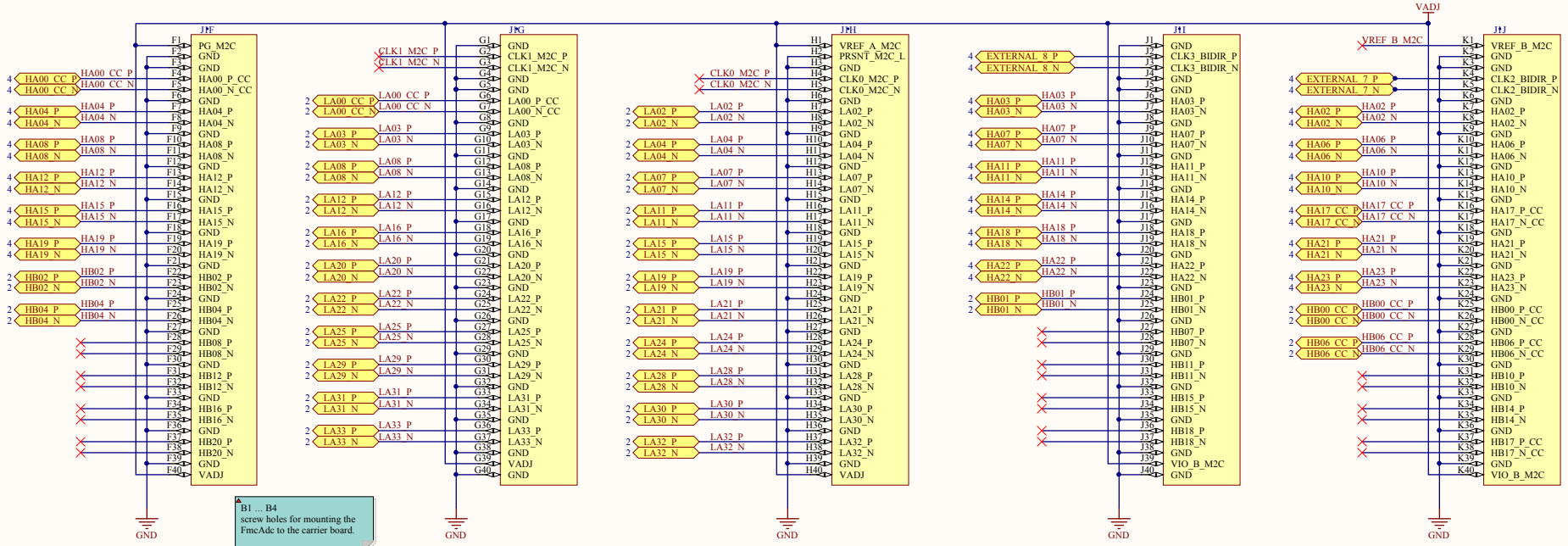
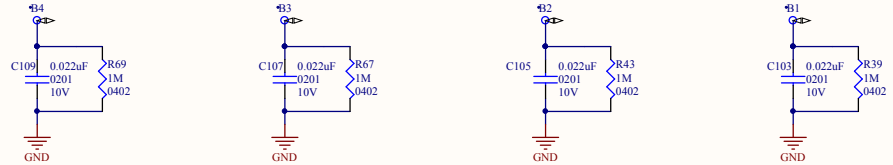
Date: 5/4/2014	Time: 9:09:01 PM	Sheet 10 of 11	Drawn By: Karen Palmer
File: C:\Pjcts\AltPro\0300-S6 FMC\0300-S6 FMC\FMC Connector.SchDoc			

CC-ended lines are renamed, because Altium Designer treats only P and N ended line names as a differential pairs.



B1 ... B4
screw holes for mounting the FmcAdc to the carrier board.

VIO_B is always set to Vadj



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