Muon Trigger Card (MTCxx)

Functional Specification

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Introduction

This document is the revised specification for the Muon Trigger Card (MTCxx), this revision of the card is completely compatible with the previous version of MTCxx and can be used interchangeably with the previous version. In addition, this new MTCxx is

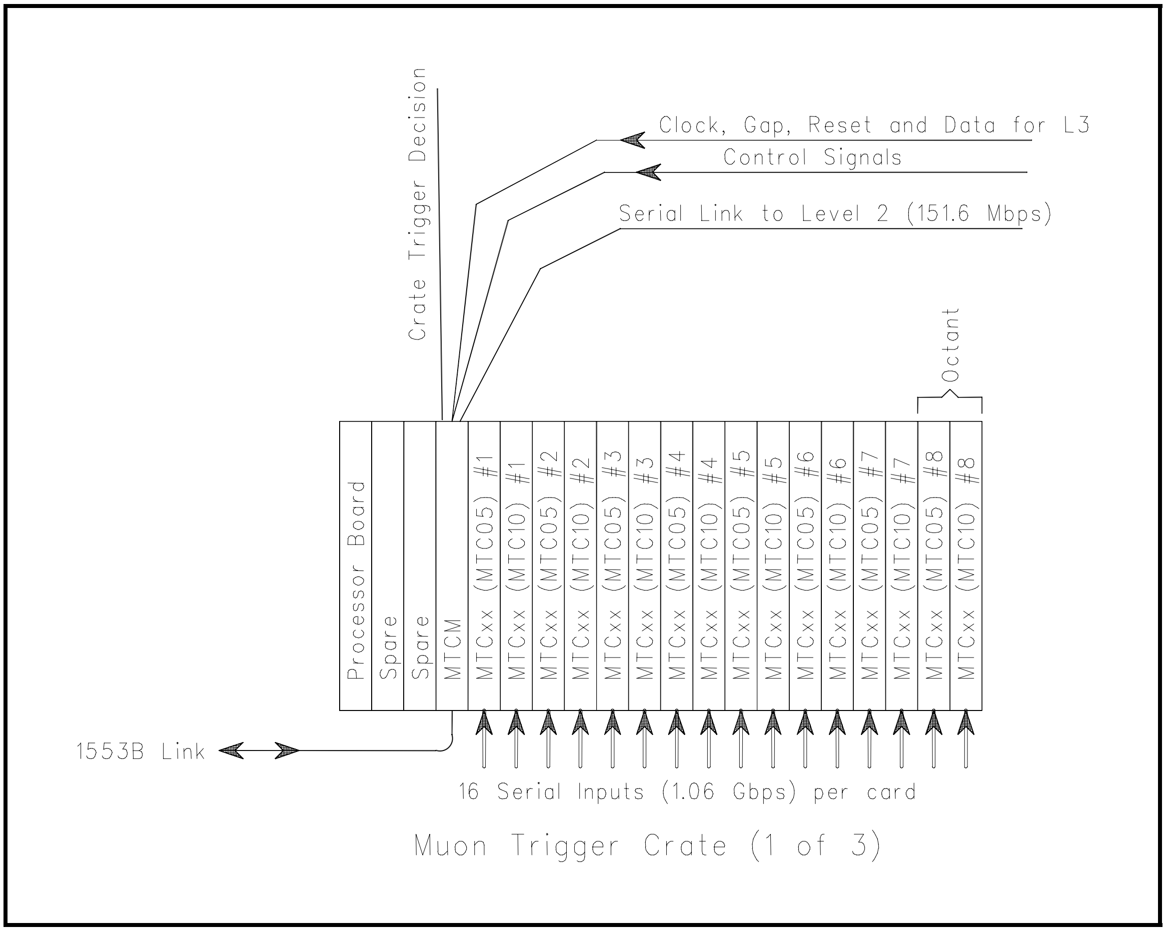


Figure 1 - Muon Trigger Crate

capable of taking advantage of added capabilities of the Universal Flavor Board (PCB-0170), including the ability to add 4 more serial transceivers (located on the Universal Flavor Board) to the MTCxx board.

An overview of the Level 1 Muon (L1MU) trigger system for Run II of the D0 experiment is given in [1]. Data from the Level 1 Central Fiber Tracker (L1CFT) trigger, Muon Centroid Cards (MCEN's), and muon front end cards are sent to the MTC05 and/or MTC10 cards via Gbit/s serial links. The MTC05 and MTC10 cards reside in three custom VME crates, referred to as Muon Trigger Crates, on the detector platform, a diagram of the crate is shown in Figure 1. The three Muon Trigger Crates correspond to three geographic regions of the detector, north, south, and central. Each pair of MTC05 and MTC10 cards each form an trigger decision for one octant within a region. The octant trigger decisions of the eight MTC05 and MTC10 cards are read by the Muon Trigger Crate Manager (MTCM) that subsequently uses this information to form a regional trigger decision. The three regional trigger decisions are sent to the Muon Trigger Manager (MTM) that subsequently uses this information to form the global muon trigger decision that is sent to the Level 1 Trigger Framework (TF).

The Muon Trigger Card (MTCxx) performs most of the trigger logic in the L1MU trigger system. It is transformed into different versions by means of a Muon Trigger Flavor Board (MTFB). The MTFB is a daughter board that connects to the MTCxx card. Thus, MTCxx cards are transformed into MTC05, MTC10, or MTM cards by using the appropriate MTFB. The term MTCxx is used as a shorthand notation when referring to the MTC05 and MTC10 cards. This document specifies the MTCxx card. The various MTFB's are described in separate documents.

The MTCxx is a 9U x 400mm VME card and provides the following functions:

⇒ Accepts up to 20 coaxial input cables (when equipped with the Universal Flavor Board). Each cable contains up to 96 bits of hit information from the L1CFT, MCEN cards, and/or muon front end electronics. This information is transmitted over serial links at 1063 Mbits/s.

⇒ Deserializes, synchronizes and buffers this hit information so that the information, received over 20 separate cables from a given Bunch Crossing (BC), can be presented to the trigger logic on the MTFB simultaneously. Each old style MTFB daughter board has as input 16 x 16 lines from the MTCxx, the new Universal MTFB has as input these 16 x 16 lines plus an additional 4 cables that supply an additional 4 x 16 lines to the Flavor Board logic.

⇒ Sends up to 36 bits of octant trigger decision information to the MTCM for each Bunch crossing. This data is output in 3 12 bit parallel data transfers for each pair of MTC05/MTC10 cards, the division of bits from each MTCxx can vary for each different type of card. This octant trigger decision data is buffered on the MTCM.

⇒ Generates and buffers 16 bits of supplemental information for each BC. The supplemental information must be buffered pending L1 and, if necessary, L2 decisions and readout by the MTCM for transfer to the Muon Readout Card (MRC).

⇒ Buffers all input data. Input Data is stored for all inputs pending L1 and L2 decisions and possible transfer to the MRC through the MTCM. The MTCM transfers 1 of N accepted Bunch Crossings, where N is set to a number from 0 (meaning no data transfer to higher levels) to N, where N is set in the MTCM.

⇒ Generates N bits of error and M bits of status information for each BC. We call this the "running" error and status information since it is updated each BC. A copy of the error information which is "latched" is also kept. In this case error bits are held high until cleared using a "0" overwrite. The "running" error and status data must be buffered pending an L1 decision, an L2 decision, and readout to the MRC.

⇒ Buffers internal BC number along with the associated input data for possible transfer to the MRC.

⇒ Receives timing and trigger information from the MTCM over the backplane.

⇒ On receipt of an L1 Accept, allows the MTCM to read its supplemental trigger, error and status information, input data, and any version data for inclusion in the data sent to the MRC. Version data specifies different versions of logic used on the MTCxx card or MTFB board. ?? is the MTCxx BC number read as well

⇒ Generates an L1 Error signal to the MTCM on any MTCxx error condition. The L1 Error signal is generated asynchronously and remains active until the condition that caused it is cleared or the data that caused the error is masked off..

- Synchronization error on a serial input line from the muon front end electronics, MCEN cards, or L1CFT.

- Mismatch between the BC number sent by the MTCM and the internal BC number on the MTCxx

⇒ Generates an L1 Busy signal to the MTCM on an MTCxx busy condition, indicating that the MTCxx can process no more data. The L1 Busy signal is sent asynchronously to the MTCM, and stays active until the MTCxx can once again process data.

⇒ Can mask individual inputs. There are several types of masks for each input. These include mask to include a channel in error generation, mask to include a channel in the trigger, mask to readout the input data.

⇒ Stores all FPGA programs in appropriate, non-volatile memory. This includes any FPGAs that are used on any MTFB, as well as the FPGAs on the MTCxx itself.

⇒ Loads the FPGA programs under program control from the non-volatile memories.

⇒ Allows test pattern information to be used in lieu of data sent to the MTFBs. That is, keeping all timing the same, substitutes test patterns for the actual data sent to the MTFB.

⇒ The MTCxx that is used with the MTM MTFB must provide 2 40 conductor twist and flat output cables. These cables carry the L1MU global trigger decision to the TF.

⇒ An extension of the MTCxx board has all input data buffered pending an L1 trigger decision. On receipt of an L1 accept, the input data is sent via an optical link to L2MU. The optical driver is implemented on a daughter board. The location of the control logic for sending this information still needs to be decided.

A detailed block diagram of the MTCxx can be found in Appendix A.

1. Inputs/Outputs

1.1 VME Bus (J1 and J2 Connectors)

The MTCxx has a VME interface using 32 bit addressing and is capable of 16 or 32 bit data transfers. The MTCxx is a VME slave and responds to address modifiers 09_h and xxx. The MTCxx VME Bus uses a 160 pin DIN connector on J1 that is consistent with the VME64x specification. The MTCxx VME Bus uses a 96 pin DIN connector on J2. The pin assignments for J1 and J2 can be found in Appendices B and C.

1.2 Connections to MTCM Board (J2 Connector)

The J2 connector is used to communicate between the MTCxx cards and MTCM. This connector is a 96 pin DIN type connector in order to accommodate all the required signals, as well as the standard VME data and address lines used in row B of the connector. Section 2.2.1 describes these signals in rows A and C and the pin assignments are given in Appendix C.

1.2.1 J2 Connections

The following is a list of the signals that exist on rows A and C of the J2 connector. For each signal, we indicate the signal name, the type of signal (TTL, PECL, etc.), and the source and destination of the signal. The actual pin assignments for J2 can be found in Appendix C.

- ⇒ RF_CLOCK - (Differential PECL) - (from MTCM to MTCxxs) 8 differential signals that are distributed as one for each pair of MTC05 and MTC10 cards in the crate. This is the 53 MHz RF clock that is received from the MRC.

- ⇒ CDD[00:11] - (TTL) - (from each MTCxx to the MTCM) – These 12 lines carry Card Decision Data from each pair of MTC05 and MTC10 cards. The lines are common for each pair of cards. The pair of cards places three sets of 12 bit trigger decision data on these lines in response to Synch L05. Data is placed on the lines at counts 1, 3, and 5 after Synch L05 is received. Which cards place what data on the lines defined in the Data Multiplexer FPGA.

- ⇒ BC_COUNT[0:7] - (TTL, terminated on backplane) - (from MTCM to MTCxxs) - This bus contains the Bunch Crossing number to associate with the data when the L1 ACCEPT signal is active. We use the words beam crossing and bunch crossing interchangeably.

- ⇒ SYNCH_L05 - (TTL, terminated on backplane) - (from MTCM to MTCxxs) - Indicates the first RF clock in a bunch crossing. This signal is used to time the Card Decision Data transfers from the MTCxxs to the MTCM

⇒ SEND_DATA - (TTL, terminated on backplane) - (from MTCM to MTCxxs) – This signal is used to tell the MTCxx to send the Card Decision Data to the MTCM. This signal is generated by the MTCM from the DATA_READY signal.

⇒ L1_ACCEPT - (TTL, terminated on the backplane) - (from MTCM to MTCxxs) - Signal to indicate that the crate has received an L1 ACCEPT from the trigger framework. Receipt of an L1 ACCEPT means that the data associated with the beam crossing that produced the L1 ACCEPT should be saved and that L2 Data should be sent to the Level 2 trigger system by the MTCM. On L1 ACCEPT, 12 bits of supplemental data is read from each MTCxx card and this data forms part of the L2 Data block. The beam crossing that generated the L1 ACCEPT is found on BC COUNT. An L1 ACCEPT or REJECT is produced for each beam crossing. L1 REJECT is defined as an absence of L1 ACCEPT.

⇒ L2_ACCEPT - (TTL, terminated on the backplane) - (from MTCM to MTCxxs) - Signal to indicate that the crate has received an L2 ACCEPT signal from the trigger framework. Receipt of an L2 ACCEPT means that a beam crossing for which there was an L1 ACCEPT passed the Level 2 trigger. The resulting action is to send L3 Data to the Level 3 trigger system from the MTCM. The address of the data on each MTCxx card that is read by the MTCM in response to L2 ACCEPT is found in the Buffer Pointer FIFO.

⇒ L2_REJECT - (TTL, terminated on the backplane) - (from MTCM to MTCxxs) - Signal to indicate that the crate has received and L2 REJECT signal from the trigger framework. The resulting action is to drop all data associated with the beam crossing to which the L2 REJECT corresponds. That is, the buffer that held this data is freed for use.

⇒ First_Crossing - (TTL, terminated on the backplane) - This signal indicates the beginning of a turn. The First_Crossing signal is associated with the sixth bunch crossing before the first bunch crossing that contains real beam. This signal resets the BC number (but not the turn number). This signal also causes the internal Turn Number on the MTCM to be reset for the first RESET signal received after a Master_Reset signal.

⇒ SYNCH_GAP - (TTL, terminated on the backplane) - (from MTCM to MTCxxs) - This signal indicates that beam crossings are in the Synch Gap. No real beam crossings take place in the Synch Gap. During the Synch Gap it is expected that front-ends will send k28.5 characters to the MTCxx in place of data. Thus during the Synch Gap we expect that the input FIFO’s would empty and the INPUT_READY signal would go low

⇒ GAP - (TTL, terminated on the backplane) - (from MTCM to MTCxxs) - This signal indicates the presence of the other two abort gaps (in the present accelerator plan). While there are no actual beam crossings during these gaps, data should be from the front-ends to the MTCxx. One can imagine using data in these GAPS for cosmic ray triggering.

⇒ INPUT_READY - (Open Collector TTL, pulled up on the MTCM) - (from MTCxxs to MTCM) - This signal is a "wire-or" that contains a high level signal when all of the MTCxxs in the crate have non-empty conditions in all of the input FIFOs that have not been masked off. If this signal does not go low during the Synch Gap or high at the appropriate time after the Sync Gap, this is an indication of an error condition to the MTCM.

⇒ DATA_READY - (Open Collector TTL, pulled up on the MTCM) - (from MTCxxs to MTCM) - This signal is a "wire-or" that contains a high level signal when all of the MTCxxs in the crate have data ready to transfer to the MTCM. Each MTCxx will release this signal when all of its active serial inputs, that have not been masked off on initialization, have received at least one byte of data and the card has created its Card Trigger Data.

⇒ BC_CLOCK - (TTL, terminated on the backplane) - (From MTCM to MTCxxs) Bunch Crossing Clock created by the MTCM. This clock, which runs continuously, is synchronous to the Bunch Crossing Clock created by the MTCM.

⇒ LEVEL_1_BUSY* - (Open Collector TTL, pulled up on the MTCM) - "Wire-or" signal, each MTCxx can cause this line to go low if there is a memory or FIFO full condition that would make it impossible for the board to process a L1 ACCEPT signal.

⇒ LEVEL_2_BUSY* - (Open Collector TTL, pulled up on the MTCM) - "Wire-or" signal, each MTCxx can cause this line to go low if there is a condition that make it impossible for the board to process an L2 ACCEPT signal. (Note, that at the time of this writing there is no condition that can cause this to occur)

⇒ LEVEL_1_ERROR* - (Open Collector TTL, pulled up on the MTCM) - "Wire-or" signal, each MTCxx can cause this line to go low if there is an error condition that needs to be reported to the MRC. This error could be caused by a mis-match between the expected and received BC Number for a L1 ACCEPT, L2 ACCEPT or L2 REJECT. This error could also be caused by an inoperative serial receiver on a MTCxx Board.

⇒ RESET_COUNTERS - (TTL, terminated on the backplane) - (from MTCM to MTCxxs) - Signal that causes the MTCxxs to reset their internal BC counters

⇒ MASTER_RESET - (TTL, terminated on backplane) - (from MTCM to MTCxxs) - Master reset generated from the initialize command that causes all internal counters, registers and FIFOs to be reset to initial condition.

1.3 Front Panel Parallel Connections (J11 and J12 Connectors)

There are 2 parallel connectors located on the front panel of the MTCxx card. J12 is used for test points generated on the flavor board as well as for programming the FPGAs on the MTCxx. The first 28 pins of J12 are directly wired to the Flavor Card, while the remaining 12 pins are used to program the FPGAs on the MTCxx. J11 is directly wired from P7 connector on the Flavor Board and is intended to be used as the connector to the Trigger Framework when the MTCxx is used as a MTM card. Pinouts for the Flavor Board connectors are in Appendix D.

1.4 Serial Connections (J3 and J4 Connectors)

The serial connections on this card are through 16 coax connectors which mate through the 2 connectors that are located on a tail at the back of the MTCxx card. The connectors are D type connectors (CONEC P/N CFM8W8S-K100 or equivalent) with 50Ω coax inserts. External to the card, the signals are carried on LMR-200 cable, manufactured by Times Microwave, that is similar to RG-58 but with a higher signal propagation velocity. Internal to the card, the signals are carried on RG-316. The serial links chosen for this application use the AMCC S2042 and S2043 parts. The serial links are implemented on serial link daughter boards (SLDB's) that plug into the appropriate mother board. In the case of the MTCxx, 16 SLDB receivers plug directly into the MTCxx card. The serialization is compatible with the Fibre Channel specification. The links operate at word rate of 53 MHz which gives a serial rate of 1060 Mbits/s after 8b/10b encoding. Additional details can be found in the specification documents for the SLDB transmitters and receivers.

The MTCxx expects that data will be transmitted during all beam crossings except those in the Synch Gap. During the Synch Gap the MTCxx expects that Fiber Channel Synch Characters (K28.5) will be sent. The serial link data received by the MTCxx cards has the form:

Word #	Description
1	Data (detector hits or one CFT track)
2	Data (detector hits or one CFT track)
3	Data (detector hits or one CFT track)
4	Data (detector hits or one CFT track)
5	Data (detector hits or one CFT track)
6	Data (detector hits or one CFT track)
7	Longitudinal Parity

1.5 MTCxx Trigger Output for the L1 Muon Trigger Decision

After data from the 16 serial links is deserialized it is sent to16 Input FIFOs, one for each serial link. Once all Input FIFOs on the board are Not Empty, the data is clocked onto the Muon Trigger Flavor Board (MTFB). The MTFB determines which FPGA trigger logic is used on the MTCxx card. Presently there are three flavors: MTC05, MTC10, and MTM. One could envision as many as five flavors though: CF and EF MTC05, CF and EF MTC10, and MTM. The trigger logic for each of these flavor boards is described in the corresponding MTFB document. The I/O for the MTFB is given in Appendix D.

Data is clocked out of the Input FIFOs at 53 MHz and the data from each FIFO is 16 bits wide. Each MTC05 and MTC10 MTFB produces a card level, 36 bit wide trigger decision every 7 RF clock cycles. This data is sent to a multiplexer where it is split into three 12 bit words, which are stored in a separate FIFO until instructed to start reading

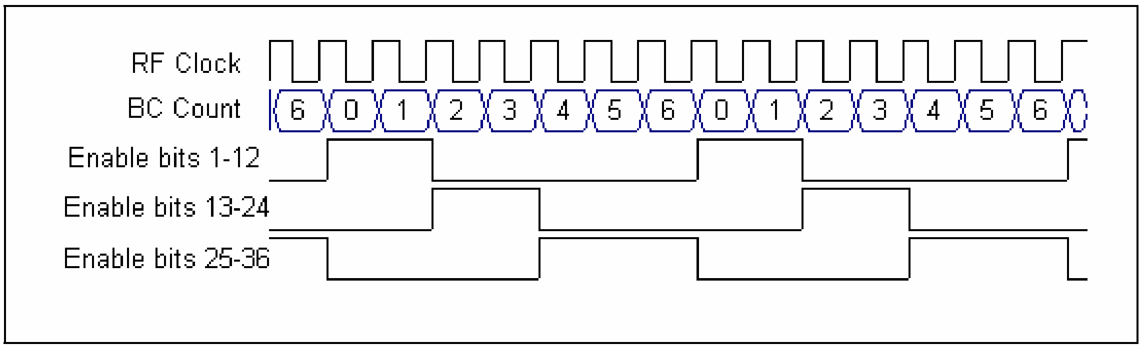


Figure 2 - Backplane Multiplexer Timing

data by the MTCM, at which point the data is sent to the backplane for inclusion in the crate trigger decision. Additionally, there are selectors on each card that enable 4 bit pieces onto the J2 backplane. For each pair of MTC05 and MTC10 cards then, 36 bits of card trigger decision are sent to the MTCM. The 36 bits are sent as three 12 bit words, one on RF clock cycles 1 and 2, one on RF clock cycles 3 and 4, and the last on clock cycles 5, 6, and 7, as shown in Figure 2. The 4 bit selectors on each card choose whether a given 4 bits placed on the bus comes from the MTC05 or MTC10 card. All 36 bits can come from either card or any combination thereof in 4 bit pieces.

For the MTC05 cards, there are 4 P_T bins, a 2 bit multiplicity counter, 3 levels of quality, and 2 bins of eta. For the MTC10 cards, there are 2 P_T bins, a 2 bit multiplicity counter, and 3 levels of quality. An example of the 36 card level trigger decision bits is shown below. Further details can be found in the MTFB document.

1.5.1 EF MTC05 Card Trigger Decision Bits

Bits	Description
0,1	2 bit counter for threshold pt1 sign0
2,3	2 bit counter for threshold pt1 sign1
4,5	2 bit counter for threshold pt2, loose
6,7	2 bit counter for threshold pt2, tight
8,9	2 bit counter for threshold pt3, loose
10,11	2 bit counter for threshold pt3, tight
12,13	2 bit counter for threshold pt4, loose
14,15	2 bit counter for threshold pt4, tight
16,17	2 bit counter for no CFT region
18-23	Unassigned

1.5.2 EF MTC10 Card Trigger Decision Bits

Bits	Description
0,1	2 bit counter for A MDT centroids
2,3	2 bit counter for AB MDT centroid correlations
4,5	2 bit counter for AB and BC centroid correlations
6,7	2 bit counter for A MDT centroid correlations no CFT region
8,9	2 bit counter for AB and BC centroid correlations no CFT region
10,11	Unassigned

1.6 MTCxx Output Upon L1 ACCEPT

On receipt of an L1 ACCEPT, the MTCxx card also provides 16 bits of supplemental trigger information for each card. These bits are read by the MTCM as 16 bit VME data transfers. For each transfer, the MTCM first reads the location of the event that corresponds to the L1 ACCEPT from the L2 Pending FIFO on the MTCxx card. Using this address as an offset, the MTCM then reads 16 bits of supplemental trigger information. Thus there are a total of 32 VME reads for each L1 ACCEPT. The supplemental data for the MTC05 and MTC10 cards is given below. This data is subsequently buffered on the MTCM pending an L2 ACCEPT.

1.6.1 EF MTC05 Supplemental Trigger Bits

Bits	Description
0-11	12 bits of phi information
11-15	Unassigned

1.6.2 EF MTC10 Supplemental Trigger Data

Bits	Description
0-11	12 bits of eta information
12-15	Unassigned

1.7 MTCxx Output Upon L2 ACCEPT

Upon an L2 ACCEPT, the MTCM reads additional information to be included in the L1MU trigger data that is sent to L3 via the MRC and VBD. This information includes error and status information, the internal bunch crossing number generated on the card, and the internal turn number generated on the card. Optionally, all input data to the MTCxx card can be readout and transferred to L3 as well.

The data is read by the MTCM using VME reads. Upon an L2 ACCEPT the MTCM reads from each MTCxx card the Buffer Transfer List FIFO. The MTCM subsequently reads the error, status, bunch crossing and turn numbers, and card input data from the MTCxx card using this address as an offset. The VME reads are 32 bit data transfers. There are 16 reads for the addresses and either 32 (2 per board) or 192 (12 per board) reads depending on whether or not the card input data is readout in addition to the status and error information.

2. Status and Error Words

2.1 MTCxx Error Words

There are two sets of error words in place on the MTCxx card. The first is a set of "running" errors that is updated each bunch crossing. The second is a set of "latched" errors that are held high until cleared during initialization or by writing a "0" to the word.

The first set is meant to be readout as part of the L1MU trigger data. The second set is meant to be monitored by the alarm system during the run. The error conditions are described below. The memory location of the error words are given in Appendix G.

Serial Lock Okay Error: This error is contained in 2 words, 0x000088 contains information for Receivers 1 to 16 in bits 0 to 15 and 0x0000b0 contains information for Receivers 17 t0 20 in bits 0 to 3. If the Lock Okay signal on the SLDB receiver goes low, it indicates that the PLL is in an out-of-lock state. This would happen if a serial link cable was unplugged for example. Writing a high to the corresponding bit will cause a receiver to be reset. A latched version of this register is located at 0x00008a for receivers 1 to 16 and 0x0000b2 for receivers 17 to 20. The latched register can only be reset by being overwritten.

Parity Error: This error is contained in 2 words, 0x000090 contains information for Receivers 1 to 16 in bits 0 to 15 and 0x0000b8 contains information for Receivers 17 t0 20 in bits 0 to 3. It indicates that a parity error has been detected on the incoming serial link data. A latched version of this register is located at 0x000092 for receivers 1 to 16 and 0x0000ba for receivers 17 to 20. The latched register can only be reset by being overwritten.

General Purpose Error: This memory location holds (0x000084) several summaries of different errors and statuses. A latched version (of errors only) of this register is located at 0x000086. The latched register can only be reset by being overwritten.

Byte.Bit	Read Description
1.0	Any Receive FIFO Full
1.1	No Input FIFO Empty
1.2	OR of Lock Okay Errors
1.3	OR of Parity Errors
1.4	Results Buffer Full
1.5	Results Buffer Empty
1.6	Unassigned
1.7	Unassigned
2.0	Unassigned
2.1	Unassigned
2.2	Unassigned
2.3	Unassigned
2.4	Unassigned
2.5	Unassigned
2.6	Unassigned
2.7	Unassigned

Buffer FIFO Status and Error: This is a read only word that monitors the full and empty flags of the four buffer pointer FIFOs (Empty Buffer, L1 Pending, L2 Pending and Transfer). This register is located at 0x000080.

Byte.Bit	Read Description
1.0	Empty Buffer Full
1.1	L1 Pending Buffer Full
1.2	L2 Pending Buffer Full
1.3	Transfer Buffer Full
1.4	Empty Buffer Empty
1.5	L1 Pending Buffer Empty
1.6	L2 Pending Buffer Empty
1.7	Transfer Buffer Empty
2.0	Unassigned
2.1	Unassigned
2.2	Unassigned
2.3	Unassigned
2.4	Unassigned
2.5	Unassigned
2.6	Unassigned
2.7	Unassigned

2.2 MTCxx Flash Memory Status/Control Word (Register 0x20)

Byte.Bit	Write Description	Read Description
1.0	Configure Sector 0	Configure Sector 0
1.1	Configure Sector 1	Configure Sector 1
1.2	Configure Sector 2	Configure Sector 2
1.3	Configure Sector 3	Configure Sector 3
1.4	Configure FPGA from Flash	FPGA being configured
1.5	Configuration Error Overwrite	Configuration Error
1.6	Configure Sector 4	Configure Sector 4
1.7	Transfer Address 4	Transfer Address 4
2.0 (1.8)	Transfer Address 0	Transfer Address 0
2.1 (1.9)	Transfer Address 1	Transfer Address 1
2.2 (1.10)	Transfer Address 2	Transfer Address 2
2.3 (1.11)	Transfer Address 3	Transfer Address 3
2.4 (1.12)	Transfer Data to Flash	Flash Memory Busy
2.5 (1.13)	Flash Memory Error Overwrite	Flash Memory Error
2.6 (1.14)	Transfer Single Sector	Transfer Single Sector
2.7 (1.15)	Reset Flash Memory Area	Flash Memory Done

The MTCxx Status/Control Word is used to put the MTCxx into Test Mode and to oversee the operation of the MTCxx's Flash Memory. The Flash Memory is a 1Mbyte device that contains the programming data for the FPGAs on the Flavor Board. The operation of the Flash Memory is described in section 5.

2.3 MTCxx Test Status/Control Word (Register 0x22)

Byte.Bit	Write Description	Read Description
1.0	Test Mode Single	Test Mode Single Confirmed
1.1	Test Mode Continuous	Test Mode Continuous Confirmed-1
1.2	Unassigned	Unassigned
1.3	Unassigned	Unassigned
1.4	Unassigned	Unassigned
1.5	Unassigned	Unassigned
1.6	Disable –5v	Disable –5v Confirmed
1.7	Programmed Reset	Confirm Programmed Reset
2.0	Unassigned	Unassigned
2.1	Unassigned	Unassigned
2.2	Unassigned	Unassigned
2.3	Unassigned	Unassigned
2.4	Unassigned	Unassigned
2.5	Unassigned	Unassigned
2.6	Unassigned	Unassigned
2.7	Unassigned	Unassigned

2.4 Multiplexer Control Word (Register 0x0e)

The Multiplexer Control Word is used to control during which of the 3 time slots in each bunch crossing the data from the flavor board is output. The 36 bits from the flavor board are divided into 3 groups of 12 bits, each enabled for one of the time slots (TS1, TS 2 and TS 3). This data is enabled onto the 12 backplane bits one nibble at a time under the control of the bits in this word.

Byte.Bit	Write Description	Read Description
1.0	TS 1, Nibble 1	TS 1, Nibble 1 Confirmed
1.1	TS 1, Nibble 2	TS 1, Nibble 2 Confirmed
1.2	TS 1, Nibble 3	TS 1, Nibble 3 Confirmed
1.3	TS 2, Nibble 1	TS 2, Nibble 1 Confirmed
1.4	TS 2, Nibble 2	TS 2, Nibble 2 Confirmed
1.5	TS 2, Nibble 3	TS 2, Nibble 3 Confirmed
1.6	TS 3, Nibble 1	TS 3, Nibble 1 Confirmed
1.7	TS 3, Nibble 2	TS 3, Nibble 2 Confirmed
2.0 (1.8)	TS 3, Nibble 3	TS 3, Nibble 3 Confirmed
2.1 (1.9)	FB Trigger OR	FB Trigger OR Confirmed
2.2 (1.10)	Unassigned	Unassigned
2.3 (1.11)	Unassigned	Unassigned
2.4 (1.12)	Unassigned	Unassigned
2.5 (1.13)	Unassigned	Unassigned
2.6 (1.14)	Unassigned	Unassigned
2.7 (1.15)	Reset FIFOs	Confirm Reset FIFOs

Bit 9 controls the source of the Trigger OR signal, low uses an internally generated Trigger OR awjile high uses the Trigger OR from the Flavor Board. Bit 15 resets the FIFOs when set high.

3. MTCxx Test Modes

One of the more difficult problems to be solved in the L1MU trigger system is the verification of the MTFB logic. One way this is done during running is to read out all input data, use the Fortran trigger simulator code to produce 36 bits of card trigger decision data, and compare that with the actual card trigger decision generated by the muon trigger card. If a disagreement is found, it is useful to have some way to debug the problem. For reference, we make use of two simulators. The first is the timing and logic simulator in MAXPLUS. The second is a Fortran trigger simulator. The former can be used to check the FPGA logic. The latter can be used to verify that the trigger decision is the one desired from a physics standpoint.

Should a disagreement between Fortran trigger simulator and MTCxx output be found one would first verify the result using the Fortran trigger simulator and MAXPLUS timing and logic simulator. If the disagreement appears to be real, one could use the Muon Trigger Test (MTT) card and load its input FIFO's with the MTCxx input data that resulted in a disagreement. An alternate method of debugging this problem would be to use the MTCxx test modes.

During normal data taking, data from the serial receivers is written into a set of input FIFO's, one for each serial receiver. Data is subsequently read out from these FIFO's and goes two places: the MTFB where card level trigger logic is performed and Dual Port Memory (DPM) where it is stored for readout on an L2 Accept.

In MTCxx test mode, one turn's worth of data is loaded into the DPM, the output of the FIFOs is turned off and the data is read from the DPM and subsequently sent to the MTFB where the card level trigger logic is performed. The crossing numbers associated with Input Ready and Data Ready have been previously saved in data registers in order to check that these signals occur at the proper times. These crossings numbers are now used to generate Input Ready and Data Ready signals for the MTCM at the proper times. Data is read out of the DPM and sent to the MTFB at the appropriate time (i.e. when Input Ready is sent), after which the timing is the same as for normal data taking

The MTCxx test mode can be run in "one turn" or continuous modes. In "one turn" mode data is read out from the DPM and sent to the MTFB for one turn only. After that, 0's are sent to the MTFB. In continuous mode, a turn's worth of data is continually sent to the MTFB. The control bits for these test modes are in the MTCxx Status/Control Word, described earlier.

4. Timing Signals

There are several signals that are used to synchronize the MTCxx to the rest of the Muon Trigger Crate. These signals originate in the Muon Trigger Crate at the MTCM, which creates the signals from signals that originate at the Trigger Framework.

- ⇒ RF_Clock - 53 MHz Clock that is the basic accelerator RF signal.
- ⇒ First_Crossing - This signal indicates the beginning of a turn. The First_Crossing signal is associated with the sixth bunch crossing before the first bunch crossing

that contains real beam. This signal resets the BC number (but not the turn number). This signals also causes the internal Turn Number on the MTCM to be reset for the first RESET signal received after a Master_Reset signal.

⇒ SYNC_GAP - Signal to indicate an accelerator gap during which L1 Accepts are not permitted. These gaps are used to allow the input FIFOs to empty (and thus become synchronized later when they are all not empty). Note that not all accelerator gaps will cause a GAP signal, some may be used for Cosmic Level 1 triggering. During the Synch Gap, all front ends will send idle signals (K28.5 as defined in the Fiber Channel specification) over their serial outputs to the MTCxxs which will maintain word synchronization at the MTCxx.

⇒ Synch_L05 - This signal indicates the first RF clock period in a bunch crossing, it is used by the MTCxx to synchronize when to present decision data to the MTCM. For example, if the MTCxx is being used as an MTC05, it may send data during RF clocks 0 and 1, while the MTC10 might send 12 bits of decision data during clocks 2 and 3 and a second set of 12 bits during clocks 4, 5 and 6.

⇒ Send_Data – This signal is used to tell the MTCxx to start putting the Card Decision Data Bits on the appropriate backplane pins. This signal is generated by the MTCM from the DATA_READY signal.

⇒ Master_Reset - This signal is created by the MTCM from the Initialize signal sent by the Trigger Framework. This signal will reset all FIFOs and memories on the MTCM and reset the internal turns counter on the first First_Crossing signal received after the Master_Reset signal.

5. Flash Memory Operation

The MTCxx contains 1Mbyte of Flash Memory that is used to hold the programs for the FPGAs that are located on the Flavor Board. The memory is mapped to locations 2000000_h - $21FFFFE_h$, as shown in the memory map in Appendix G. Because the Flash Memory operates in 64K sectors (the entire memory has 32 sectors) that must be erased all at once, we have (arbitrarily) partitioned the memory into 8 FPGAs, which should be EPF10K70s or smaller. Larger devices can be accommodated by using 3 or more sectors instead of 2 for the device, the critical points are that each FPGA start at the beginning of a 64K sector and that the data ordered as shown in Appendix G. The first byte is a Program ID, the second byte is a mask to show which of the possible 8 devices on a flavor card the data will be aimed at , the third byte is a checksum for the data and the fourth byte on contains the data for the FPGA.

The flash memory can be read over the VME bus as any other memory location but must be programmed using a 128K transfer memory on the MTCxx. This is because of the unique programming methods that must be used for the flash memory (AMD AM29F080B), before any byte is written the sector that is to be written must be erased and then after writing each byte the user must wait until the flash has completed the internal memory operation. Both of these processes can be fairly lengthy, the erase cycle per sector is typically 1 second and can be as long as 8 seconds, while the writes take typically 7 μsec per byte and can take as long as 300 μsec per byte. The write operation for the user has been simplified on the MTCxx by the use of a 128 Kbyte transfer memory that the user can write into when it is necessary to reprogram any of the FPGAs. Before writing the desired program into the transfer memory the user should first examine the MTCxx Status/Command register to ensure that there are no flash memory operations in progress, then after writing the program into the transfer memory the user just sets up the number of the FPGA to be transferred and the “Transfer Data to Flash” bits in the MTCxx Status/Control Register and the logic in the MTCxx will transfer the contents of the transfer memory to the appropriate location in flash memory. The flash memory busy flag in the MTCxx Status/Control register will be high until the transfer is complete and the flash transfer error bit will go high if there is a problem with the transfer. The user should monitor the MTCxx status control register until the flash busy bit goes low to make sure that no errors are encountered while programming.

6. Dual Port Memory Organization

The Dual Port Memory (DPM) on the MTCxx stores all the input data from the receivers as well as the results from the Flavor Board, the Local BC Count and the Status Word. This memory is 32 bits wide and is located at $2x040000_h$ to $2x047ffc_h$, there are 66 words associated with each bunch crossing, these words, and their location, are shown in Appendix F.

7. Front Panel Indicators, Switches and Monitors

7.1 Front Panel Indicators

⇒ Power indicators for +5V, -5V, +3.3V (Green)

⇒ Lock Okay Error (Red)

⇒ Parity Error (Red)

⇒ Input FIFO Full Error (Red)

⇒ Buffer FIFO Full Error (Red)

⇒ Memory Error (Red)

⇒ Crossing Error Mismatch (Red)

⇒ All Inputs Locked (Green)

⇒ Trigger OR (Yellow)

7.2 Front Panel Switches

There are no Front Panel Switches

7.3 Front Panel Monitor Points

There are NIM compatible front panel monitors to indicate

⇒ Board Input Ready Signal

⇒ Board Data Ready Signal

8. JTAG and Programming Connectors

There are 5 JTAG chains on the MTCxx, one of which is used for JTAG testing only and 4 which are used for both programming FPGAs and JTAG testing. I am using the term FPGA here to indicate both CPLDs, that are typically non-volatile, and FPGAs which are typically volatile and need to be reprogrammed on every power cycle. The devices that are programmed fall into 2 groups, ones that are directly programmed (CPLDs) and EPROMs that are used to program FPGAs after a power cycle.

8.1 Programming Connectors

8.1.1 J7 (External Programming A)

J7 programs a FPGA EPROM, U74, which programs the Data Multiplexer, the FPGA Configuration, the Receive FIFO Control and Pointer Control FPGAs. The signals on this connector are also available at J12 on pins 31 to 34 to allow programming this chain without removing the board from the card cage.

8.1.2 J5 (External Programming B)

J5 programs the EPROMs that program the Input Buffer FPGAs. There are 2 of these EPROMS, U3 and U4 which are both EPC2s and each one programs 8 of the Input Buffers. The signals on this connector are also available at J12 on pins 37 to 40 to allow programming this chain without removing the board from the card cage.

8.1.3 J4 (VME Interface)

J4 programs the VME Interface circuit on the MTCxx, U70, which is an EPM3128 CPLD.

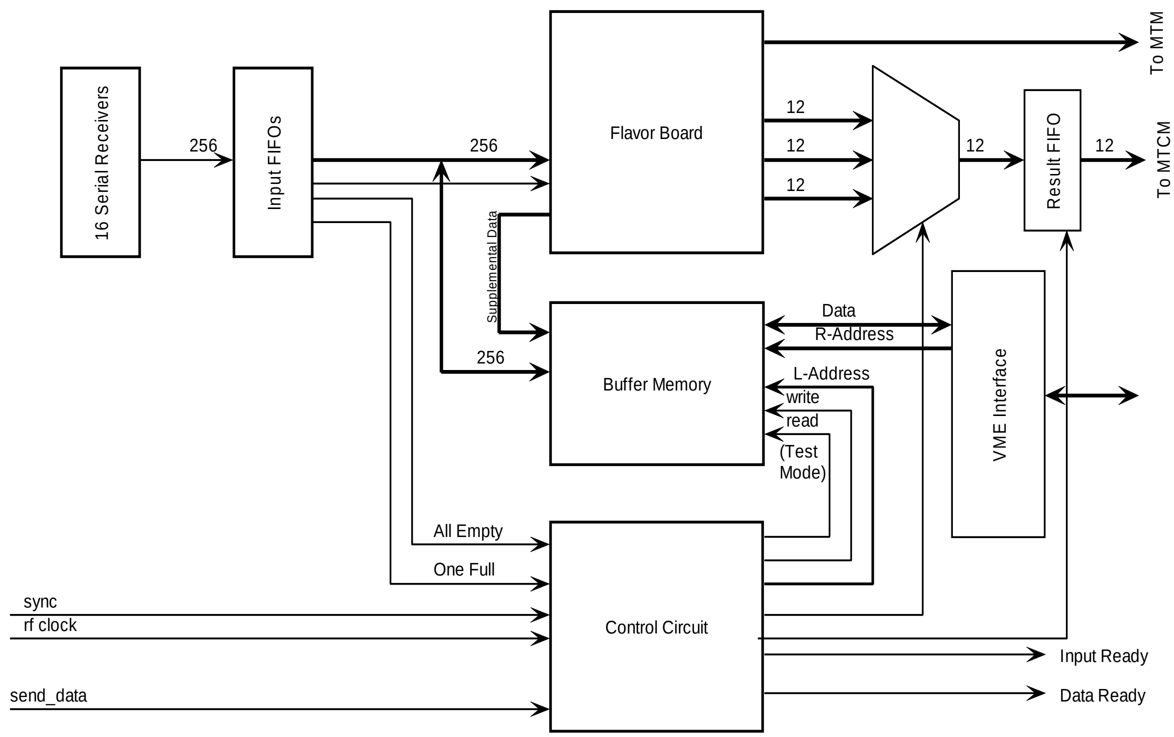
8.1.4 J34 (Flavor Board Control Circuit)

J34 programs the CPLD on the flavor board which is used to control the programming of the the FPGAs on the flavor board.

8.2 Testing Connector

The main JTAG chain for testing in input through unused pins on the J1 VME connector. The JTAG test stand is then used to connect this chain to a JTAG tester, the programming connectors can also be connected to the JTAG tester for complete coverage of the board. This chain runs through all the JTAG compatible devices on the board as well as all the daughter cards on the board (the Receivers and Flavor Board) which must be jumpered out (TDO connected to TDI) of they are not present in order to use the test chain).

Appendix A - Block Diagram of MTCxx



Appendix B - J1 Connections

Pin	Label	Pin	Label	Pin	Label	Pin	Label	Pin	Label
Z1		A1	D00	B1	SSBY*	C1	D08	D1	VPC
Z2	GND	A2	D01	B2	BCLR*	C2	D09	D2	GND
Z3		A3	D02	B3	ACF*	C3	D10	D3	
Z4	GND	A4	D03	B4		C4	D11	D4	
Z5		A5	D04	B5		C5	D12	D5	
Z6	GND	A6	D05	B6		C6	D13	D6	
Z7		A7	D06	B7		C7	D14	D7	
Z8	GND	A8	D07	B8		C8	D15	D8	
Z9		A9	GND	B9		C9	GND	D9	GAP*
Z10	GND	A10		B10		C10	SYSF*	D10	GA0*
Z11		A11	GND	B11		C11	BERR*	D11	GA1*
Z12	GND	A12	DS1*	B12		C12	RST*	D12	+3.3V
Z13		A13	DS0*	B13		C13	LWRD*	D13	GA2*
Z14	GND	A14	WR*	B14		C14	AM5	D14	+3.3V
Z15		A15	GND	B15		C15	A23	D15	GA3*
Z16	GND	A16	DTCK*	B16	AM0	C16	A22	D16	+3.3V
Z17		A17	GND	B17	AM1	C17	A21	D17	GA4*
Z18	GND	A18	AS*	B18	AM2	C18	A20	D18	+3.3V
Z19		A19	GND	B19	AM3	C19	A19	D19	
Z20	GND	A20		B20	GND	C20	A18	D20	+3.3V
Z21		A21		B21		C21	A17	D21	
Z22	GND	A22		B22		C22	A16	D22	+3.3V
Z23		A23	AM4	B23		C23	A15	D23	
Z24	GND	A24	A07	B24	TRST*	C24	A14	D24	+3.3V
Z25		A25	A06	B25	TDI	C25	A13	D25	
Z26	GND	A26	A05	B26	TDO	C26	A12	D26	+3.3V
Z27		A27	A04	B27	TMS	C27	A11	D27	
Z28	GND	A28	A03	B28	TCK	C28	A10	D28	+3.3V
Z29		A29	A02	B29	IRQ2*	C29	A09	D29	
Z30	GND	A30	A01	B30	IRQ1*	C30	A08	D30	+3.3V
Z31		A31	-12V	B31	+5V	C31	+12V	D31	GND
Z32	GND	A32	+5V	B32	+5V	C32	+5V	D32	VPC

Appendix C - J2 Connections

Pin	Label	Pin	Label	Pin	Label
A1	RF_CLOCK+	B2	+5V	C1	RF_CLOCK-
A2	GND	B2	GND	C2	GND
A3	CDD00	B3		C3	+3.3V
A4	CDD01	B4	A24	C4	+3.3V
A5	CDD02	B5	A25	C5	+3.3V
A6	CDD03	B6	A26	C6	+3.3V
A7	CDD04	B7	A27	C7	GND
A8	CDD05	B8	A28	C8	GND
A9	CDD06	B9	A29	C9	GND
A10	CDD07	B10	A30	C10	GND
A11	CDD08	B11	A31	C11	+5V
A12	CDD09	B12	GND	C12	+5V
A13	CDD10	B13	+5V	C13	+5V
A14	CDD11	B14	D16	C14	GND
A15	GND	B15	D17	C15	GND
A16	+5V	B16	D18	C16	GND
A17	+5V	B17	D19	C17	GND
A18	+5V	B18	D20	C18	GND
A19	SEND_DATA	B19	D21	C19	BC_COUNT0
A20	SYNCH_L05	B20	D22	C20	BC_COUNT1
A21	INPUT_READY	B21	D23	C21	BC_COUNT2
A22	L1_BUSY*	B22	GND	C22	BC_COUNT3
A23	L2_BUSY*	B23	D24	C23	BC_COUNT4
A24	MTCxx_ERROR	B24	D25	C24	BC_COUNT5
A25	RESET_COUNTERS	B25	D26	C25	BC_COUNT6
A26	MASTER_RESET	B26	D27	C26	BC_COUNT7
A27	L1_ACCEPT	B27	D28	C27	BC_CLOCK
A28	L1_REJECT	B28	D29	C28	1^{ST}_CROSS
A29	L2_ACCEPT	B29	D30	C29	GAP
A30	L2_REJECT	B30	D31	C30	SYNC_GAP
A31	GND	B31	GND	C31	GND
A32	DATA_READY	B32	+5V	C32	+5V

Appendix D - Flavor Board Connections

(This connector consists of 6 separate connectors that have been combined into a single part to ease the PC layout requirements)

MTFB Connector P1

Pin	Label	Pin	Label	Pin	Label	Pin	Label
A1	+3.3V	B1	+3.3V	C1	+3.3V	D1	+3.3V
A2	GND	B1	GND	C2	GND	D2	GND
A3	IN1-0	B3	IN2-0	C3	IN3-0	D3	IN4-0
A4	IN1-1	B4	IN2-1	C4	IN3-1	D4	IN4-1
A5	IN1-2	B5	IN2-2	C5	IN3-2	D5	IN4-2
A6	IN1-3	B6	IN2-3	C6	IN3-3	D6	IN4-3
A7	GND	B7	GND	C7	GND	D7	GND
A8	IN1-4	B8	IN2-4	C8	IN3-4	D8	IN4-4
A9	IN1-5	B9	IN2-5	C9	IN3-5	D9	IN4-5
A10	IN1-6	B10	IN2-6	C10	IN3-6	D10	IN4-6
A11	IN1-7	B11	IN2-7	C11	IN3-7	D11	IN4-7
A12	GND	B12	GND	C12	GND	D12	GND
A13	IN1-8	B13	IN2-8	C13	IN3-8	D13	IN4-8
A14	IN1-9	B14	IN2-9	C14	IN3-9	D14	IN4-9
A15	IN1-10	B15	IN2-10	C15	IN3-10	D15	IN4-10
A16	IN1-11	B16	IN2-11	C16	IN3-11	D16	IN4-11
A17	GND	B17	GND	C17	GND	D17	GND
A18	IN1-12	B18	IN2-12	C18	IN3-12	D18	IN4-12
A19	IN1-13	B19	IN2-13	C19	IN3-13	D19	IN4-13
A20	IN1-14	B20	IN2-14	C20	IN3-14	D20	IN4-14
A21	IN1-15	B21	IN2-15	C21	IN3-15	D21	IN4-15
A22	GND	B22	GND	C22	GND	D22	GND
A23	+2.5V	B23	+2.5V	C23	LADDR0	D23	LADDR1
A24	+3.3V	B24	+3.3V	C24	+3.3V	D24	+3.3V
A25	RF-CLK1	B25	GND	C25	INT_BC_CK1	D25	GND

MTFB Connector P2

Pin	Label	Pin	Label	Pin	Label	Pin	Label
A1	+3.3V	B1	+3.3V	C1	+3.3V	D1	+3.3V
A2	GND	B1	GND	C2	GND	D2	GND
A3	IN5-0	B3	IN6-0	C3	IN7-0	D3	IN8-0
A4	IN5-1	B4	IN6-1	C4	IN7-1	D4	IN8-1
A5	IN5-2	B5	IN6-2	C5	IN7-2	D5	IN8-2
A6	IN5-3	B6	IN6-3	C6	IN7-3	D6	IN8-3
A7	GND	B7	GND	C7	GND	D7	GND
A8	IN5-4	B8	IN6-4	C8	IN7-4	D8	IN8-4
A9	IN5-5	B9	IN6-5	C9	IN7-5	D9	IN8-5
A10	IN5-6	B10	IN6-6	C10	IN7-6	D10	IN8-6
A11	IN5-7	B11	IN6-7	C11	IN7-7	D11	IN8-7
A12	GND	B12	GND	C12	GND	D12	GND
A13	IN5-8	B13	IN6-8	C13	IN7-8	D13	IN8-8
A14	IN5-9	B14	IN6-9	C14	IN7-9	D14	IN8-9
A15	IN5-10	B15	IN6-10	C15	IN7-10	D15	IN8-10
A16	IN5-11	B16	IN6-11	C16	IN7-11	D16	IN8-11
A17	GND	B17	GND	C17	GND	D17	GND
A18	IN5-12	B18	IN6-12	C18	IN7-12	D18	IN8-12
A19	IN5-13	B19	IN6-13	C19	IN7-13	D19	IN8-13
A20	IN5-14	B20	IN6-14	C20	IN7-14	D20	IN8-14
A21	IN5-15	B21	IN6-15	C21	IN7-15	D21	IN8-15
A22	GND	B22	GND	C22	GND	D22	GND
A23	+2.5V	B23	+2.5V	C23	LADDR2	D23	MT0
A24	+3.3V	B24	+3.3V	C24	+3.3V	D24	+3.3V
A25	RF-CLK2	B25	GND	C25	INT_BC_CK2	D25	GND

MTFB Connector P3

Pin	Label	Pin	Label	Pin	Label	Pin	Label
A1	+3.3V	B1	+3.3V	C1	+3.3V	D1	+3.3V
A2	GND	B1	GND	C2	GND	D2	GND
A3	IN9-0	B3	IN10-0	C3	IN11-0	D3	IN12-0
A4	IN9-1	B4	IN10-1	C4	IN11-1	D4	IN12-1
A5	IN9-2	B5	IN10-2	C5	IN11-2	D5	IN12-2
A6	IN9-3	B6	IN10-3	C6	IN11-3	D6	IN12-3
A7	GND	B7	GND	C7	GND	D7	GND
A8	IN9-4	B8	IN10-4	C8	IN11-4	D8	IN12-4
A9	IN9-5	B9	IN10-5	C9	IN11-5	D9	IN12-5
A10	IN9-6	B10	IN10-6	C10	IN11-6	D10	IN12-6
A11	IN9-7	B11	IN10-7	C11	IN11-7	D11	IN12-7
A12	GND	B12	GND	C12	GND	D12	GND
A13	IN9-8	B13	IN10-8	C13	IN11-8	D13	IN12-8
A14	IN9-9	B14	IN10-9	C14	IN11-9	D14	IN12-9
A15	IN9-10	B15	IN10-10	C15	IN11-10	D15	IN12-10
A16	IN9-11	B16	IN10-11	C16	IN11-11	D16	IN12-11
A17	GND	B17	GND	C17	GND	D17	GND
A18	IN9-12	B18	IN10-12	C18	IN11-12	D18	IN12-12
A19	IN9-13	B19	IN10-13	C19	IN11-13	D19	IN12-13
A20	IN9-14	B20	IN10-14	C20	IN11-14	D20	IN12-14
A21	IN9-15	B21	IN10-15	C21	IN11-15	D21	IN12-15
A22	GND	B22	GND	C22	GND	D22	GND
A23	+2.5V	B23	+2.5V	C23		D23	
A24	+3.3V	B24	+3.3V	C24	+3.3V	D24	+3.3V
A25	RF-CLK3	B25	GND	C25	INT_BC_CK3	D25	GND

MTFB Connector P4

Pin	Label	Pin	Label	Pin	Label	Pin	Label
A1	+3.3V	B1	+3.3V	C1	+3.3V	D1	+3.3V
A2	GND	B1	GND	C2	GND	D2	GND
A3	IN13-0	B3	IN14-0	C3	IN15-0	D3	IN16-0
A4	IN13-1	B4	IN14-1	C4	IN15-1	D4	IN16-1
A5	IN13-2	B5	IN14-2	C5	IN15-2	D5	IN16-2
A6	IN13-3	B6	IN14-3	C6	IN15-3	D6	IN16-3
A7	GND	B7	GND	C7	GND	D7	GND
A8	IN13-4	B8	IN14-4	C8	IN15-4	D8	IN16-4
A9	IN13-5	B9	IN14-5	C9	IN15-5	D9	IN16-5
A10	IN13-6	B10	IN14-6	C10	IN15-6	D10	IN16-6
A11	IN13-7	B11	IN14-7	C11	IN15-7	D11	IN16-7
A12	GND	B12	GND	C12	GND	D12	GND
A13	IN13-8	B13	IN14-8	C13	IN15-8	D13	IN16-8
A14	IN13-9	B14	IN14-9	C14	IN15-9	D14	IN16-9
A15	IN13-10	B15	IN14-10	C15	IN15-10	D15	IN16-10
A16	IN13-11	B16	IN14-11	C16	IN15-11	D16	IN16-11
A17	GND	B17	GND	C17	GND	D17	GND
A18	IN13-12	B18	IN14-12	C18	IN15-12	D18	IN16-12
A19	IN13-13	B19	IN14-13	C19	IN15-13	D19	IN16-13
A20	IN13-14	B20	IN14-14	C20	IN15-14	D20	IN16-14
A21	IN13-15	B21	IN14-15	C21	IN15-15	D21	IN16-15
A22	GND	B22	GND	C22	GND	D22	GND
A23	+2.5V	B23	+2.5V	C23		D23	
A24	+3.3V	B24	+3.3V	C24	+3.3V	D24	+3.3V
A25	RF-CLK4	B25	GND	C25	INT_BC_CK4	D25	GND

MTFB Connector P5

Pin	Label	Pin	Label	Pin	Label	Pin	Label
A1	+5V	B1	+5V	C1	+5V	D1	+5V
A2	GND	B1	GND	C2	GND	D2	GND
A3	OTD1	B3	OTD10	C3	OTD19	D3	OTD28
A4	OTD2	B4	OTD11	C4	OTD20	D4	OTD29
A5	OTD3	B5	OTD12	C5	OTD21	D5	OTD30
A6	OTD4	B6	OTD13	C6	OTD22	D6	OTD31
A7	OTD5	B7	OTD14	C7	OTD23	D7	OTD32
A8	OTD6	B8	OTD15	C8	OTD24	D8	OTD33
A9	OTD7	B9	OTD16	C9	OTD25	D9	OTD34
A10	OTD8	B10	OTD17	C10	OTD26	D10	OTD35
A11	OTD9	B11	OTD18	C11	OTD27	D11	OTD36
A12	MT1	B12	MT2	C12	MT3	D12	MT4
A13	GND	B13	GND	C13	GND	D13	GND
A14	SD1	B14	SD5	C14	SD9	D14	SD13
A15	SD2	B15	SD6	C15	SD10	D15	SD14
A16	SD3	B16	SD7	C16	SD11	D16	SD15
A17	SD4	B17	SD8	C17	SD12	D17	SD16
A18	-5V	B18	-5V	C18	-5V	D18	-5V
A19	GND	B19	LOC_SGAP	C19	GND	D19	LOC_GAP
A20	RF-CLOCK	B20	GND	C20	BC-CLOCK	D20	GND
A21	PROG-TDI	B21	PROG-TMS	C21	PROG-TCK	D21	PROG-TDO
A22	INIT	B22		C22	TEST_READ	D22	SYNCH-GAP
A23	WR_D_EN*	B23	DAV	C23	TOR	D23	START-PROC
A24	GND	B24	GND	C24	GND	D24	GND
A25	NCONFIG	B25	NSTATUS	C25	DCLOCK	D25	FB_IN_RDY
A26	DATA0	B26	CONF_DONE	C26	LOCAL_AS	D26	UFB-NONE-MT
A27	TDI	B27	TDO	C27	TCK	D27	TMS
A28	INT_D0	B28	INT_D1	C28	INT_D2	D28	INT_D3
A29	INT_D4	B29	INT_D5	C29	INT_D6	D29	INT_D7
A30	REG_READ	B30	REG_WRITE	C30	LOCAL_WR	D30	LOCAL_DS0
A31	MT5	B31	MT6	C31	MT7	D31	UFB-FULL-RCVR
A32	GND	B32	INT_A1	C32	INT_A2	D32	INT_A3
A33	INT_A4	B33	INT_A5	C33	INT_A6	D33	INT_A7
A34	GND	B34	GND	C34	GND	D34	GND
A35	SEL0	B35	SEL1	C35	SEL2	D35	TRST

MTFB Connector P6

Pin	Label	Pin	Label	Pin	Label	Pin	Label
A1	TERM_A0+	B1	TERM_A0-	C1	TERM_B0+	D1	TERM_B0-
A2	TERM_A1+	B1	TERM_A1-	C2	TERM_B1+	D2	TERM_B1-
A3	TERM_A2+	B3	TERM_A2-	C3	TERM_B2+	D3	TERM_B2-
A4	TERM_A3+	B4	TERM_A3-	C4	TERM_B3+	D4	TERM_B3-
A5	TERM_A4+	B5	TERM_A4-	C5	TERM_B4+	D5	TERM_B4-
A6	TERM_A5+	B6	TERM_A5-	C6	TERM_B5+	D6	TERM_B5-
A7	TERM_A6+	B7	TERM_A6-	C7	TERM_B6+	D7	TERM_B6-
A8	TERM_A7+	B8	TERM_A7-	C8	TERM_B7+	D8	TERM_B7-
A9	TERM_A8+	B9	TERM_A8-	C9	TERM_B8+	D9	TERM_B8-
A10	TERM_A9+	B10	TERM_A9-	C10	TERM_B9+	D10	TERM_B9-
A11	TERM_A10+	B11	TERM_A10-	C11	TERM_B10+	D11	TERM_B10-
A12	TERM_A11+	B12	TERM_A11-	C12	TERM_B11+	D12	TERM_B11-
A13	TERM_A12+	B13	TERM_A12-	C13	TERM_B12+	D13	TERM_B12-
A14	TERM_A13+	B14	TERM_A13-	C14	TERM_B13+	D14	TERM_B13-
A15	TERM_A14+	B15	TERM_A14-	C15	TERM_B14+	D15	TERM_B14-
A16	TERM_A15+	B16	TERM_AA15-	C16	TERM_B15+	D16	TERM_BA15-
A17	GAP_A+	B17	GAP_A-	C17	GAP_B	D17	GAP_B
A18	GROUND1	B18	GROUND3	C18	GROUND5	D18	GROUND7
A19	STROBE_A+	B19	STROBE_A-	C19	STROBE_B	D19	STROBE_B
A20	GROUND2	B20	GROUND4	C20	GROUND6	D20	GROUND8

MTFB Connector P7

Pin	Label	Pin	Label	Pin	Label	Pin	Label
A1	TEST1	B1	TEST15	C1	INT_D8	D1	INT_D28
A2	TEST2	B1	TEST16	C2	INT_D9	D2	INT_D29
A3	TEST3	B3	TEST17	C3	INT_D10	D3	INT_D30
A4	TEST4	B4	TEST18	C4	INT_D11	D4	INT_D31
A5	TEST5	B5	TEST19	C5	INT_D12	D5	INT_A8
A6	TEST6	B6	TEST20	C6	INT_D13	D6	INT_A9
A7	TEST7	B7	TEST21	C7	INT_D14	D7	INT_A10
A8	TEST8	B8	TEST22	C8	INT_D15	D8	INT_A11
A9	TEST9	B9	TEST23	C9	INT_D16	D9	INT_A12
A10	TEST10	B10	TEST24	C10	INT_D17	D10	INT_A13
A11	TEST11	B11	TEST25	C11	INT_D18	D11	INT_A14
A12	TEST12	B12	TEST26	C12	INT_D19	D12	INT_A15
A13	TEST13	B13	TEST27	C13	INT_D20	D13	INT_A16
A14	TEST14	B14	TEST28	C14	INT_D21	D14	INT_A17
A15		B15		C15	INT_D22	D15	INT_A18
A16		B16		C16	INT_D23	D16	INT_A19
A17		B17		C17	INT_D24	D17	INT_A20
A18		B18		C18	INT_D25	D18	INT_A21
A19		B19		C19	INT_D26	D19	INT_A22
A20		B20		C20	INT_D27	D20	INT_A23

Appendix E – Front Panel Connectors

J11 Connector on Front Panel (MTM Connector)

Pin	Label	Pin	Label	Pin	Label	Pin	Label
A1	TERM_A0+	A2	TERM_A0-	B1	TERM_B0+	B2	TERM_B0-
A3	TERM_A1+	A4	TERM_A1-	B3	TERM_B1+	B4	TERM_B1-
A5	TERM_A2+	A6	TERM_A2-	B5	TERM_B2+	B6	TERM_B2-
A7	TERM_A3+	A8	TERM_A3-	B7	TERM_B3+	B8	TERM_B3-
A9	TERM_A4+	A10	TERM_A4-	B9	TERM_B4+	B10	TERM_B4-
A11	TERM_A5+	A12	TERM_A5-	B11	TERM_B5+	B12	TERM_B5-
A13	TERM_A6+	A14	TERM_A6-	B13	TERM_B6+	B14	TERM_B6-
A15	TERM_A7+	A16	TERM_A7-	B15	TERM_B7+	B16	TERM_B7-
A17	TERM_A8+	A18	TERM_A8-	B17	TERM_B8+	B18	TERM_B8-
A19	TERM_A9+	A20	TERM_A9-	B19	TERM_B9+	B20	TERM_B9-
A21	TERM_A10+	A22	TERM_A10-	B21	TERM_B10+	B22	TERM_B10-
A23	TERM_A11+	A24	TERM_A11-	B23	TERM_B11+	B24	TERM_B11-
A25	TERM_A12+	A26	TERM_A12-	B25	TERM_B12+	B26	TERM_B12-
A27	TERM_A13+	A28	TERM_A13-	B27	TERM_B13+	B28	TERM_B13-
A29	TERM_A14+	A30	TERM_A14-	B29	TERM_B14+	B30	TERM_B14-
A31	TERM_A15+	A32	TERM_AA15-	B31	TERM_B15+	B32	TERM_BA15-
A33	GAP_A+	A34	GAP_A-	B33	GAP_B	B34	GAP_B
A35	GROUND1	A36	GROUND3	B35	GROUND5	B36	GROUND7
A37	STROBE_A+	A38	STROBE_A-	B37	STROBE_B	B38	STROBE_B
A39	GROUND2	A40	GROUND4	B39	GROUND6	B40	GROUND8

J12 Connector on Front Panel

Pin	Label	Pin	Label
1	TEST1	2	TEST15
3	TEST2	4	TEST16
5	TEST3	6	TEST17
7	TEST4	8	TEST18
9	TEST5	10	TEST19
11	TEST6	12	TEST20
13	TEST7	14	TEST21
15	TEST8	16	TEST22
17	TEST9	18	TEST23
19	TEST10	20	TEST24
21	TEST11	22	TEST25
23	TEST12	24	TEST26
25	TEST13	26	TEST27
27	TEST14	28	TEST28
29	GND	30	GND
31	TMS-A	32	TCK-A
33	TDI-A	34	TDO-A
35	GND	36	GND
37	TMS-B	38	TCK-B
39	TDI-B	40	TDO-B

Note:

TMS-A, TCK-A, TDI-A, and TDO-A are used to program U70, U73 and U74

TMS-B, TCK-B, TDI-B, and TDO-B are used to program U3 and U4

Appendix F - MTCxx Memory Map

MTCxx Memory Locations	
Relative Address	Description
000000	MTCxx Serial Number
000002	Flavor Board type and Serial Number
000004	Unassigned Register
000006	MTCxx Serial Input Mask Register – Receivers 1 to 16
000008	MTCxx Serial Input Trigger Mask Register – Receivers 1 to 16
00000A	Lock Error Mask - Receivers 1 to 16
00000C	Parity Error Mask - Receivers 1 to 16
00000E	Multiplexer Control
000010	Input Ready BC Number
000012	Data Ready BC Number
000014	Unassigned Register
000016	Pending Transfer FIFO (Read Only)
000018	MTCxx Mask Control Register, Bit 0 high masks board
00001A	Auxiliary Control (bit 0 high permanently enables Data ready, bit 1 high disables receiver reset on init)
00001C	End Count Register (last BC that contains data)
00001E	First Crossing Register (sets first crossing for local BC counter)
000020	MTCxx Card Flash Memory Status/Control Register
000022	MTCxx Card Test Status/Control Register
000024	Temporary Read L1 Pending Direct (Test Only!)
000026	Buffer Transfer FIFO (Write to this register indicates buffer may be transferred to empty buffer list)
000028	Programmed Init (write 1 to bit 0) / bit 1 indicates length error detected
00002a	Results Fine Delay Adjust (bits 0-2 adjust delay of result data
00002c	Flavor Board Status and Done Flags (Status bits 15..8, Done bits 7..0)
00002e	Flavor Board Status and Done Flags Mask (low masks off bit)
000030 – 000072	Reserved Register Area
000074 – 00007e	Unassigned Register Area
000080	Buffer FIFO Status/Error Register
000082	Unassigned

MTCxx Memory Locations	
Relative Address	Description
000084	MTCxx Card General Purpose Error Register
000086	MTCxx Card Latched General Purpose Error Register
000088	MTCxx Serial Lock Okay Register (Write high for reset) – Receivers 1 to 16
00008A	MTCxx Latched Serial Lock Error Register - Receivers 1 to 16
00008C	Receive FIFO Full – Registers 1 to 16
00008E	Receive FIFO Full – Registers 17 to 20
000090	MTCxx Serial Parity Error Register - Receivers 1 to 16
000092	MTCxx Latched Serial Parity Error Register- Receivers 1 to 16
000094	Unassigned
000096	None Empty delay register (3 bits)), bit 15 is used to indicate absence of serial receivers on UFB (i.e. set high if not using receivers on UFB)
000098 – 00009E	Unassigned Register Area
0000A0	MTCxx Serial Input Mask Register – Receivers 17 to 20
0000A2	MTCxx Serial Input Trigger Mask Register – Receivers 17 to 20
0000A4	Lock Error Mask - Receivers 17 to 20
0000A6	Parity Error Mask - Receivers 17 to 20
0000A8 – 0000AE	
0000B0	MTCxx Serial Lock Okay Register (Write high for reset)–Receivers 17 to 20
0000B2	MTCxx Latched Serial Lock Error Register - Receivers 17 to 20
0000B4	MTCxx Input Full Error Register - Receivers 17 to 20
0000B6	MTCxx Latched Input Full Error Register - Receivers 17 to 20
0000B8	MTCxx Serial Parity Error Register - Receivers 17 to 20
0000BA	MTCxx Latched Serial Parity Error Register- Receivers 17 to 20
0000BC – 0000FE	Unassigned Register Area
040000 – 05FFFC	Dual Port Ram (for 20 SLDBs on MTCxx)
060000 – 0FFFFE	Undefined
100000 – 13FFFE	Transfer Memory for FPGA Programs
200000 – 5FFFFE	Program Data for Flavor Board FPGAs

Appendix G – DPM Bunch Crossing Data

DPM Memory Locations	
Relative Address	Description
000	Receiver 1 Word 0 (Low 16 bits), Receiver 0 Word 0 (High 16 bits)
004	Receiver 3 Word 0 (Low 16 bits), Receiver 2 Word 0 (High 16 bits)
008	Receiver 5 Word 0 (Low 16 bits), Receiver 4 Word 0 (High 16 bits)
00c	Receiver 7 Word 0 (Low 16 bits), Receiver 6 Word 0 (High 16 bits)
010	Receiver 9 Word 0 (Low 16 bits), Receiver 8 Word 0 (High 16 bits)
014	Receiver 11 Word 0 (Low 16 bits), Receiver 10 Word 0 (High 16 bits)
018	Receiver 13 Word 0 (Low 16 bits), Receiver 12 Word 0 (High 16 bits)
01c	Receiver 15 Word 0 (Low 16 bits), Receiver 14 Word 0 (High 16 bits)
020	Bits 31-24 floating, bits 23-16 BC Counter, bits 15-0 Status
024	Bits 31-16 floating, bits (15-12) are zero, bits (11-0) are OTD (12-1)
028	Receiver 17 Word 0 (Low 16 bits), Receiver 16 Word 0 (High 16 bits)
02c	Receiver 19 Word 0 (Low 16 bits), Receiver 18 Word 0 (High 16 bits)
040	Receiver 1 Word 1 (Low 16 bits), Receiver 0 Word 1 (High 16 bits)
044	Receiver 3 Word 1 (Low 16 bits), Receiver 2 Word 1 (High 16 bits)
048	Receiver 5 Word 1 (Low 16 bits), Receiver 4 Word 1 (High 16 bits)
04c	Receiver 7 Word 1 (Low 16 bits), Receiver 6 Word 1 (High 16 bits)
050	Receiver 9 Word 1 (Low 16 bits), Receiver 8 Word 1 (High 16 bits)
054	Receiver 11 Word 1 (Low 16 bits), Receiver 10 Word 1 (High 16 bits)
058	Receiver 13 Word 1 (Low 16 bits), Receiver 12 Word 1 (High 16 bits)
05c	Receiver 15 Word 1 (Low 16 bits), Receiver 14 Word 1 (High 16 bits)
060	Bits 31-24 floating, bits 23-16 BC Counter, bits 15-0 Status (repeated)
064	Bits 31-16 floating, bits (15-12) are zero, bits (11-0) are OTD (24-13)
068	Receiver 17 Word 1 (Low 16 bits), Receiver 16 Word 1 (High 16 bits)
06c	Receiver 19 Word 1 (Low 16 bits), Receiver 18 Word 1 (High 16 bits)
080	Receiver 1 Word 2 (Low 16 bits), Receiver 0 Word 2 (High 16 bits)
084	Receiver 3 Word 2 (Low 16 bits), Receiver 2 Word 2 (High 16 bits)
088	Receiver 5 Word 2 (Low 16 bits), Receiver 4 Word 2 (High 16 bits)
08c	Receiver 7 Word 2 (Low 16 bits), Receiver 6 Word 2 (High 16 bits)

DPM Memory Locations	
Relative Address	Description
090	Receiver 9 Word 2 (Low 16 bits), Receiver 8 Word 2 (High 16 bits)
094	Receiver 11 Word 2 (Low 16 bits), Receiver 10 Word 2 (High 16 bits)
098	Receiver 13 Word 2 (Low 16 bits), Receiver 12 Word 2 (High 16 bits)
09c	Receiver 15 Word 2 (Low 16 bits), Receiver 14 Word 2 (High 16 bits)
0a0	Bits 31-24 floating, bits 23-16 BC Counter, bits 15-0 Status (repeated)
0a4	Bits 31-16 floating, bits (15-12) are zero, bits (11-0) are OTD (36-25)
0a8	Receiver 17 Word 2 (Low 16 bits), Receiver 16 Word 2 (High 16 bits)
0ac	Receiver 19 Word 2 (Low 16 bits), Receiver 18 Word 2 (High 16 bits)
0c0	Receiver 1 Word 3 (Low 16 bits), Receiver 0 Word 3 (High 16 bits)
0c4	Receiver 3 Word 3 (Low 16 bits), Receiver 2 Word 3 (High 16 bits)
0c8	Receiver 5 Word 3 (Low 16 bits), Receiver 4 Word 3 (High 16 bits)
0cc	Receiver 7 Word 3 (Low 16 bits), Receiver 6 Word 3 (High 16 bits)
0d0	Receiver 9 Word 3 (Low 16 bits), Receiver 8 Word 3 (High 16 bits)
0d4	Receiver 11 Word 3 (Low 16 bits), Receiver 10 Word 3 (High 16 bits)
0d8	Receiver 13 Word 3 (Low 16 bits), Receiver 12 Word 3 (High 16 bits)
0dc	Receiver 15 Word 3 (Low 16 bits), Receiver 14 Word 3 (High 16 bits)
0e0	Bits 31-24 floating, bits 23-16 BC Counter, bits 15-0 Status (repeated)
0e4	Bits 31-16 floating, bits (15-0) Supplemental Data
0e8	Receiver 17 Word 3 (Low 16 bits), Receiver 16 Word 3 (High 16 bits)
0ec	Receiver 19 Word 3 (Low 16 bits), Receiver 18 Word 3 (High 16 bits)
100	Receiver 1 Word 4 (Low 16 bits), Receiver 0 Word 4 (High 16 bits)
104	Receiver 3 Word 4 (Low 16 bits), Receiver 2 Word 4 (High 16 bits)
108	Receiver 5 Word 4 (Low 16 bits), Receiver 4 Word 4 (High 16 bits)
10c	Receiver 7 Word 4 (Low 16 bits), Receiver 6 Word 4 (High 16 bits)
110	Receiver 9 Word 4 (Low 16 bits), Receiver 8 Word 4 (High 16 bits)
114	Receiver 11 Word 4 (Low 16 bits), Receiver 10 Word 4 (High 16 bits)
118	Receiver 13 Word 4 (Low 16 bits), Receiver 12 Word 4 (High 16 bits)
11c	Receiver 15 Word 4 (Low 16 bits), Receiver 14 Word 4 (High 16 bits)
120	Bits 31-24 floating, bits 23-16 BC Counter, bits 15-0 Status (repeated)

DPM Memory Locations	
Relative Address	Description
128	Receiver 17 Word 4 (Low 16 bits), Receiver 16 Word 4 (High 16 bits)
12c	Receiver 19 Word 4 (Low 16 bits), Receiver 18 Word 4 (High 16 bits)
140	Receiver 1 Word 5 (Low 16 bits), Receiver 0 Word 5 (High 16 bits)
144	Receiver 3 Word 5 (Low 16 bits), Receiver 2 Word 5 (High 16 bits)
148	Receiver 5 Word 5 (Low 16 bits), Receiver 4 Word 5 (High 16 bits)
14c	Receiver 7 Word 5 (Low 16 bits), Receiver 6 Word 5 (High 16 bits)
150	Receiver 9 Word 5 (Low 16 bits), Receiver 8 Word 5 (High 16 bits)
154	Receiver 11 Word 5 (Low 16 bits), Receiver 10 Word 5 (High 16 bits)
158	Receiver 13 Word 5 (Low 16 bits), Receiver 12 Word 5 (High 16 bits)
15c	Receiver 15 Word 5 (Low 16 bits), Receiver 14 Word 5 (High 16 bits)
160	Bits 31-24 floating, bits 23-16 BC Counter, bits 15-0 Status (repeated)
168	Receiver 17 Word 5 (Low 16 bits), Receiver 16 Word 5 (High 16 bits)
16c	Receiver 19 Word 5 (Low 16 bits), Receiver 18 Word 5 (High 16 bits)
180	Receiver 1 Word 6 (Low 16 bits), Receiver 0 Word 6 (High 16 bits)
184	Receiver 3 Word 6 (Low 16 bits), Receiver 2 Word 6 (High 16 bits)
188	Receiver 5 Word 6 (Low 16 bits), Receiver 4 Word 6 (High 16 bits)
18c	Receiver 7 Word 6 (Low 16 bits), Receiver 6 Word 6 (High 16 bits)
190	Receiver 9 Word 6 (Low 16 bits), Receiver 8 Word 6 (High 16 bits)
194	Receiver 11 Word 6 (Low 16 bits), Receiver 10 Word 6 (High 16 bits)
198	Receiver 13 Word 6 (Low 16 bits), Receiver 12 Word 6 (High 16 bits)
19c	Receiver 15 Word 6 (Low 16 bits), Receiver 14 Word 6 (High 16 bits)
1a0	Bits 31-24 floating, bits 23-16 BC Counter, bits 15-0 Status (repeated)
1a8	Receiver 17 Word 6 (Low 16 bits), Receiver 16 Word 6 (High 16 bits)
1ac	Receiver 19 Word 6 (Low 16 bits), Receiver 18 Word 6 (High 16 bits)

Note: All other words in the range 000_h to $1fc_h$ are undefined

The BC Counter and Status Bits are repeated 7 times.