

Overview of the Level 1 Calorimeter-Track Trigger (L1CalTrack)

In order to exploit the Run II discovery potential of the DØ experiment, the Tevatron must run at the highest luminosity possible. While the present luminosity provided by the Tevatron is only modestly higher than in Run I, there is a well-defined upgrade plan to increase the luminosity by a factor of ~ 3 by early 2005 and ~ 7 by early 2007. The increased luminosity will place increased pressure on the DØ trigger system at all levels.

In particular, the present Level 1 (L1) Accept rate of 1500 Hz is already a factor of ~ 3 below the Run II design goal, primarily because of the front-end busy rate of the tracking electronics and limited processing power at Level 2 (both problems are being addressed). In order to keep the most important physics triggers unrescaled as the luminosity increases, additional rejection power must be brought to bear at Level 1. To this end, both the Level 1 Calorimeter Trigger (L1CAL) and Level 1 Central Tracker Trigger (L1CTT) will be upgraded in the coming years.

As the name implies, the L1CalTrack trigger utilizes matches in the ϕ position of tracks from the L1CTT trigger with that of EM and jet objects from the L1CAL trigger. The requirement of correlations in ϕ and/or P_T will reduce combinatoric contributions to the L1 trigger rates of EM and tau triggers. Information from the Central Preshower (CPS) and Forward Preshower (FPS) detectors is also used. Monte Carlo studies show that the improvement in the reported ϕ position from 90° to 11.25° of EM objects can reduce medium P_T electron triggers by a factor of 2-3. Additionally, large factors of rejection (10-70) can be achieved by matching track triggers with calorimeter towers of modest energy. This latter is important in triggering on hadronic tau decays such as in $H \rightarrow \tau\tau$.

The implementation of the L1CalTrack trigger uses the **existing** Level 1 Muon Trigger (L1MU) architecture with small modifications. The L1MU trigger, designed, built, and commissioned by the University of Arizona, matches the ϕ position of tracks from the L1CTT trigger with that of muon objects derived using muon scintillation counter hits. Similarly, the L1CalTrack trigger is designed to match the ϕ position of tracks from the L1CTT trigger with calorimeter objects (EM objects and jets) from the L1CAL trigger. The huge advantage of this implementation is that the L1MU trigger has been successfully running since the start of Run II. Thus issues such as synchronization, buffering, outputs to L2 and L3, electronics testing, monitoring, power supplies, and rack infrastructure have proven, working solutions.

The Level 1 Calorimeter-Track Trigger (L1CalTrack) receives inputs from the L1CAL and L1CTT triggers. It matches jets and EM objects in 32 ϕ wedges with tracks in 80 ϕ wedges (finer granularity is also available) from the L1CTT. EM/jet object E_T and track P_T can also be used in the matching. Data from the L1CAL and L1CTT triggers are transmitted on custom Gbit/s serial links over standard TM LMR-200 coaxial cable. The links are based on the AMCC S2042/S2043 fiber-optic transmitter/receiver pair and use an amplifier/equalizer circuit on the receiver to correct for the attenuation of the signal over the coaxial cable. Both serial link transmitters and receivers are implemented on small daughter boards.

The serial link receivers reside on the Muon Trigger Card (MTCxx), which can be thought of as a motherboard. Each serial link can transmit up to $16 \times 7 = 112$ bits every 132 ns bunch

crossing. Presently, each MTCxx card receives ten serial link inputs from the L1CTT, three inputs from L1CAL (for overlap), and four inputs from the FPS. In fact, the MTCxx can accommodate up to twenty serial link inputs. The MTCxx card, serial links, and trigger daughterboard used in the L1MU trigger system are shown in Figures 1 and 2.

Any trigger logic in the L1CalTrack or L1MU trigger systems is implemented on daughterboards. For the L1MU trigger system, different flavors (number and type of FPGA's) of daughterboards were required. However FPGA technology advanced to the point where only one flavor of daughterboard, called the Universal Flavor Board (UFB), is needed for either the L1MU or L1CalTrack systems. The UFB also resides on the MTCxx cards. The present design of the UFB uses the Altera Stratix EP1S20F780 as the primary FPGA on the board.

The L1CalTrack system is divided into octants for parallelism. Information on the matches in each octant is sent over Gbit/s serial links to a global Trigger Manager (MTM) card where it is summed. The MTM forms 256 global L1CalTrack triggers and sends up to 32 of these to the Trigger Framework for inclusion in the Level 1 physics trigger. The MTM trigger logic is implemented on the UFB described above. Matches in each octant are also sent to the Muon Trigger Crate Managers (MTCM) card, which can send this and other information to the Level 2 (L2) and Level 3 (L3) trigger systems. Data is sent to L2 and L3 using the Cypress Hotlink chipset CY7B23/33 over "Astro cable" from AMP.

The serial link data from the L1CAL and L1CTT systems arrive asynchronously at L1CalTrack and must be synchronized before triggers can be formed for a given event. To accomplish this, all received data are written directly into FIFO's, which are initially empty. When all FIFO's are not empty (i.e., they have all received data for the first bunch crossing), the data are read from the FIFO's and sent to the UFB flavor card for trigger formation. In addition to synchronizing the data for a given event, the MTCxx trigger cards also buffer the input data and trigger decisions pending global Level 1 (L1) and Level 2 (L2) trigger decisions. The input data and trigger decisions are stored in Dual Port Memories (DPM's) and a pointer to the data is written into a FIFO. When an L1 or L2 Accept is received, the pointer is used to read the data for a particular event. The L1MU trigger can also send all of the received input data from the detector front-ends to aid debugging.

While the architecture of the L1CalTrack trigger is similar to that of L1MU, there are some differences. The first is that FIFO's and DPM's are now incorporated inside FPGA's rather than using discrete components. This greatly reduces the number of chips on the L1CalTrack trigger cards. The second is that by exploiting the latest FPGA technology, one UFB (Universal Flavor Board) can be used for all L1MU and L1CalTrack trigger functions. The third difference is that additional inputs were added to the MTCxx trigger cards. In fact these were add to the UFB cards. The L1CalTrack trigger cards are backwards compatible in the sense that they can serve as L1MU trigger cards if needed.



Figure 1. Photograph of the L1MU motherboard, MTC05 daughter card, and serial link receivers.

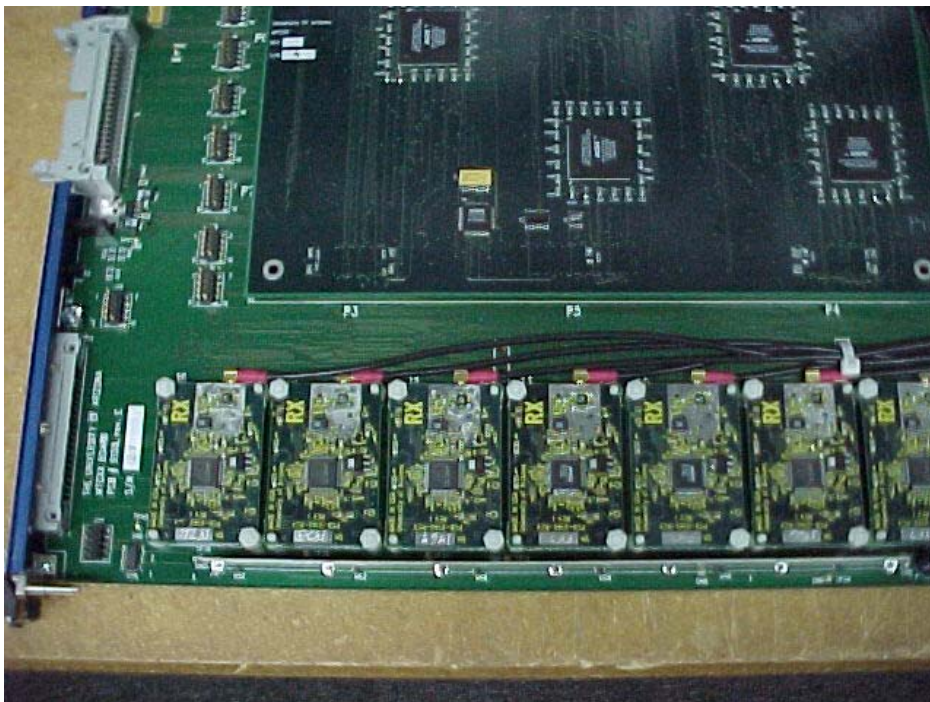


Figure 2. Closeup photograph of the L1MU motherboard, MTC05 daughter card, and serial link receivers.