Forward Calorimeter Baseplane and FC1 Layer Sum Board

D. Tompkins 30 June 2015

Rev A Prototype in Hand



TDR testing shows trace impedance very close to 50 Ohms



Data from 5 traces on each of the 7 routing layers:

	B B B Barrowson										
	Layer	1	2	3	4	5	Ave	SD	100	. ~	
	2	50.0	50.3	49.7	51.4	50.3	50.3	0.64			
	4	50.0	49.2	49.1	50.3	49.5	49.6	0.52			
,	6	49.9	50.9	49.1	50.6	49.9	50.1	0.70			
2	8	49.7	49.6	49.8	48.8	49.4	49.5	0.40			
0	10	49.2	49.9	49.4	48.7	48.3	49.1	0.62	-		
0	12	49.7	49.0	50.2	49.7	49.5	49.6	0.43	The second		
d	14	47.9	48.2	47.5	47.6	4/./	47.8	0.28			
				•							

Some issues:

- Non-plated through holes are flooded over.
- Unused pads removed on all internal layers. This was done to minimize crosstalk and preserve the ground plane as much as possible.
- Current vertical dimension is at maximum for panel size. Any increase would require moving to the next larger panel size

One major problem

• A new mapping scheme is needed to be compatible with the Back End Readout

New Mapping Scheme

• The Back End System requires LTDBO to handle all of the FCAL 1 trigger groups

	FCal1	FCal2	FCal3	Total	
LTDB0					ΔΜΟ
Hi-Z	0	0	0	0	
Lo-Z	192	0	0	192	FC1
Outputs	0	0	0	0	

	FCal1	FCal2	FCal3	Total	
LTDB1					ΔΜΟ
Hi-Z	0	0	64	64	
Lo-Z	0	128	0	128	FC2/3
Outputs	0	64	0	64	

LTDB0 Mapping

LTDB0 JS3 ADC# Pin# D С В ADC# E Α 47 GND GND GND GND GND 46 FC1 GND GND FC1 GND 45 FC1 FC1 GND FC1 FC1 34 44 FC1 FC1 GND FC1 FC1 36 FC1 FC1 43 FC1 GND FC1 42 GND FC1 GND GND FC1 41 GND GND GND 40 GND 39 GND GND GND FC1 GND FC1 GND 38 GND 37 FC1 FC1 GND FC1 FC1 36 35 35 34 37 33 GND FC1 FC1 FC1 FC1 32 FC1 FC1 GND FC1 FC1 31 GND FC1 GND GND FC1 30 FC1 GND GND GND 29 FC1 FC1 GND 33 28 FC1 FC1 GND 38 27 FC1 FC1 GND GND FC1 GND GND 26 GND GND FC1 GND 25 24 GND FC1 FC1 23 GND GND FC1 FC1 40 FC1 GND 22 GND FC1 FC1 21 FC1 FC1 GND GND FC1 32 20 FC1 FC1 GND GND 19 FC1 FC1 GND GND FC1 18 GND GND 17 FC1 GND GND FC1 GND FC1 FC1 GND FC1 FC1 16 31 15 FC1 FC1 GND FC1 FC1 39 14 FC1 FC1 GND FC1 FC1 13 GND FC1 GND GND FC1

	12		GND	GND	FC1	GND	
	11			GND	FC1	FC1	
	10	GND		GND	FC1	FC1	24
	9	FC1	GND	GND	FC1	FC1	21
20	8	FC1	FC1	GND	GND	FC1	
29	7	FC1	FC1	GND		GND	
	6	FC1	FC1	GND			
	5	GND	FC1	GND	GND		
	4	FC1	GND	GND	FC1	GND	
	3	FC1	FC1	GND	FC1	FC1	
	2	GND	FC1	GND	GND	FC1	
	1	GND	GND	GND	GND	GND	
30			JS	2			22
	Pin#	E	D	С	В	Α	
	47	GND	GND	GND	GND	GND	
	46	FC1	GND	GND	FC1	GND	
	45	FC1	FC1	GND	FC1	FC1	
	44	GND	FC1	GND	GND	FC1	
	43		GND	GND		GND	
	42			GND			
	41	GND		GND			22
	40	FC1	GND	GND			25
20	39	FC1	FC1	GND	GND		
20	38	FC1	FC1	GND	FC1	GND	
	37	FC1	FC1	GND	FC1	FC1	
	36						
	35						
	34						25
	33	GND	FC1	GND	FC1	FC1	
	32		GND	GND	FC1	FC1	
27	31			GND	GND	FC1	
21	30			GND		GND	
	29			GND			
	28	GND		GND	GND		
	27		GND	GND	FC1	GND	
26	26			GND	FC1	FC1	
20	25			GND	FC1	FC1	24
	24			GND	FC1	FC1	24
	22	GND		GND	GND	EC1	

	22		GND	GND	FC1	GND				
14	21			GND	FC1	FC1				
14	20			GND	FC1	FC1	10			
	19		_	GND	FC1	FC1	10			
	18	GND		GND	GND	FC1				
	17		GND	GND		GND				
45	16			GND						
15	15			GND	GND					
	14		_	GND		GND				
	13	GND		GND						
	12	FC1	GND	GND			17			
12	11	FC1	FC1	GND			1/			
13	10	FC1	FC1	GND	GND					
	9	FC1	FC1	GND		GND				
	8	GND	FC1	GND						
	7		GND	GND			10			
	6			GND			18			
	5	GND		GND	GND					
	4	FC1	GND	GND	FC1	GND				
	3	FC1	FC1	GND	FC1	FC1				
	2	GND	FC1	GND	GND	FC1				
	1	GND	GND	GND	GND	GND				
12	JS1									
	Pin#	E	D	С	В	Α	20			
	47	GND	GND	GND	GND	GND				
	46	FC1	GND	GND	FC1	GND				
	45	FC1	FC1	GND	FC1	FC1				
	44	GND	FC1	GND	GND	FC1				
	43	FC1	GND	GND		GND				
11	42	FC1	FC1	GND						
11	41	FC1	FC1	GND	GND					
	40	FC1	FC1	GND	FC1	GND				
	39	GND	FC1	GND	FC1	FC1				
	38		GND	GND	FC1	FC1				
	37			GND	FC1	FC1				
	36						19			
	35									
	34									
	33	GND		GND	GND	FC1				

	32	FC1	GND	GND	FC1	GND	
0	31	FC1	FC1	GND	FC1	FC1	
9	30	FC1	FC1	GND	FC1	FC1	
	29	FC1	FC1	GND	FC1	FC1	1
	28	GND	FC1	GND	GND	FC1	
	27		GND	GND		GND	
10	26			GND			
10	25			GND	GND		
	24		_	GND		GND	
	23	GND		GND			
	22		GND	GND			2
	21			GND			2
	20	GND		GND	GND		
	19		GND	GND		GND	
0	18			GND			
0	17			GND			2
	16		_	GND			5
	15	GND		GND	GND		
	14		GND	GND		GND	
-	13			GND			
/	12			GND			c
	11		_	GND			5
	10	GND		GND	GND		
	9		GND	GND		GND	
	8			GND			
	7	GND		GND	GND		
	6		GND	GND		GND	
6	5			GND			
U	4			GND			
	3			GND			4
	2	GND		GND	GND		
	1	GND	GND	GND	GND	GND	

LTDB1 Mapping

	LTDB1									
	JS6									
Pin#	ADC#	E	D	С	В	Α	ADC#			
47		GND	GND	GND	GND	GND				
46		gnd	GND	GND	gnd	GND				
45	24	gnd		GND	gnd	gnd				
44	54	FC2		GND	FC2	gnd	20			
43		FC2	FC2	GND	FC2	FC2	30			
42		GND	FC2	GND	GND	FC2				
41		Out	GND	GND	Out	GND				
40		Out	Out	GND	Out	Out				
39		GND	Out	GND	GND	Out				
38		FC2	GND	GND	FC2	GND				
37		FC2	FC2	GND	FC2	FC2				
36	25									
35	35									
34							37			
33		gnd	FC2	GND	gnd	FC2				
32		gnd	gnd	GND	gnd	gnd				
31		GND	gnd	GND	GND	gnd				
30		gnd	GND	GND	FC3	GND				
29	22	gnd	gnd	GND	FC3	FC3				
28	35	FC2	gnd	GND	FC3	FC3	29			
27		FC2	FC2	GND	FC3	FC3	50			
26		GND	FC2	GND	GND	FC3				
25		Out	GND	GND	gnd	GND				
24		Out	Out	GND	gnd	gnd				
23		GND	Out	GND	FC2	gnd	40			
22		FC2	GND	GND	FC2	FC2	40			
21	22	FC2	FC2	GND	GND	FC2				
20	32	gnd	FC2	GND	Out	GND				
19		gnd	gnd	GND	Out	Out				
18		GND	gnd	GND	GND	Out				
17		gnd	GND	GND	FC2	GND				
16	21	gnd		GND	FC2	FC2				
15		FC2		GND	gnd	FC2	20			
14		FC2	FC2	GND	gnd	gnd	35			
13		GND	FC2	GND	GND	gnd				

							-
12		Out	GND	GND	gnd	GND	
11		Out	Out	GND	gnd	gnd	
10		GND	Out	GND	FC2	gnd	21
9		FC2	GND	GND	FC2	FC2	21
8	20	FC2	FC2	GND	GND	FC2	
7	25	gnd	FC2	GND	Out	GND	
6		gnd	gnd	GND	Out	Out	
5		GND	gnd	GND	GND	Out	
4		gnd	GND	GND	FC2	GND	
3		gnd	gnd	GND	FC2	FC2	
2		GND	gnd	GND	GND	FC2	
1		GND	GND	GND	GND	GND	
	30			JS5			22
Pin#		E	D	С	В	Α	
47		GND	GND	GND	GND	GND	
46		FC2	GND	GND	gnd	GND	
45		FC2	FC2	GND	gnd	gnd	
44		GND	FC2	GND	GND	gnd	
43		Out	GND	GND	FC3	GND	
42		Out	Out	GND	FC3	FC3	
41		GND	Out	GND	FC3	FC3	22
40		FC2	GND	GND	FC3	FC3	23
39	20	FC2	FC2	GND	GND	FC3	
38	28	gnd	FC2	GND	gnd	GND	
37		gnd	gnd	GND	gnd	gnd	
36							
35							
34							25
33		GND	gnd	GND	FC2	gnd	
32		FC3	GND	GND	FC2	FC2	
31	27	FC3	FC3	GND	GND	FC2	
30	27	FC3	FC3	GND	Out	GND	
29		FC3	FC3	GND	Out	Out	
28		GND	FC3	GND	GND	Out	
27		FC3	GND	GND	FC2	GND	
26	26	FC3	FC3	GND	FC2	FC2	
25	20	FC3	FC3	GND	gnd	FC2	24
24		FC3	FC3	GND	gnd	gnd	24
23		GND	FC3	GND	GND	gnd	

22		FC3	GND	GND	gnd	GND	
21	14	FC3	FC3	GND	gnd	gnd	
20	14	FC3	FC3	GND	FC2	gnd	10
19		FC3	FC3	GND	FC2	FC2	16
18		GND	FC3	GND	GND	FC2	
17		FC3	GND	GND	Out	GND	
16	15	FC3	FC3	GND	Out	Out	
15	15	FC3	FC3	GND	GND	Out	
14		FC3	FC3	GND	FC2	GND	
13		GND	FC3	GND	FC2	FC2	
12		gnd	GND	GND	gnd	FC2	17
11	12	gnd	gnd	GND	gnd	gnd	1/
10	15	FC2	gnd	GND	GND	gnd	
9	1	FC2	FC2	GND	FC3	GND	
8		GND	FC2	GND	FC3	FC3	
7		Out	GND	GND	FC3	FC3	10
6		Out	Out	GND	FC3	FC3	18
5		GND	Out	GND	GND	FC3	
4		FC2	GND	GND	gnd	GND	
3		FC2	FC2	GND	gnd	gnd	
2		GND	FC2	GND	GND	gnd	
1		GND	GND	GND	GND	GND	
	12			JS4			20
Pin#		E	D	С	В	Α	20
47		GND	GND	GND	GND	GND	
46		gnd	GND	GND	FC2	GND	
45		gnd	gnd	GND	FC2	FC2	
44		GND	gnd	GND	GND	FC2	
43		gnd	GND	GND	Out	GND	
42	11	gnd	gnd	GND	Out	Out	
41	11	FC2	gnd	GND	GND	Out	
40		FC2	FC2	GND	FC2	GND	
39		GND	FC2	GND	FC2	FC2	
38		Out	GND	GND	gnd	FC2	
37		Out	Out	GND	gnd	gnd	
36							19
35							
34							
33		GND	Out	GND	GND	gnd	

32		FC2	GND	GND	gnd	GND	
31	0	FC2	FC2	GND	gnd	gnd	
30	9	gnd	FC2	GND	FC2	gnd	
29		gnd	gnd	GND	FC2	FC2	1
28		GND	gnd	GND	GND	FC2	
27		gnd	GND	GND	Out	GND	
26	10	gnd	gnd	GND	Out	Out	
25	10	FC2	gnd	GND	GND	Out	
24		FC2	FC2	GND	FC2	GND	
23		GND	FC2	GND	FC2	FC2	
22		Out	GND	GND	gnd	FC2	2
21		Out	Out	GND	gnd	gnd	2
20		GND	Out	GND	GND	gnd	
19		FC2	GND	GND	FC3	GND	
18		FC2	FC2	GND	FC3	FC3	
17	0	gnd	FC2	GND	FC3	FC3	2
16		gnd	gnd	GND	FC3	FC3	3
15		GND	gnd	GND	GND	FC3	
14		gnd	GND	GND	gnd	GND	
13	7	gnd	gnd	GND	gnd	gnd	
12	1	FC2	gnd	GND	FC2	gnd	c.
11		FC2	FC2	GND	FC2	FC2	J
10		GND	FC2	GND	GND	FC2	
9		Out	GND	GND	Out	GND	
8		Out	Out	GND	Out	Out	
7		GND	Out	GND	GND	Out	
6		FC2	GND	GND	FC2	GND	
5	6	FC2	FC2	GND	FC2	FC2	
4	0	gnd	FC2	GND	gnd	FC2	
3		gnd	gnd	GND	gnd	gnd	4
2		GND	gnd	GND	GND	gnd	
1		GND	GND	GND	GND	GND	

Is this scheme feasible?

- Preliminary routing indicates this scheme will be easier to route than the original.
- The tower driver board connectors don't need to be swapped.

Layer Sum Board, Rev B

- Redesigned to equalize delay
- Now using single stage non-inverting summing circuits



LSB Block Diagram



Summing Stage



.