Forward Calorimeter Baseplane and FC1 Layer Sum Board

D. Tompkins

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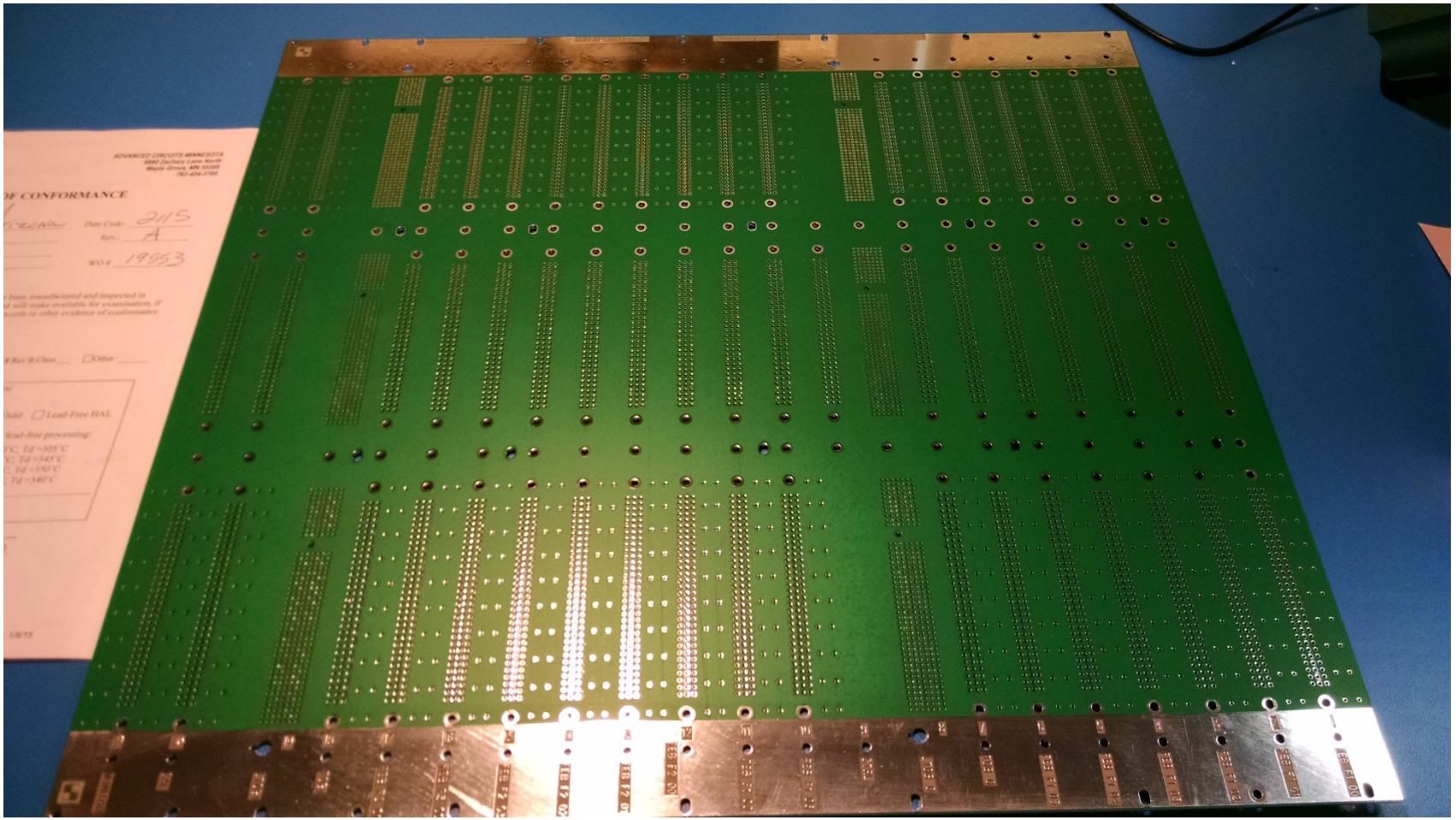
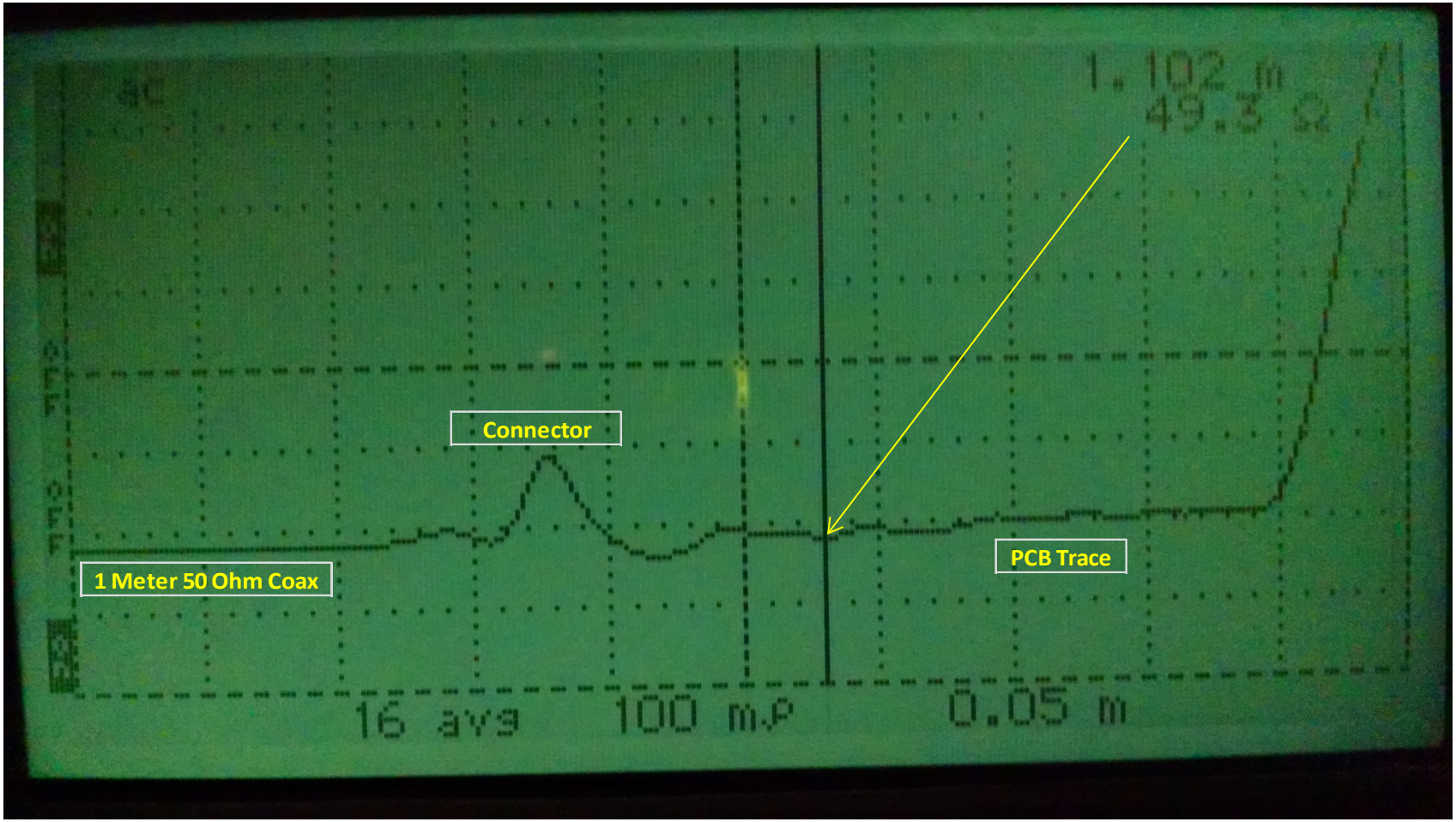
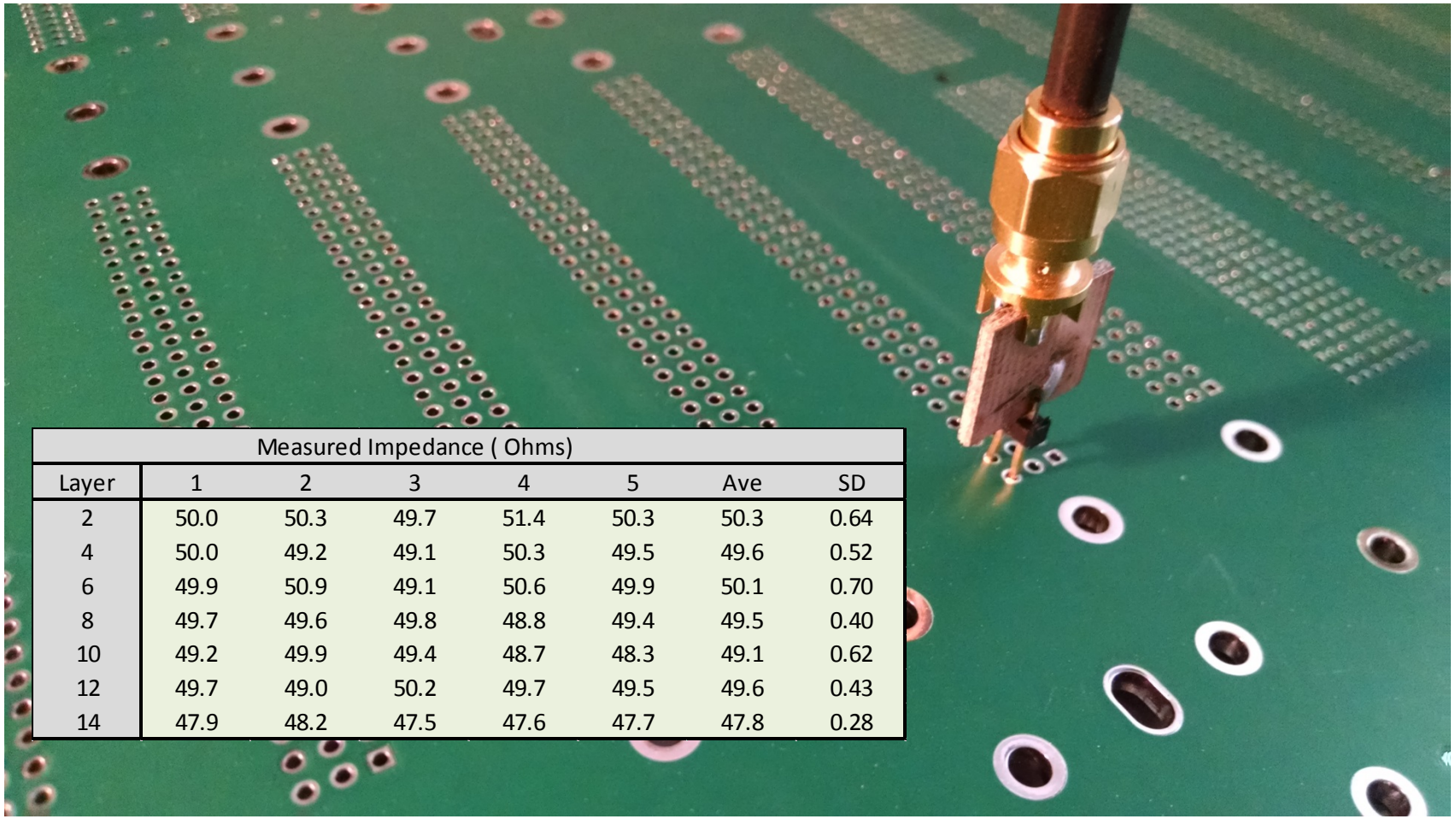
Rev A Prototype in Hand



TDR testing shows trace impedance very close to 50 Ohms



Data from 5 traces on each of the 7 routing layers:



Measured Impedance (Ohms)							
Layer	1	2	3	4	5	Ave	SD
2	50.0	50.3	49.7	51.4	50.3	50.3	0.64
4	50.0	49.2	49.1	50.3	49.5	49.6	0.52
6	49.9	50.9	49.1	50.6	49.9	50.1	0.70
8	49.7	49.6	49.8	48.8	49.4	49.5	0.40
10	49.2	49.9	49.4	48.7	48.3	49.1	0.62
12	49.7	49.0	50.2	49.7	49.5	49.6	0.43
14	47.9	48.2	47.5	47.6	47.7	47.8	0.28

Some issues:

- Non-plated through holes are flooded over.
- Unused pads removed on all internal layers. This was done to minimize crosstalk and preserve the ground plane as much as possible.
- Current vertical dimension is at maximum for panel size. Any increase would require moving to the next larger panel size

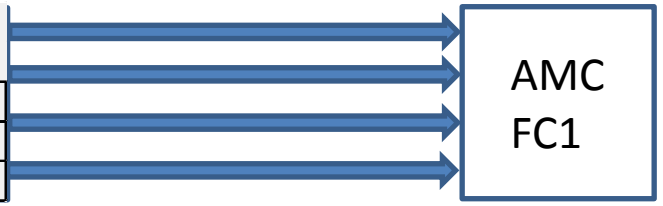
One major problem

- A new mapping scheme is needed to be compatible with the Back End Readout

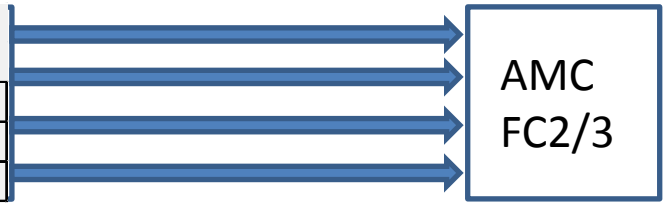
New Mapping Scheme

- The Back End System requires LTDB0 to handle all of the FCAL 1 trigger groups

LTDB0	FCal1	FCal2	FCal3	Total
Hi-Z	0	0	0	0
Lo-Z	192	0	0	192
Outputs	0	0	0	0



LTDB1	FCal1	FCal2	FCal3	Total
Hi-Z	0	0	64	64
Lo-Z	0	128	0	128
Outputs	0	64	0	64



LTDB0 Mapping

LTDB0

JS3

ADC#	Pin#	E	D	C	B	A	ADC#
	47	GND	GND	GND	GND	GND	
	46	FC1	GND	GND	FC1	GND	
34	45	FC1	FC1	GND	FC1	FC1	
	44	FC1	FC1	GND	FC1	FC1	36
	43	FC1	FC1	GND	FC1	FC1	
	42	GND	FC1	GND	GND	FC1	
	41		GND	GND		GND	
	40			GND			
	39	GND		GND	GND		
	38	FC1	GND	GND	FC1	GND	
35	37	FC1	FC1	GND	FC1	FC1	
	36						
	35						
	34						37
	33	FC1	FC1	GND	FC1	FC1	
	32	FC1	FC1	GND	FC1	FC1	
	31	GND	FC1	GND	GND	FC1	
	30	FC1	GND	GND		GND	
33	29	FC1	FC1	GND			
	28	FC1	FC1	GND			38
	27	FC1	FC1	GND			
	26	GND	FC1	GND	GND		
	25		GND	GND	FC1	GND	
	24			GND	FC1	FC1	
	23	GND		GND	FC1	FC1	
	22	FC1	GND	GND	FC1	FC1	40
32	21	FC1	FC1	GND	GND	FC1	
	20	FC1	FC1	GND		GND	
	19	FC1	FC1	GND			
	18	GND	FC1	GND	GND		
	17	FC1	GND	GND	FC1	GND	
31	16	FC1	FC1	GND	FC1	FC1	
	15	FC1	FC1	GND	FC1	FC1	
	14	FC1	FC1	GND	FC1	FC1	39
	13	GND	FC1	GND	GND	FC1	

JS2

	12		GND	GND	FC1	GND	
	11			GND	FC1	FC1	
	10	GND		GND	FC1	FC1	
29	9	FC1	GND	GND	FC1	FC1	21
	8	FC1	FC1	GND	GND	FC1	
	7	FC1	FC1	GND		GND	
	6	FC1	FC1	GND			
	5	GND	FC1	GND	GND		
	4	FC1	GND	GND	FC1	GND	
30	3	FC1	FC1	GND	FC1	FC1	
	2	GND	FC1	GND	GND	FC1	
	1	GND	GND	GND	GND	GND	

Pin#	E	D	C	B	A	
47	GND	GND	GND	GND	GND	
46	FC1	GND	GND	FC1	GND	
45	FC1	FC1	GND	FC1	FC1	
44	GND	FC1	GND	GND	FC1	22
43		GND	GND		GND	
42			GND			
41	GND		GND			
40	FC1	GND	GND			
39	FC1	FC1	GND	GND		
38	FC1	FC1	GND	FC1	GND	
37	FC1	FC1	GND	FC1	FC1	23
36						
35						
34						
33	GND	FC1	GND	FC1	FC1	
32		GND	GND	FC1	FC1	
31			GND	GND	FC1	
30			GND		GND	
29			GND			
28	GND		GND	GND		
27		GND	GND	FC1	GND	
26			GND	FC1	FC1	
25			GND	FC1	FC1	
24			GND	FC1	FC1	
23	GND		GND	GND	FC1	

	22		GND	GND	FC1	GND	
14	21			GND	FC1	FC1	
	20			GND	FC1	FC1	
	19			GND	FC1	FC1	16
	18	GND		GND	GND	FC1	
	17		GND	GND		GND	
15	16			GND			
	15			GND	GND		
	14			GND		GND	
	13	GND		GND			
	12	FC1	GND	GND			
13	11	FC1	FC1	GND			17
	10	FC1	FC1	GND	GND		
	9	FC1	FC1	GND		GND	
	8	GND	FC1	GND			
	7		GND	GND			
	6			GND			18
	5	GND		GND	GND		
	4	FC1	GND	GND	FC1	GND	
12	3	FC1	FC1	GND	FC1	FC1	
	2	GND	FC1	GND	GND	FC1	
	1	GND	GND	GND	GND	GND	

JS1

Pin#	E	D	C	B	A	
47	GND	GND	GND	GND	GND	
46	FC1	GND	GND	FC1	GND	
45	FC1	FC1	GND	FC1	FC1	
44	GND	FC1	GND	GND	FC1	20
43	FC1	GND	GND		GND	
42	FC1	FC1	GND			
41	FC1	FC1	GND	GND		
40	FC1	FC1	GND	FC1	GND	
39	GND	FC1	GND	FC1	FC1	
38		GND	GND	FC1	FC1	
37			GND	FC1	FC1	
36						19
35						
34						
33	GND		GND	GND	FC1	

	32	FC1	GND	GND	FC1	GND	
9	31	FC1	FC1	GND	FC1	FC1	
	30	FC1	FC1	GND	FC1	FC1	1
	29	FC1	FC1	GND	FC1	FC1	
	28	GND	FC1	GND	GND	FC1	
	27		GND	GND		GND	
10	26			GND			
	25			GND	GND		
	24			GND		GND	
	23	GND		GND			
	22		GND	GND			2
	21			GND			
	20	GND		GND	GND		
	19		GND	GND		GND	
8	18			GND			
	17			GND			3
	16			GND			
	15	GND		GND	GND		
	14		GND	GND		GND	
7	13			GND			
	12			GND			5
	11			GND			
	10	GND		GND	GND		
	9		GND	GND		GND	
	8			GND			
	7	GND		GND	GND		
	6		GND	GND		GND	
6	5			GND			
	4			GND			4
	3			GND			
	2	GND		GND	GND		
	1	GND	GND	GND	GND	GND	

LTDB1 Mapping

LTDB1 — JS6

Pin#	ADC#	E	D	C	B	A	ADC#
47		GND	GND	GND	GND	GND	
46		gnd	GND	GND	gnd	GND	
45	34	gnd		GND	gnd	gnd	
44		FC2		GND	FC2	gnd	36
43		FC2	FC2	GND	FC2	FC2	
42		GND	FC2	GND	GND	FC2	
41		Out	GND	GND	Out	GND	
40		Out	Out	GND	Out	Out	
39		GND	Out	GND	GND	Out	
38		FC2	GND	GND	FC2	GND	
37		FC2	FC2	GND	FC2	FC2	
36	35						
35							
34							37
33		gnd	FC2	GND	gnd	FC2	
32		gnd	gnd	GND	gnd	gnd	
31		GND	gnd	GND	GND	gnd	
30		gnd	GND	GND	FC3	GND	
29	33	gnd	gnd	GND	FC3	FC3	
28		FC2	gnd	GND	FC3	FC3	38
27		FC2	FC2	GND	FC3	FC3	
26		GND	FC2	GND	GND	FC3	
25		Out	GND	GND	gnd	GND	
24		Out	Out	GND	gnd	gnd	
23		GND	Out	GND	FC2	gnd	40
22		FC2	GND	GND	FC2	FC2	
21	32	FC2	FC2	GND	GND	FC2	
20		gnd	FC2	GND	Out	GND	
19		gnd	gnd	GND	Out	Out	
18		GND	gnd	GND	GND	Out	
17		gnd	GND	GND	FC2	GND	
16	31	gnd		GND	FC2	FC2	
15		FC2		GND	gnd	FC2	39
14		FC2	FC2	GND	gnd	gnd	
13		GND	FC2	GND	GND	gnd	

JS5

Pin#	E	D	C	B	A
47	GND	GND	GND	GND	GND
46	FC2	GND	GND	gnd	GND
45	FC2	FC2	GND	gnd	gnd
44	GND	FC2	GND	GND	gnd
43	Out	GND	GND	FC3	GND
42	Out	Out	GND	FC3	FC3
41	GND	Out	GND	FC3	FC3
40	FC2	GND	GND	FC3	FC3
39	FC2	FC2	GND	GND	FC3
38	gnd	FC2	GND	gnd	GND
37	gnd	gnd	GND	gnd	gnd
36					
35					
34					
33	GND	gnd	GND	FC2	gnd
32	FC3	GND	GND	FC2	FC2
31	FC3	FC3	GND	GND	FC2
30	FC3	FC3	GND	Out	GND
29	FC3	FC3	GND	Out	Out
28	GND	FC3	GND	GND	Out
27	FC3	GND	GND	FC2	GND
26	FC3	FC3	GND	FC2	FC2
25	FC3	FC3	GND	gnd	FC2
24	FC3	FC3	GND	gnd	gnd
23	GND	FC3	GND	GND	gnd

JS4

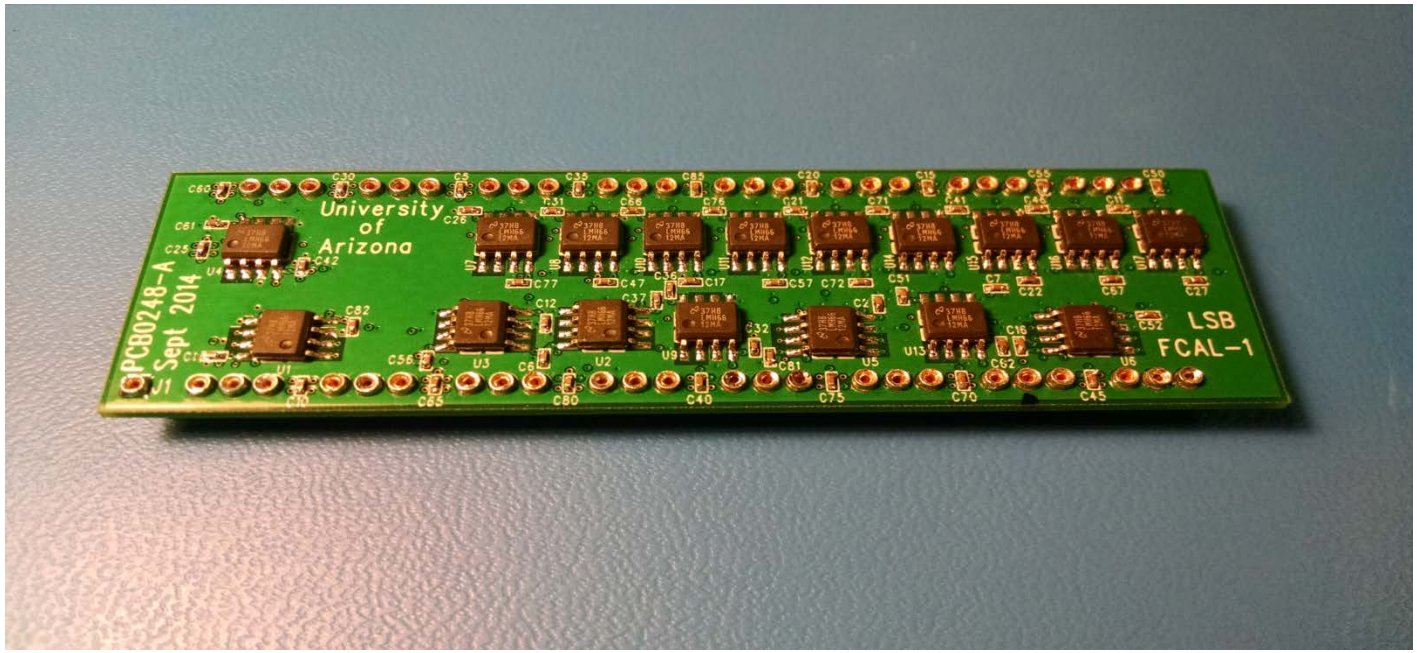
Pin#	E	D	C	B	A
47	GND	GND	GND	GND	GND
46	gnd	GND	GND	FC2	GND
45	gnd	gnd	GND	FC2	FC2
44	GND	gnd	GND	GND	FC2
43	gnd	GND	GND	Out	GND
42	gnd	gnd	GND	Out	Out
41	FC2	gnd	GND	GND	Out
40	FC2	FC2	GND	FC2	GND
39	GND	FC2	GND	FC2	FC2
38	Out	GND	GND	gnd	FC2
37	Out	Out	GND	gnd	gnd
36					
35					
34					
33	GND	Out	GND	GND	gnd

Is this scheme feasible?

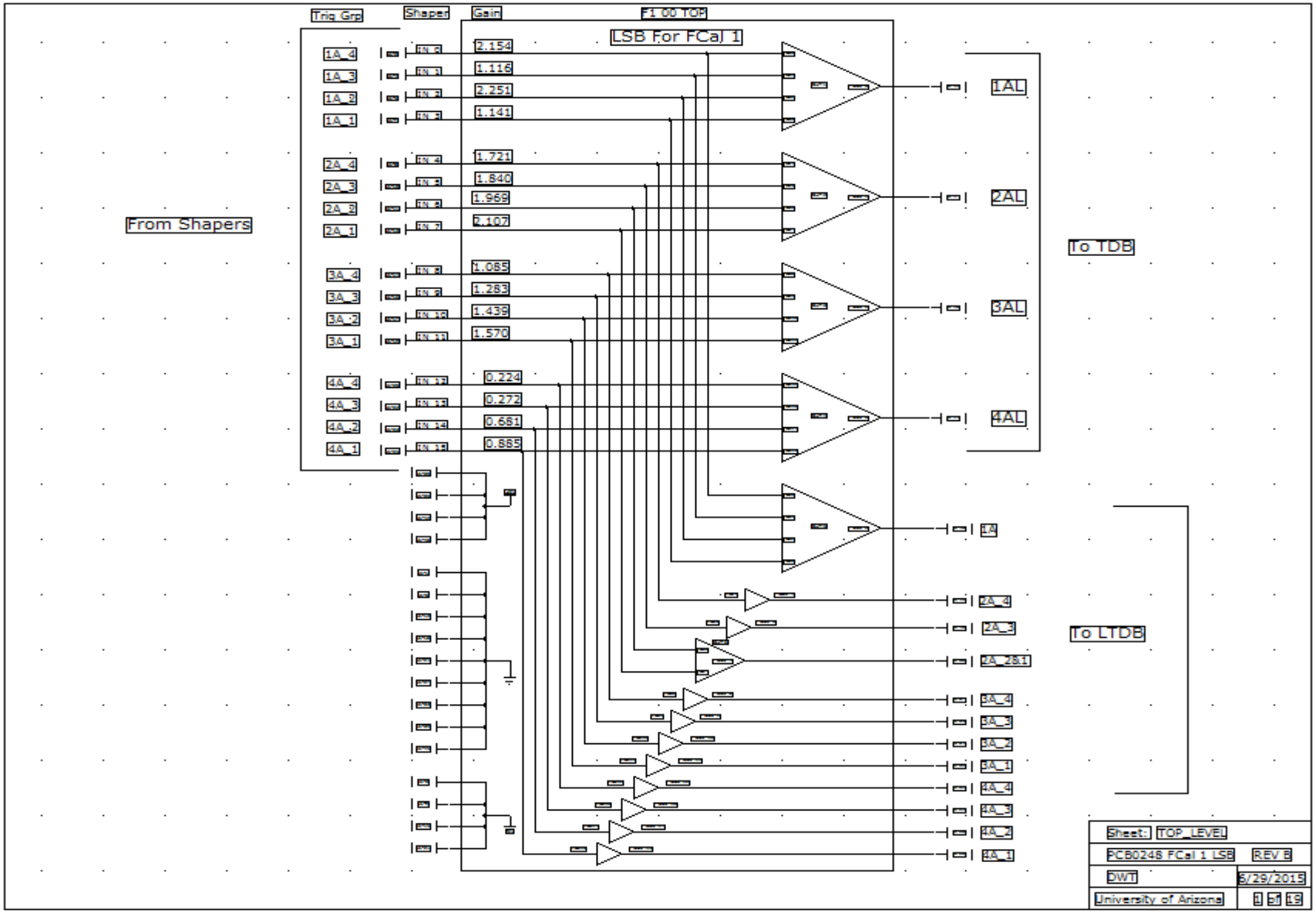
- Preliminary routing indicates this scheme will be easier to route than the original.
- The tower driver board connectors don’t need to be swapped.

Layer Sum Board, Rev B

- Redesigned to equalize delay
- Now using single stage non-inverting summing circuits



LSB Block Diagram



Summing Stage