

Leak 2

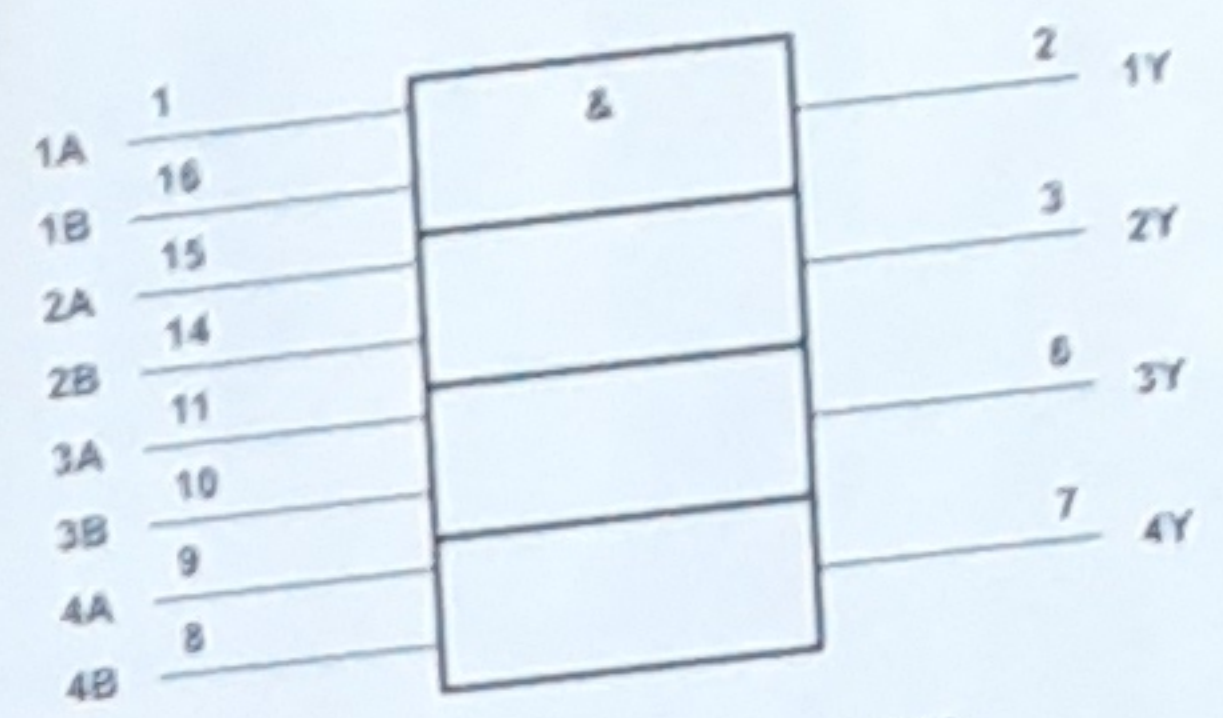
QUADRUPLE 2-INPUT...

Architecture Optimizes
VCC and GND Configurations
High-Speed Switching Noise
High-Performance Implanted
Process
High Latch-Up Immunity at
High Temperatures
Options Include Plastic
SOIC (D) and Thin Shrink
SOIC (PW) Packages, and
Plastic 300-mil DIPs (N)

contains four independent 2-input AND gates. It performs the function $Y = \overline{A} + \overline{B}$ in positive logic.
The device is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L



This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



Please be aware that an important notice concerning availability, standard warranty, and Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS
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top" as a function of
of 50mV/100mV
different scope

charge early dynamic bias?

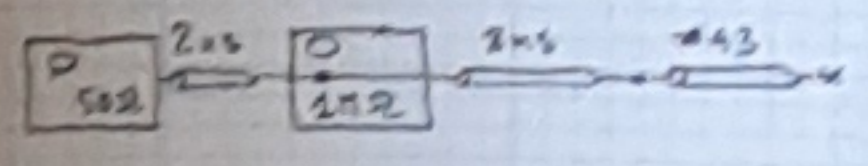
to
with
with
with

Procedure 11.09-02.07.2018

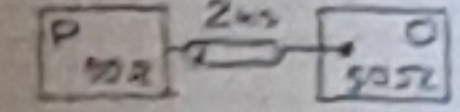
43.96 Measurements of TF of Characteristic
Cable #43 (~40m)

All measurements done with pulser B&K 4005
pulse period: 2µs PW 20µs
oscilloscope TDS2054, CH1 in sample
mode, TRIG from CH1

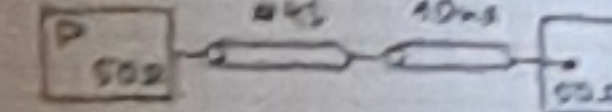
1. TDR-like waveform
Vp = 2V H scale 200ns/div 500pt
file: tek0002.tst



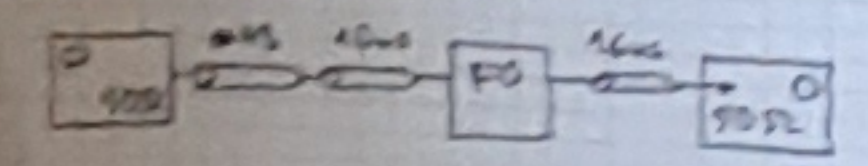
2. Full SWR waveform
Vp = 400mV H scale 100ns/div 100pt
file: tek0001.tst



3. Long cable TF
Vp = 400mV H scale 100ns/div 10x pt
file: tek0002.tst

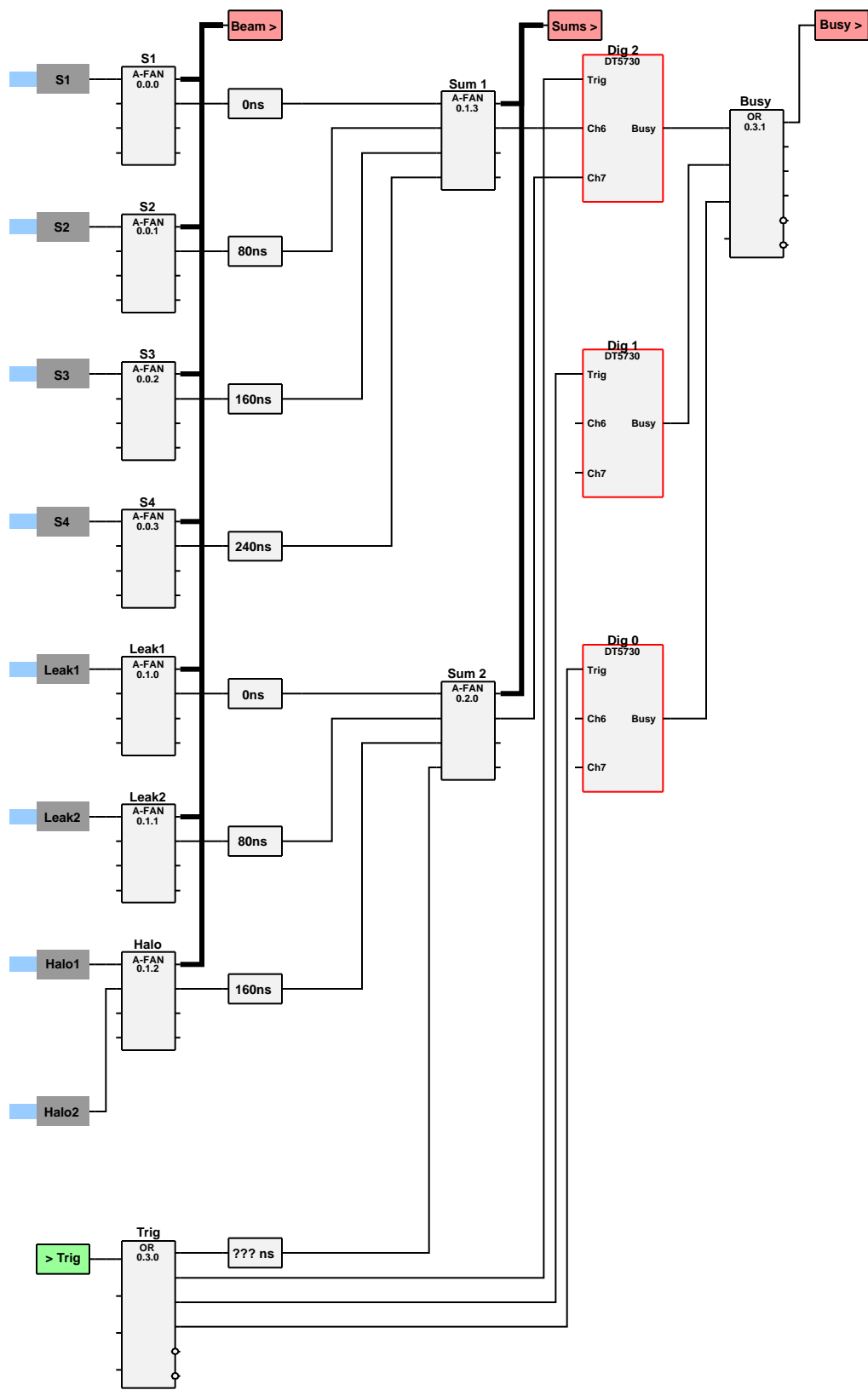


4. Full setup
Vp = 400mV H scale 100ns/div 100pt
file: tek0005.tst



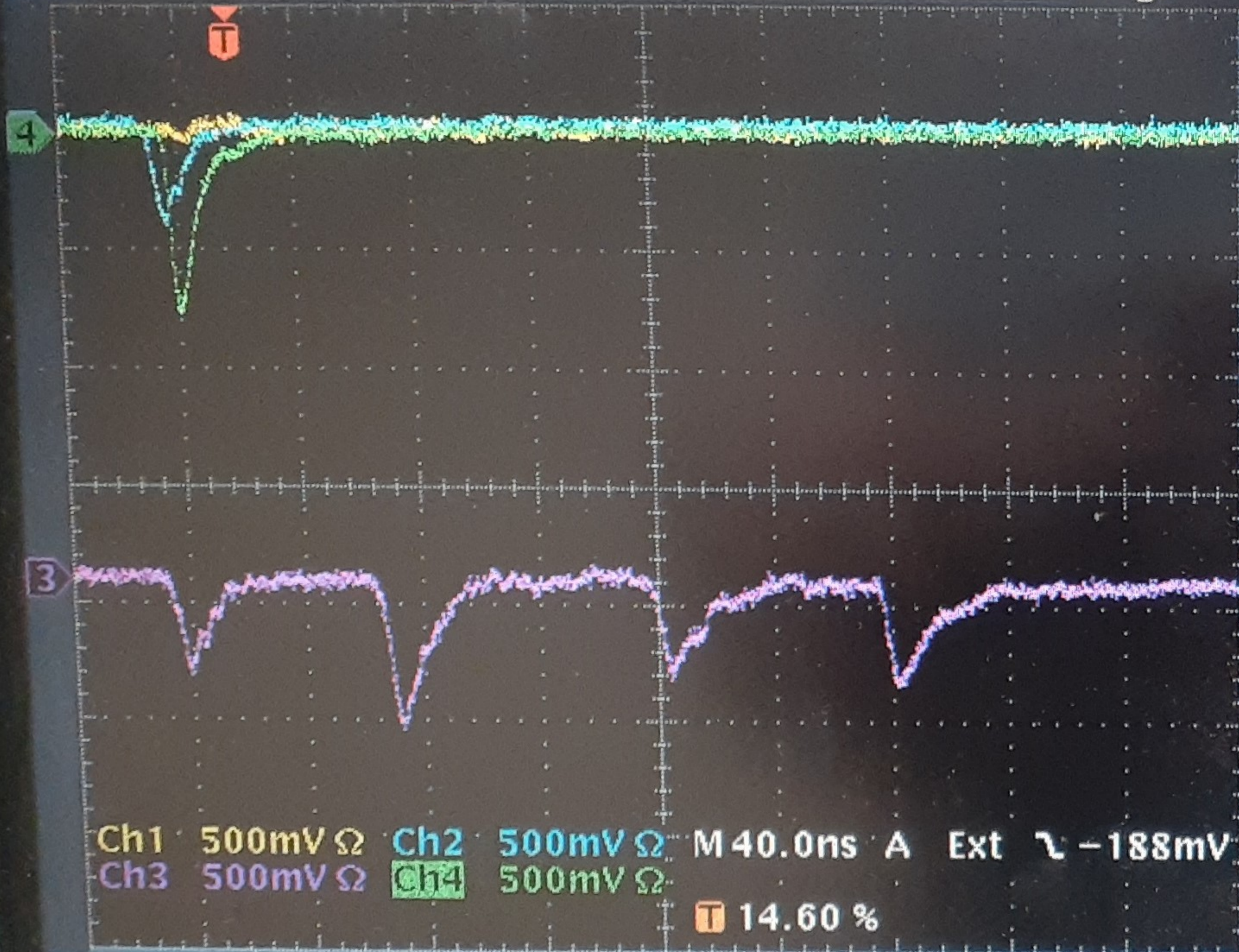
WORKING
5-31-90
E-800

Beam Area



Run

Trig?



A Trigger Source

Ext

Ext/10

Ext Probe

1X

Voltage



AC Line

-more-
2 of 3

Ch1 500mV Ω Ch2 500mV Ω M 40.0ns A Ext \sim -188mV
 Ch3 500mV Ω Ch4 500mV Ω
 T 14.60 %

Type
Edge

Source
Ext

Coupling
DC

Slope
 \sim

Level
-188mV

Mode
Normal
& Holdoff

Trigger

